TEXAS INSTRUMENTS

Data Transmission Circuits

Communications Controllers

Data Book

Volume 2

1996

Mixed-Signal Products

General Information 1
UARTs 2
UART Product Previews 3
IEEE-1394 4
IEEE-1394 Product Previews 5
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Data Transmission Circuits Data Book

Volume 2

Communications Controllers

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INTRODUCTION

In the 1996 ***Data Transmission Circuits Data Book, Volume 2***, the Mixed-Signal Products Division of Texas Instruments (TI) presents technical information on various products for electronic media and electronic devices.

The TI data transmission circuits represent technologies from classic bipolar through Advanced Low-Power Schottky (ALS), IMPACT™, LinBiCMOS™, CMOS, and BiMOS processes. The ALS and IMPACT oxide-isolated technologies provide the data transmission family with improved speed-power characteristics.

This data book provides information on the following types of products:

- UARTs
- Plug-and-play compatible devices
- Infrared serial data inputs and outputs
- IEEE 1394-1995

Among the new products offered by TI within the 1996 Data Transmission Circuits Data Book, Volume 2 are:

- TL16PNP100A – a standalone plug-and-play controller.
- TL16PNP550A – the industry's first UART with plug-and-play capability.
- TL16C750 – a UART with a 64-byte FIFO buffer that reduces the number of interrupt requests.
- TSB21LV03 – a 1394 triple cable transceiver/arbiter that provides three fully compliant cable ports at 100/200 Mbits/s
- TSB11LV01 – a 1-port 1394 cable transceiver/arbiter for 3-V supply operation at 100 Mbits/s
- TSB14C01 – a 1-port 1394 backplane transceiver/arbiter that provides the transceiver functions needed to implement a single port node at 50/100 Mbits/s in a backplane-based 1394 network.

The data book is organized for quick location of a specific data sheet. The sequence is in base part number order (i.e., TL16C450 is located next to the TL16C451). The alphanumeric index provides a quick method of locating the data sheet for a known part number and indicates new products in this edition. A preview of new products that are near release to production are included for the first time in this data book.

The selection guide is grouped by industry standard and includes key features and the standard device footprint of the products in each category. The cross-reference guide lists other manufacturers' devices with the suggested TI replacement. Package mechanical information is in the last section of the data book.

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While this data book offers design and specification data only for data transmission products, complete technical data for any TI semiconductor product is available from your nearest TI Field Sales Office, local authorized TI distributor, or by writing directly to:

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We sincerely believe the new 1996 *Data Transmission Circuits Data Book, Volume 2* will be a valuable addition to your collection of technical literature.

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1 General Information

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TL16C451	Asynchronous Communications Element	2–33
TL16C452	Asynchronous Communications Element	2–33
TL16C550A	Asynchronous Communications Element	2–57
TL16C550B	Asynchronous Communications Element	2–87
TL16C550C	Asynchronous Communications Element with Autoflow Control	2–117
TL16C552	Dual Asynchronous Communications Element with FIFO	2–151
TL16C552A	Dual Asynchronous Communications Element with FIFO	2–183
TL16C552AI	Dual Asynchronous Communications Element with FIFO	2–217
TL16C554	Asynchronous Communications Element	2–251
TL16C750	Asynchronous Communications Element with 64-Byte FIFOs and Autoflow Control	2–281
TL16PC564A	PCMCIA Universal Asynchronous Receiver Transmitter	2–315
TL16PIR552	Dual UART with Dual IrDA and 1284 Parallel Port	3–3
TL16PNP100A	Standalone Plug-and-Play (PnP) Controller	2–347
TL16PNP200†	Standalone Plug-and-Play (PnP) Controller	3–5
TL16PNP550A	Asynchronous Communications Element with Plug-and-Play and Autoflow Control	2–365
TSB11C01	IEEE 1394-1995 Triple-Cable Transceiver/Arbiter	4–3
TSB11LV01†	1-Port P1394 Cable Transceiver/Arbiter For 3-Volt Supply Operation	5–3
TSB12C01A	1394 High-Speed Serial-Bus Link-Layer Controller	4–21
TSB12C01AM†	P1394 High-Speed Serial-Bus Link-Layer Controller	5–7
TSB14C01†	P1394 Backplane Transceiver/Arbiter For 5-Volt Supply Operation	5–21
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TSB21LV03†	P1394 Triple-Cable Transceiver/Arbiter	5–25
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† This is a product preview data sheet.

SELECTION GUIDE

UARTs

DEVICE	DEVICE TYPE†	DESCRIPTION‡	PACKAGES	PAGE
TIR1000	IR	Standalone IrDA encoder and decoder	PS	2–3
TL16C450	UART	Single ACE without FIFO	FN, N	2–9
TL16C451	UART	Single ACE with parallel port and without FIFO	FN	2–33
TL16C452	UART	Dual ACE with parallel port and without FIFO	FN	2–33
TL16C550A	UART	Single ACE with FIFO	FN, N	2–57
TL16C550B	UART	Single ACE with 16-byte FIFOs	FN, N, PT	2–87
TL16C550C	UART	Single ACE with 16-byte FIFOs and auto flow control	FN, N, PT	2–117
TL16C552	UART	Dual ACE with 16-byte FIFOs and parallel port	FN	2–151
TL16C552A	UART	Dual ACE with 16-byte FIFOs and parallel port	FN	2–183
TL16C552AI	UART	Dual ACE with 16-byte FIFOs and parallel port characterized over industrial temperature range	FN	2–217
TL16C554	UART	Quadruple ACE with 16-byte FIFOs	FN	2–251
TL16C750	UART	Single ACE with 64-byte FIFOs, autoflow control, and low-power modes	FN, PM	2–281
TL16PC564A	UART, PCMCIA	Single ACE with 64-byte FIFOs and PCMCIA interface	PZ	2–315
TL16PIR552§	UART, IR	Dual ACE with 16-byte FIFOs and has selectable IR and 1284 modes	n/a	3–3
TL16PNP100A	PnP	Standalone PnP controller that supports two logical devices	FN, PT	2–347
TL16PNP200§	PnP	Standalone PnP controller that supports five logical devices	n/a	3–5
TL16PNP550A	UART, PnP	Single ACE with 64-byte FIFOs, autoflow control, and PnP controller	FN	2–365

† UART = universal asynchronous receivers/transmitters, PCMCIA = Personal Computer Memory Card International Association , PnP = plug and play, IR = ifrared.
‡ ACE = asynchronous communications element , FIFO = first in/first out, IrDA = Infrared Data Association
§ The data sheet for this device is product preview.

IEEE 1394-1995

DEVICE	DESCRIPTION	PACKAGE	PAGE
TSB11C01	Triple-cable transceiver/arbiter	DL	4–3
TSB11LV01†	Triple-cable transceiver/arbiter	—	5–3
TSB12C01A	High-speed serial-bus link-layer controller	PZ	4–21
TSB12C01AM†	High-speed serial-bus link-layer controller	WN	5–7
TSB14C01†	P1394 Single-Port Backplane Transceiver/Arbiter For 5-Volt Supply Operation	—	5–21
TSB14C01M†	P1394 Single-Port Backplane Transceiver/Arbiter For 5-Volt Supply Operation	WD	5–23
TSB21LV03†	Triple-cable transceiver/arbiter	—	5–25
TSB21LV03M†	Triple-cable transceiver/arbiter	HV	5–29

† The data sheet for this device is product preview.

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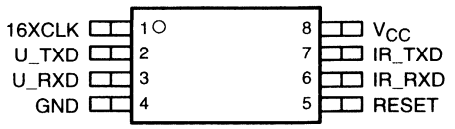
2 UARTs

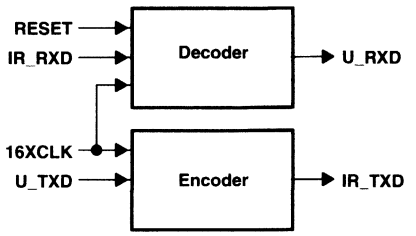
SLLS228A – DECEMBER 1995 – REVISED FEBRUARY 1996

- **Adds Infrared (IR) Port to Universal Asynchronous Receiver Transmitter (UART)**
- **Compatible with Infrared Data Association (IrDA) & Hewlett Packard Serial Infrared (HPSIR)**
- **Provides 1200 bps to 115 kbps Data Rate**
- **Uses 2.7-V to 5.5-V Supply**
- **Provides Simple Interface With UART**
- **Decodes Negative or Positive Pulses**
- **Available in 8-Pin Small Outline Package (SOP)**

PS PACKAGE
(TOP VIEW)



functional block diagram



description

The TIR1000 serial infrared (SIR) encoder/ decoder is a CMOS device which encodes and decodes bit data in conformance with the IrDA specification.

A transceiver device is needed to interface to the photo-sensitive diode (PIN) and the light emitting diode (LED). A UART is needed to interface to the serial data lines.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
16XCLK	1	I	Clock signal. 16XCLK should be set to 16 times the baud rate. The highest baud rate for IrDA is 115.2 kbps, for which the clock frequency equals to 1.843 MHz (this terminal is tied to the BAUDOUT of a UART).
GND	4		Ground
IR_RXD	6	I	Infrared receiver data. IR_RXD is IRDA-SIR modulated input from an optoelectronics transceiver whose input pulses should be 3/16 of the baud rate period.
IR_TXD	7	O	Infrared transmitter data. IR_TXD is IRDA-SIR modulated output to an optoelectronics transceiver.
RESET	5	I	Active high reset. RESET initializes a IRDA-SIR decode/encode state machine (this terminal is tied to a UART reset line).
U_RXD	3	O	Receiver data. U_RXD is decoded (demodulated) data from IR_RXD per the IRDA specification (this terminal is tied to SIN of a UART).
U_TXD	2	I	Transmitter data. U_TXD is encoded (modulated) data and output data as IR_TXD (this terminal is tied to SOUT from a UART).
V_{CC}	8		Power supply. The V_{CC} requirement is 2.7 V to 5.5 V

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... –0.5 V to 6 V
Input voltage range at any input, V_I ..... –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O ..... –0.5 V to V_{CC} + 0.5 V
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Case temperature for 10 seconds: SOP package ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage levels are with respect to GND.

recommended operating conditions over recommended operating free-air temperature range

low voltage (3 V nominal)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	2.7	3	3.3	V
High-level input voltage, V_{IH}	0.7 V_{CC}			V
Low-level input voltage, V_{IL}			0.2 V_{CC}	V
Operating free-air temperature, T_A	0		70	°C

standard voltage (5 V nominal)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	0.7 V_{CC}			V
Low-level input voltage, V_{IL}			0.2 V_{CC}	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA	V_{CC} = 5 V	V_{CC} – 0.8			V
		I_{OH} = –1.8 mA	V_{CC} = 3 V	V_{CC} – 0.55			
V_{OL}	Low-level output voltage	I_{OL} = +4 mA	V_{CC} = 5 V			0.5	V
		I_{OL} = +1.8 mA	V_{CC} = 3 V			0.5	
I_I	Input current	V_I = 0 to V_{CC},	All other pins floating			± 1	µA
I_{CC}	Supply current	V_{CC} = 5.25 V, All inputs at 0.2 V, No load on outputs	T_A = 25°C, 16XCLK at 2 Mhz,			1	mA
$C_{i(16XCLK)}$	Clock input capacitance				5		pF
$f_{(16XCLK)}$	Clock frequency					2	MHz

switching characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
tr	Output rise time	$C_{(LOAD)}$ = 15 pF (10% to 90%)		1.3		ns
tf	Output fall time	$C_{(LOAD)}$= 15 pF (90% to 10%)		1.8		ns

† Typical values are at T_A = 25°C.

APPLICATION

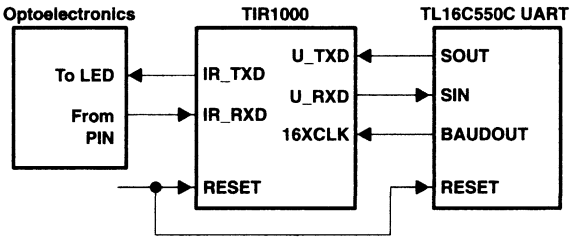


Figure 1. Typical application of the TIR1000

PRINCIPLES OF OPERATION

IrDA overview

The Infrared Data Association (IrDA) defines several protocols for sending and receiving serial infrared data, including rates of 115.2 kbps, 0.576 Mbps, 1.152 Mbps, and 4 Mbps. The low rate of 115.2 kbps was specified first and the others must maintain downward compatibility with it. At the 115.2 kbps rate, the protocol implemented in the hardware is fairly simple. It primarily defines a serial infrared data "word" to be surrounded by a start bit equal to 0 and a stop bit equal to 1. Individual bits are encoded or decoded the same whether they are start, data, or stop bits. The TIR1000 evaluates only single bits and only follows the 115.2 kbps protocol. The 115.2 kbps rate is a maximum rate. When both ends of the transfer are set up to a lower but matching speed, the protocol (with the TIR1000) still works. The clock used to code or sample the data is 16 times the baud rate, or 1.843 Mhz maximum. To code a 1, no pulse is sent or received for 1-bit time period, or 16 clock cycles. To code a 0, one pulse is sent or received within a 1-bit time period, or 16 clock cycles. The pulse must be at least 1.6 µs wide and 3 clock cycles long at 1.843 Mhz. At lower baud rates the pulse can be 1.6 µs wide or as long as 3 clock cycles. The transmitter output, IR_TXD, is intended to drive a LED circuit to generate an infrared pulse. The LED circuits work on positive pulses. A PIN circuit is expected to create the receiver input, IR_RXD. Most, but not all, PIN circuits have inversion and generate negative pulses from the detected infrared light. Their output is normally high. The TIR1000 can decode either negative or positive pulses on IR_RXD.

PRINCIPLES OF OPERATION

IrDA encoder function

Serial data from a UART is encoded to transmit data to the optoelectronics. While the serial data input to this block (U_TXD) is high, the output (IR_TXD) is always low, and the counter used to form a pulse on IR_TXD is continuously cleared. After U_TXD resets to 0, IR_TXD rises on the falling edge of the seventh 16XCLK. On the falling edge of the tenth 16XCLK pulse, IR_TXD falls, creating a 3-clock-wide pulse. While U_TXD stays low, a pulse is transmitted during the seventh to tenth clocks of each 16-clock bit cycle.

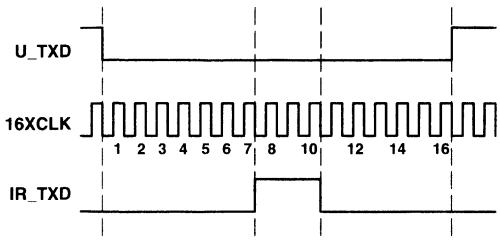


Figure 2. IrDA-SIR Encoding Scheme – Detailed Timing Diagram

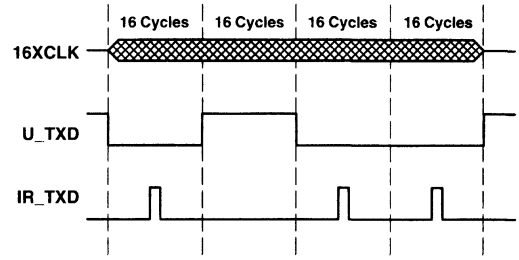


Figure 3. Encoding Scheme – Macro View

IrDA decoder function

After reset, U_RXD is high and the 4-bit counter is cleared. When a falling edge is detected on IR_RXD, U_RXD falls on the next rising edge of 16XCLK with sufficient setup time. U_RXD stays low for 16 (16XCLK) cycles and then returns to high as required by the IrDA specification. As long as no pulses (falling edges) are detected on IR_TXD, U_RXD stays high.

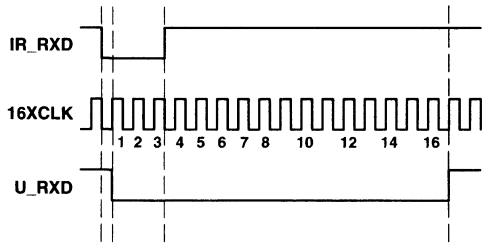


Figure 4. IrDA-SIR Decoding Scheme – Detailed Timing Diagram

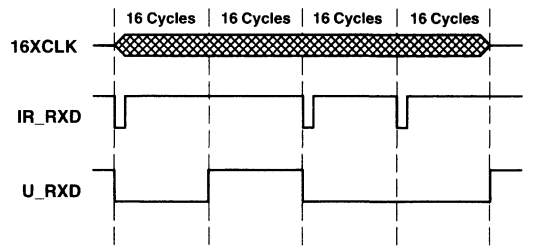


Figure 5. Decoding Scheme – Macro View

PRINCIPLES OF OPERATION

It is possible for jitter or slight frequency differences to cause the next falling edge on IR_RXD to be missed for one 16XCLK cycle. In that case, a 1-clock wide pulse appears on U_RXD between consecutive zeroes. It is important for the UART to strobe U_RXD in the middle of the bit time to avoid latching this temporary value. The TL16C550C UART already strobes incoming serial data at the proper time. Otherwise, note that data is required to be framed by a leading zero and a trailing one. The falling edge of that first zero on U_RXD synchronizes the read strobe. The strobe is on the eighth 16XCLK pulse after the U_RXD falling edge and once every 16 cycles thereafter until the stop bit occurs.

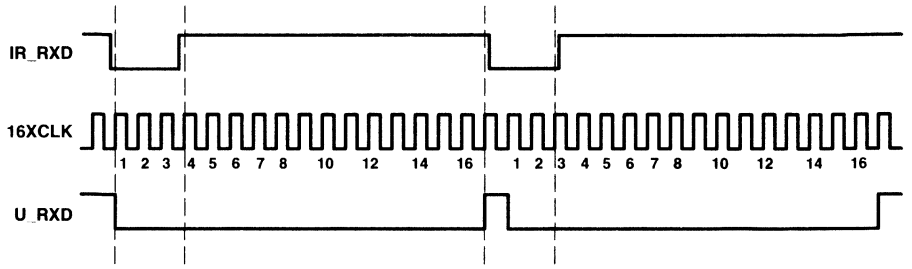


Figure 6. Timing Causing 1-clock Wide Pulse Between Consecutive Ones

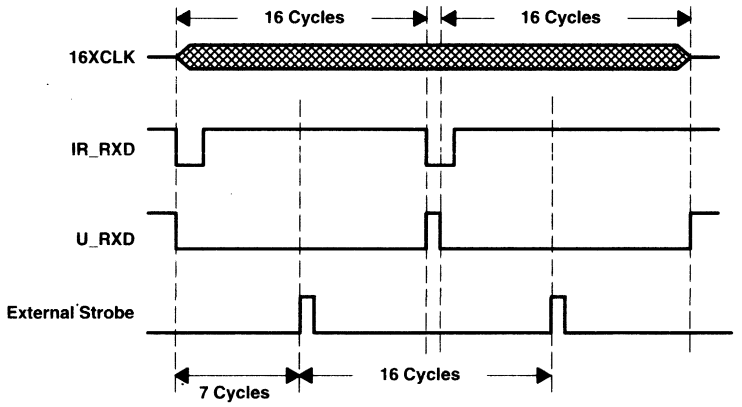


Figure 7. Recommended Strobing For Decoded Data

PRINCIPLES OF OPERATION

The TIR1000 can also decode positive pulses on IR_RXD. The timing is different, but the variation is invisible to the UART. Because the decoder works from the falling edge, it now recognizes a zero on the trailing edge of the pulse rather than on the leading edge. As long as the pulse width is fairly constant, as defined by the specification, the trailing edges should also be 16 clock cycles apart and data can readily be decoded. The zero appears on U_RXD after the pulse rather than at the start of it.

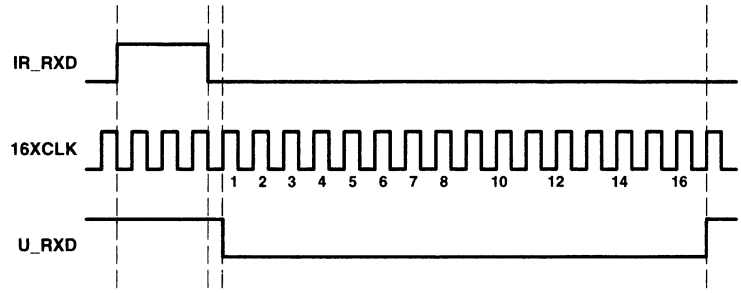


Figure 8. Positive IR_RXD Pulse Decode – Detailed View

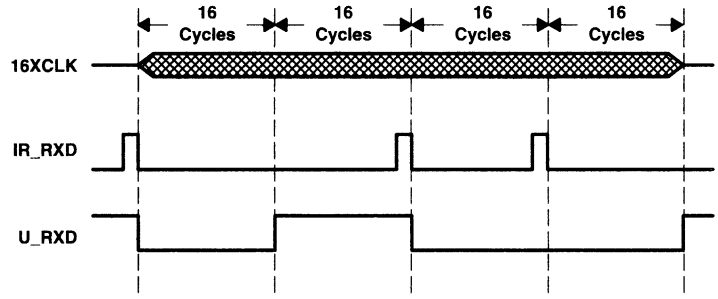
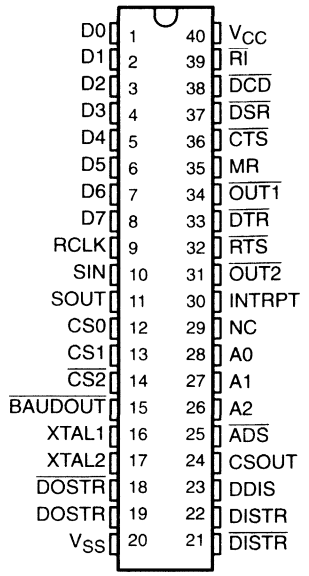


Figure 9. Positive IR_RXD Pulse Decode – Macro View

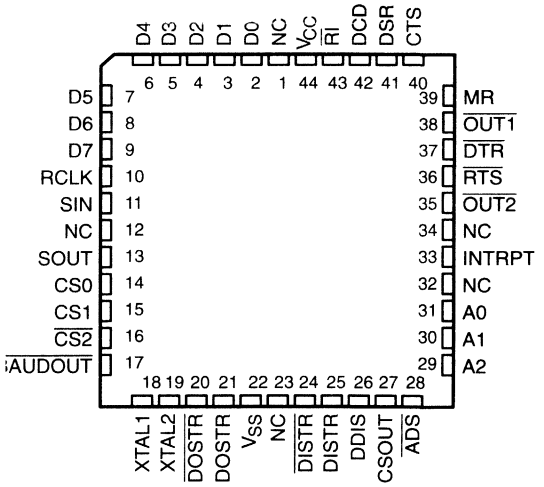
SLLS037B – MARCH 1988 – REVISED MARCH 1996

- Programmable Baud Rate Generator Allows Division of Any Input Reference Clock by 1 to ($2^{16}-1$) and Generates an Internal 16× Clock
- Full Double Buffering Eliminates the Need for Precise Synchronization
- Standard Asynchronous Communication Bits (Start, Stop, and Parity) Added or Deleted to or From the Serial Data Stream
- Independent Receiver Clock Input
- Transmit, Receive, Line Status, and Data Set Interrupts Independently Controlled
- Fully Programmable Serial Interface Characteristics:
  - 5-, 6-, 7-, or 8-Bit Characters
  - Even-, Odd-, or No-Parity Bit Generation and Detection
  - 1-, 1 1/2-, or 2-Stop Bit Generation
  - Baud Generation (dc to 256 Kbit/s)
- False Start Bit Detection
- Complete Status Reporting Capabilities
- 3-State TTL Drive Capabilities for Bidirectional Data Bus and Control Bus
- Line Break Generation and Detection
- Internal Diagnostic Capabilities:
  - Loopback Controls for Communications Link Fault Isolation
  - Break, Parity, Overrun, Framing Error Simulation
- Fully Prioritized Interrupt System Controls
- Modem Control Functions ($\overline{CTS}$, $\overline{RTS}$, $\overline{DSR}$, $\overline{DTR}$, $\overline{RI}$, and $\overline{DCD}$)
- Easily Interfaces to Most Popular Microprocessors
- Faster Plug-In Replacement for National Semiconductor NS16C450

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



IC – No internal connection

description

The TL16C450 is a CMOS version of an asynchronous communications element (ACE). It typically functions in a microcomputer system as a serial input/output interface.

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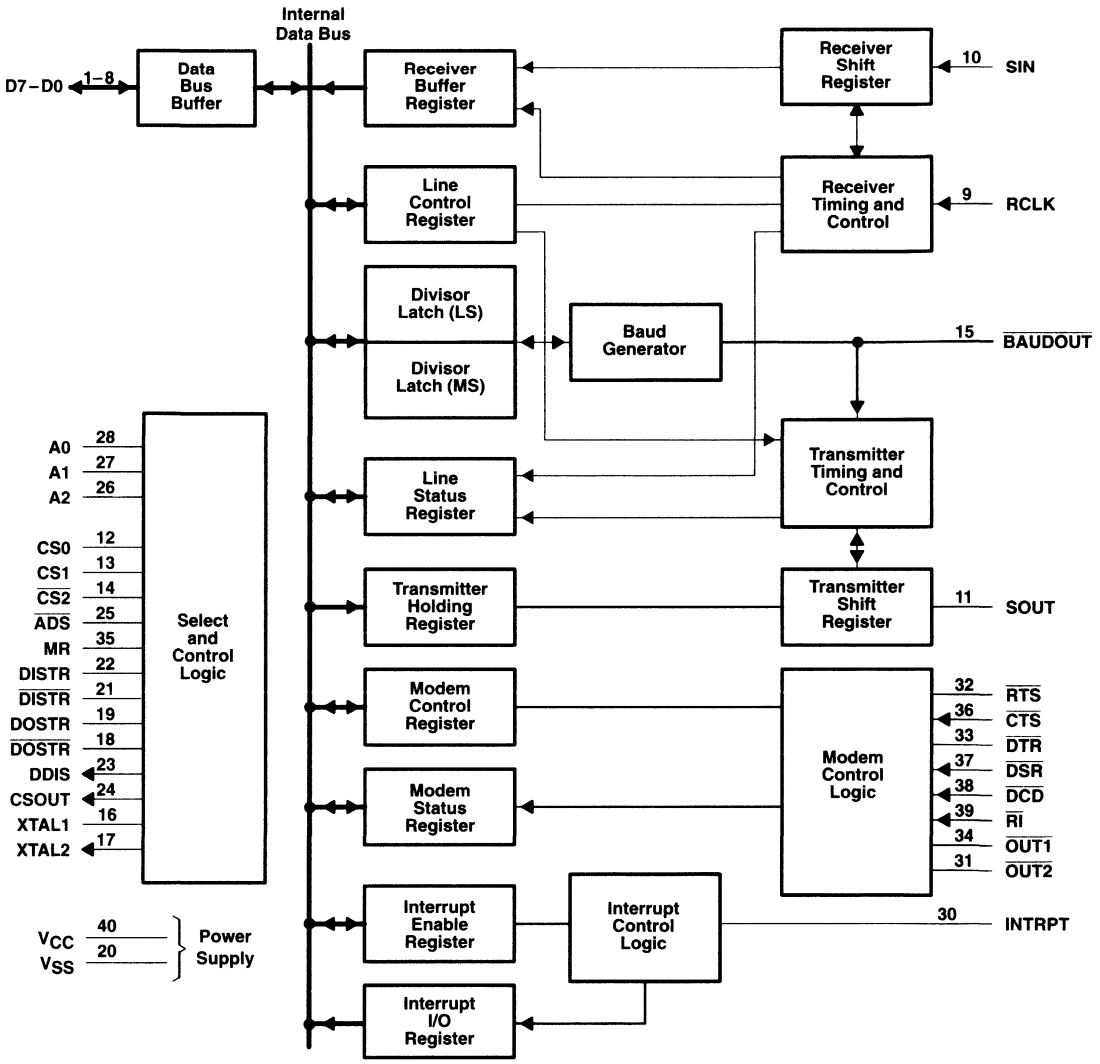
description (continued)

The TL16C450 performs serial-to-parallel conversion on data received from a peripheral device or modem and parallel-to-serial conversion on data received from its CPU. The CPU can read and report on the status of the ACE at any point in the ACE's operation. Reported status information includes the type of transfer operation in progress, the status of the operation, and any error conditions encountered.

The TL16C450 ACE includes a programmable, on-board, baud rate generator. This generator is capable of dividing a reference clock input by divisors from 1 to $(2^{16}-1)$ and producing a 16× clock for driving the internal transmitter logic. Provisions are included to use this 16× clock to drive the receiver logic. Also included in the ACE is a complete modem control capability and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link.

block diagram



Terminal numbers shown are for the N package.

Terminal Functions

TERMINAL NAME	TERMINAL NO.†	I/O	DESCRIPTION
A0 A1 A2	28 27 26	I	Register select. A0, A1, and A2 are three inputs used during read and write operations to select the ACE register to read from or write to. Refer to Table 1 for register addresses, also refer to the address strobe ($\overline{ADS}$) signal description.
$\overline{ADS}$	25	I	Address strobe. When $\overline{ADS}$ is active (low), the register select signals (A0, A1, and A2) and chip select signals (CS0, CS1, $\overline{CS2}$) drive the internal select logic directly; when high, the register select and chip select signals are held in the state they were in when the low-to-high transition of $\overline{ADS}$ occurred.
$\overline{BAUDOUT}$	15	O	Baud out. $\overline{BAUDOUT}$ is a16× clock signal for the transmitter section of the ACE. The clock rate is established by the reference oscillator frequency divided by a divisor specified by the baud generator divisor latches. $\overline{BAUDOUT}$ may also be used for the receiver section by tying this output to the RCLK input.
CS0 CS1 $\overline{CS2}$	12 13 14	I	Chip select. When CSx is active (high, high, and low respectively), the ACE is selected. Refer to the $\overline{ADS}$ signal description.
CSOUT	24	O	Chip select out. When CSOUT is high, it indicates that the ACE has been selected by the chip select inputs (CS0, CS1, and $\overline{CS2}$). CSOUT is low when the chip is deselected.
$\overline{CTS}$	36	I	Clear to send. $\overline{CTS}$ is a modem status signal. Its condition can be checked by reading bit 4 (CTS) of the modem status register. Bit 0 (DCTS) of the modem status register indicates that this signal has changed states since the last read from the modem status register. If the modem status interrupt is enabled when $\overline{CTS}$ changes state, an interrupt is generated.
D0 – D7	1 – 8	I/O	Data bus. D0 – D7 are 3-state data lines that provide a bidirectional path for data, control, and status information between the ACE and the CPU.
$\overline{DCD}$	38	I	Data carrier detect. $\overline{DCD}$ is a modem status signal. Its condition can be checked by reading bit 7 (DCD) of the modem status register. Bit 3 (DDCD) of the modem status register indicates that this signal has changed states since the last read from the modem status register. If the modem status interrupt is enabled when the $\overline{DCD}$ changes state, an interrupt is generated.
DDIS	23	O	Driver disable. DDIS is active (high) when the CPU is not reading data. When active, this output can disable an external transceiver.
DISTR $\overline{DISTR}$	22 21	I	Data input strobes. When either DISTR or $\overline{DISTR}$ is active (high or low respectively) while the ACE is selected, the CPU is allowed to read status information or data from a selected ACE register. Only one of these inputs is required for the transfer of data during a read operation. The other input should be tied in its inactive state (i.e., DISTR tied low or $\overline{DISTR}$ tied high).
DOSTR $\overline{DOSTR}$	19 18	I	Data output strobes. When either DOSTR or $\overline{DOSTR}$ is active (high or low respectively), while the ACE is selected, the CPU is allowed to write control words or data into a selected ACE register. Only one of these inputs is required to transfer data during a write operation. The other input should be tied in its inactive state (i.e., DOSTR tied low or $\overline{DOSTR}$ tied high).
$\overline{DSR}$	37	I	Data set ready. $\overline{DSR}$ is a modem status signal. Its condition can be checked by reading bit 5 (DSR) of the modem status register. Bit 1 (DDSR) of the modem status register indicates that this signal has changed state since the last read from the modem status register. If the modem status interrupt is enabled when the $\overline{DSR}$ changes state, an interrupt is generated.
$\overline{DTR}$	33	O	Data terminal ready. When active (low), $\overline{DTR}$ informs a modem or data set that the ACE is ready to establish communication. $\overline{DTR}$ is placed in the active state by setting the DTR bit of the modem control register to a high level. $\overline{DTR}$ is placed in the inactive state either as a result of a master reset or during loop mode operation or clearing bit 0 (DTR) of the modem control register.
INTRPT	30	O	Interrupt. When active (high), INTRPT informs the CPU that the ACE has an interrupt to be serviced. The four conditions that cause an interrupt are: a receiver error, received data is available, the transmitter holding register is empty, or an enabled modem status interrupt. The INTRPT output is reset (inactivated) either when the interrupt is serviced or as a result of a master reset.
MR	35	I	Master reset. When active (high), MR clears most ACE registers and sets the state of various output signals. Refer to Table 2 for ACE reset functions.

† Terminal numbers shown are for the N package.

Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO.†	I/O	DESCRIPTION
$\overline{OUT1}$ $\overline{OUT2}$	34 31	O	Outputs 1 and 2. $\overline{OUT1}$ and $\overline{OUT2}$ are user-designated output terminals that are set to their active states by setting their respective modem control register bits (OUT1 and OUT2) high. $\overline{OUT1}$ and $\overline{OUT2}$ are set to their inactive (high) states as a result of master reset or during loop mode operations or by clearing bit 2 (OUT1) or bit 3 (OUT2) of the MCR.
RCLK	9	I	Receiver clock. RCLK is the 16× baud rate clock for the receiver section of the ACE.
$\overline{RI}$	39	I	Ring indicator. $\overline{RI}$ is a modem status signal. Its condition can be checked by reading bit 6 (RI) of the modem status register. Bit 2 (TERI) of the modem status register indicates that the $\overline{RI}$ input has transitioned from a low to a high state since the last read from the modem status register. If the modem status interrupt is enabled when this transition occurs, an interrupt is generated.
$\overline{RTS}$	32	O	Request to send. When active, $\overline{RTS}$ informs the modem or data set that the ACE is ready to transmit data. $\overline{RTS}$ is set to its active state by setting the RTS modem control register bit and is set to its inactive (high) state either as a result of a master reset or during loop mode operations or by clearing bit 1 (RTS) of the MCR.
SIN	10	I	Serial input. SIN is the serial data input from a connected communications device.
SOUT	11	O	Serial output. SOUT is the composite serial data output to a connected communication device. SOUT is set to the marking (set) state as a result of MR.
V_{CC}	40		5-V supply voltage
V_{SS}	20		Supply common
XTAL1 XTAL2	16 17	I/O	External clock. XTAL1 and XTAL2 connect the ACE to the main timing reference (clock or crystal).

† Terminal numbers shown are for the N package.

absolute maximum ratings over free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.5 V to 7 V
Input voltage range at any input, V_I . . . . . −0.5 V to 7 V
Output voltage range, V_O . . . . . −0.5 V to 7 V
Continuous total power dissipation at (or below) 70°C free-air temperature: FN package . . . . . 1100 mW
N package . . . . . 800 mW
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Case temperature for 10 seconds, T_C: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2		V_{CC}	V
Low-level input voltage, V_{IL}	−0.5		0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}‡	HIgh-level output voltage	I_{OH} = –1 mA	2.4			V
V_{OL}‡	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
I_{lkg}	Input leakage current	V_{CC} = 5.25 V, V_{SS} = 0, V_I = 0 to 5.25 V, All other terminals floating			±10	µA
I_{OZ}	High-impedance output current	V_{CC} = 5.25 V, V_{SS} = 0, V_O = 0 V to 5.25 V, Chip selected, write mode,or chip deselected			±20	µA
I_{CC}	Supply current	V_{CC} = 5.25 V, T_A = 25°C, SIN, DSR, DCD, CTS, and RI at 2 V, All other inputs at 0.8 V, Baud rate = 50 kbits/s, XTAL1 at 4 MHz, No load on outputs			10	mA
C_{XTAL1}	Clock input capacitance	V_{CC} = 0, V_{SS} = 0, f = 1 MHz, T_A = 25°C, All other terminals grounded		15	20	pF
C_{XTAL2}	Clock output capacitance			20	30	pF
C_i	Input capacitance			6	10	pF
C_o	Output capacitance			10	20	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ These parameters apply for all outputs except XTAL2.

system timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		FIGURE	MIN	MAX	UNIT
t_{cR}	Cycle time, read ($t_{w7} + t_{d8} + t_{d9}$)		175		ns
t_{cW}	Cycle time, write ($t_{w6} + t_{d5} + t_{d6}$)		175		ns
t_{w5}	Pulse duration, $\overline{ADS}$ low	2,3	15		ns
t_{w6}	Pulse duration, write strobe	2	80		ns
t_{w7}	Pulse duration, read strobe	3	80		ns
t_{wMR}	Pulse duration, master reset		1000		ns
t_{su1}	Setup time, address valid before $\overline{ADS}\uparrow$	2,3	15		ns
t_{su2}	Setup time, CS valid before $\overline{ADS}\uparrow$	2,3	15		ns
t_{su3}	Setup time, data valid before $\overline{WR1}\downarrow$ or WR2$\uparrow$	2	15		ns
t_{h1}	Hold time, address low after $\overline{ADS}\uparrow$	2,3	0		ns
t_{h2}	Hold time, CS valid after $\overline{ADS}\uparrow$	2,3	0		ns
t_{h3}	Hold time, CS valid after $\overline{WR1}\uparrow$ or WR2$\downarrow$	2	20		ns
t_{h4}§	Hold time, address valid after $\overline{WR1}\uparrow$ or WR2$\downarrow$	2	20		ns
t_{h5}	Hold time, data valid after $\overline{WR1}\uparrow$ or WR2$\downarrow$	2	15		ns
t_{h6}	Hold time, CS valid after $\overline{RD1}\uparrow$ or RD2$\downarrow$	3	20		ns
t_{h7}§	Hold time, address valid after $\overline{RD1}\uparrow$ or RD2$\downarrow$	3	20		ns
t_{d4}§	Delay time, CS valid before $\overline{WR1}\downarrow$ or WR2$\uparrow$	2	15		ns
t_{d5}§	Delay time, address valid before $\overline{WR1}\downarrow$ or WR2$\uparrow$	2	15		ns
t_{d6}	Delay time, write cycle, $\overline{WR1}\uparrow$ or WR2$\downarrow$ to $\overline{ADS}\downarrow$	2	80		ns
t_{d7}§	Delay time, CS valid to $\overline{RD1}\downarrow$ or RD2$\uparrow$	3	15		ns
t_{d8}§	Delay time, address valid to $\overline{RD1}\downarrow$ or RD2$\uparrow$	3	15		ns
t_{d9}	Delay time, read cycle, $\overline{RD1}\uparrow$ or RD2$\downarrow$ to $\overline{ADS}\downarrow$	3	80		ns

§ Only applies when ADS is low.

system switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{w1}	Pulse duration, clock high	1	f = 9 MHz maximum	50		ns
t_{w2}	Pulse duration, clock low	1	f = 9 MHz maximum	50		ns
t_{d3}	Delay time, select to CS output	2, 3†	C_L = 100 pF		70	ns
t_{d10}	Delay time, $\overline{RD1}\downarrow$ or RD2↑ to data valid	3	C_L = 100 pF		60	ns
t_{d11}	Delay time, $\overline{RD1}\uparrow$ or RD2↓ to floating data	3	C_L = 100 pF	0	60	ns
$t_{dis(R)}$	Disable time, $\overline{RD1}\downarrow\uparrow$ or RD2↑↓ to DDIS↑↓	3	C_L = 100 pF		60	ns

† Only applies when $\overline{ADS}$ is low.

baud generator switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{w3}	Pulse duration, $\overline{BAUDOUT}$ low	1	f = 6.25 MHz, CLK ÷ 1, C_L = 100 pF	80		ns
t_{w4}	Pulse duration, $\overline{BAUDOUT}$ high	1	f = 6.25 MHz, CLK ÷ 1, C_L = 100 pF	80		ns
t_{d1}	Delay time, XIN↑ to $\overline{BAUDOUT}\uparrow$	1	C_L = 100 pF		125	ns
t_{d2}	Delay time, XIN↑↓ to $\overline{BAUDOUT}\downarrow$	1	C_L = 100 pF		125	ns

receiver switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d12}	Delay time, RCLK to sample clock	4			100	ns
t_{d13}	Delay time, stop to set RCV error interrupt or read RDR to LSI interrupt or stop to $\overline{RXRDY}\downarrow$	4		1	1	RCLK cycles
t_{d14}	Delay time, read RBR/LSR to reset interrupt	4	C_L = 100 pF		140	ns

transmitter switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d15}	Delay time, INTRPT to transmit start	5		8	24	baudout cycles
t_{d16}	Delay time, start to interrupt	5		8	8	baudout cycles
t_{d17}	Delay time, WR THR to reset interrupt	5	C_L = 100 pF		140	ns
t_{d18}	Delay time, initial write to interrupt (THRE)	5		16	32	baudout cycles
t_{d19}	Delay time, read IIR to reset interrupt (THRE)	5	C_L = 100 pF		140	ns

modem control switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d20}	Delay time, WR MCR to output	6	C_L = 100 pF		100	ns
t_{d21}	Delay time, modem interrupt to set interrupt	6	C_L = 100 pF		170	ns
t_{d22}	Delay time, RD MSR to reset interrupt	6	C_L = 100 pF		140	ns

PARAMETER MEASUREMENT INFORMATION

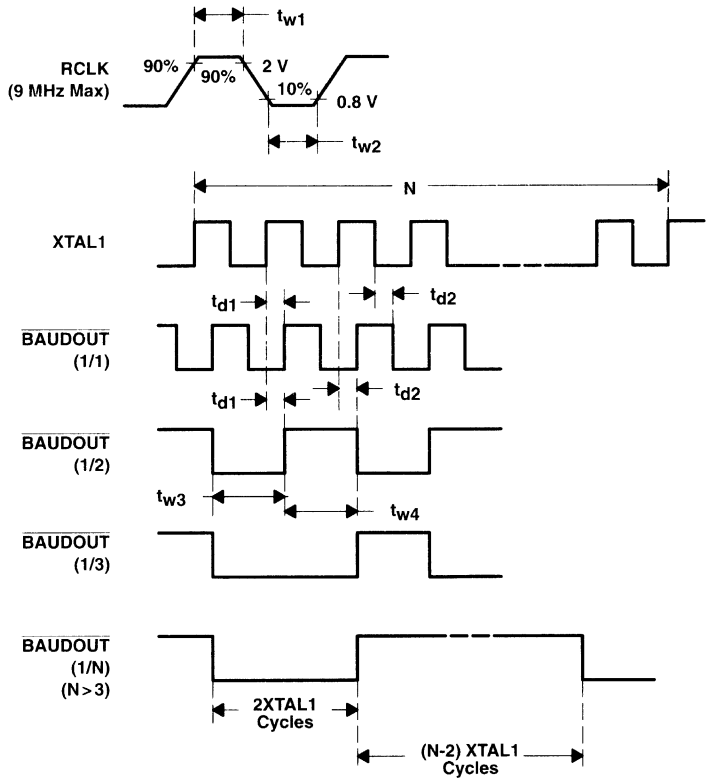
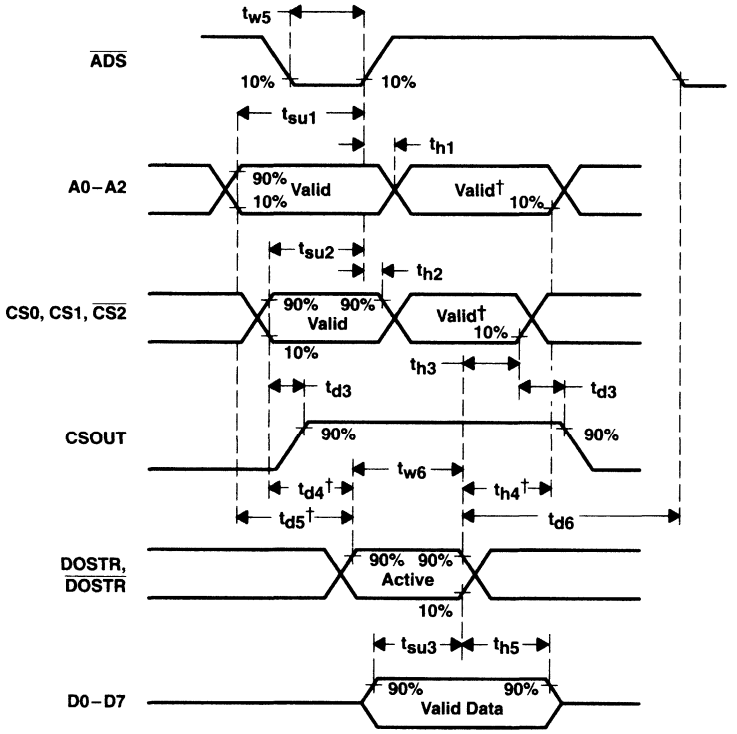


Figure 1. Baud Generator Timing Waveforms

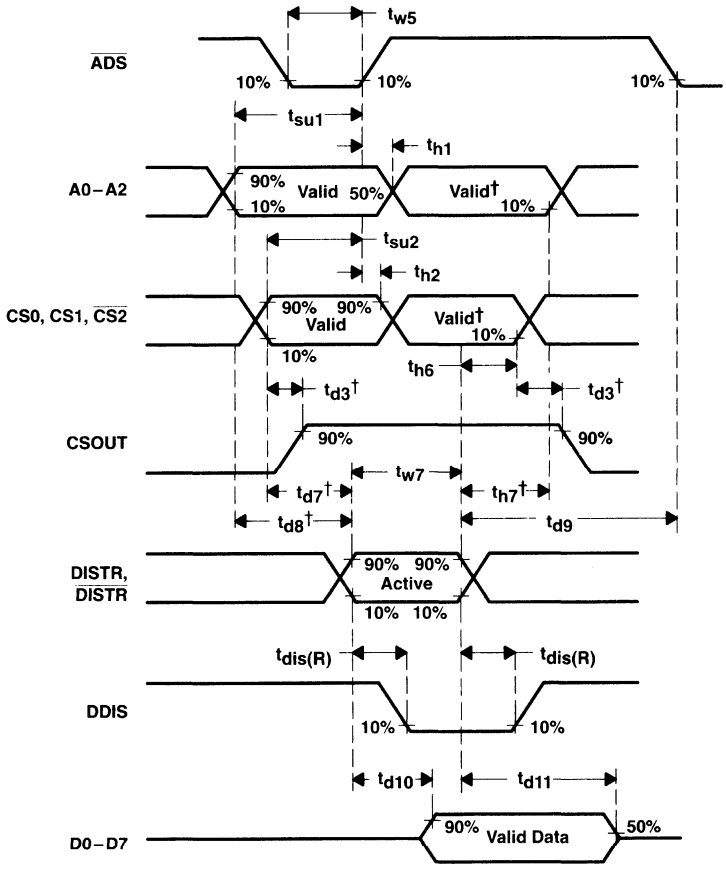
PARAMETER MEASUREMENT INFORMATION



† Applicable only when $\overline{ADS}$ is tied low.

Figure 2. Write Cycle Timing Waveforms

PARAMETER MEASUREMENT INFORMATION



† Applicable only when $\overline{ADS}$ is tied low.

Figure 3. Read Cycle Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

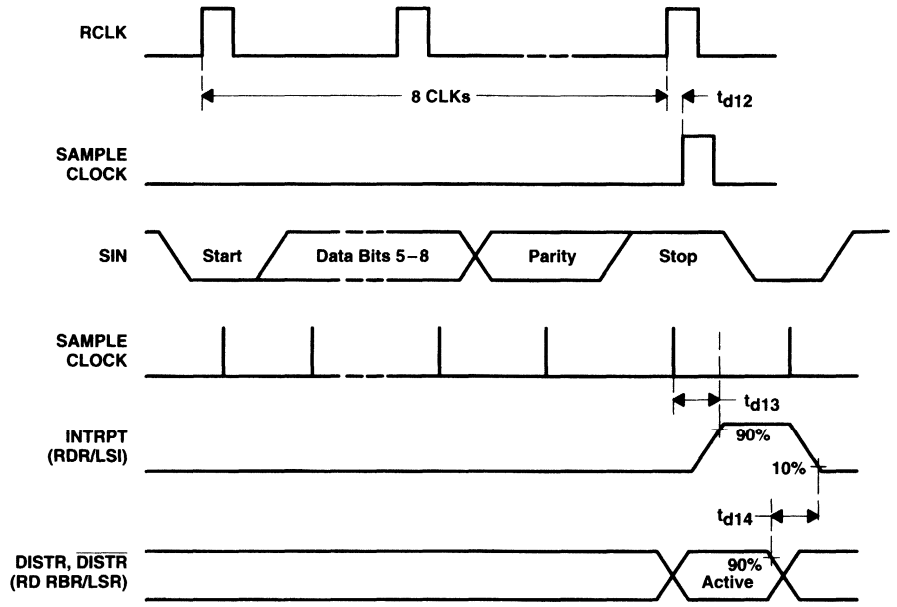


Figure 4. Receiver Timing Waveforms

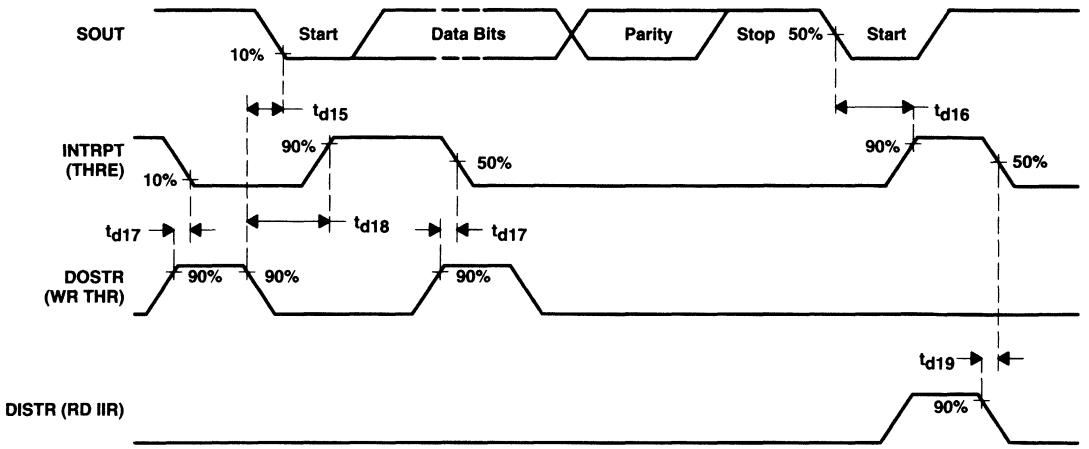


Figure 5. Transmitter Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

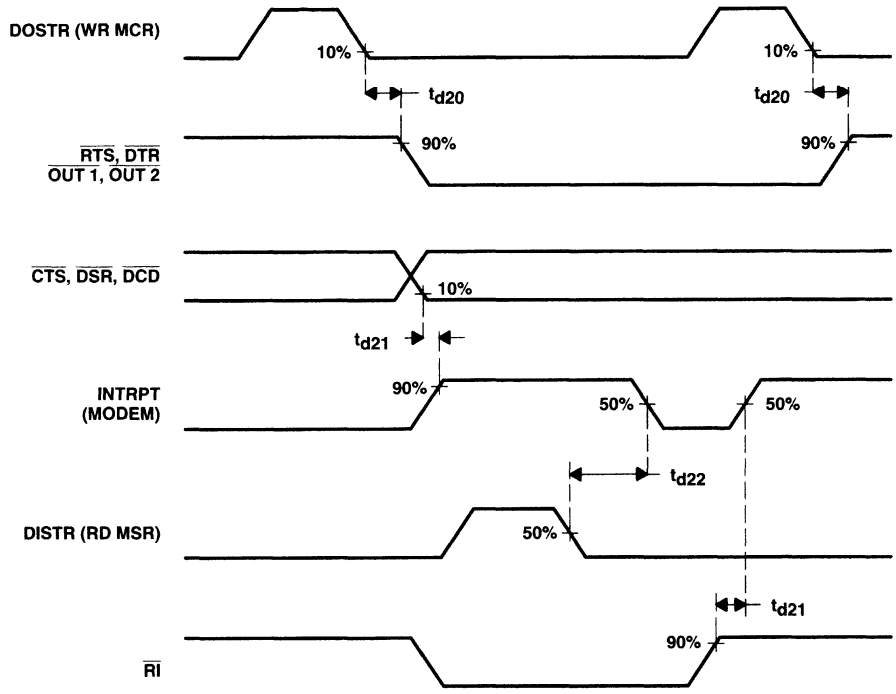


Figure 6. Modem Control Timing Waveforms

APPLICATION INFORMATION

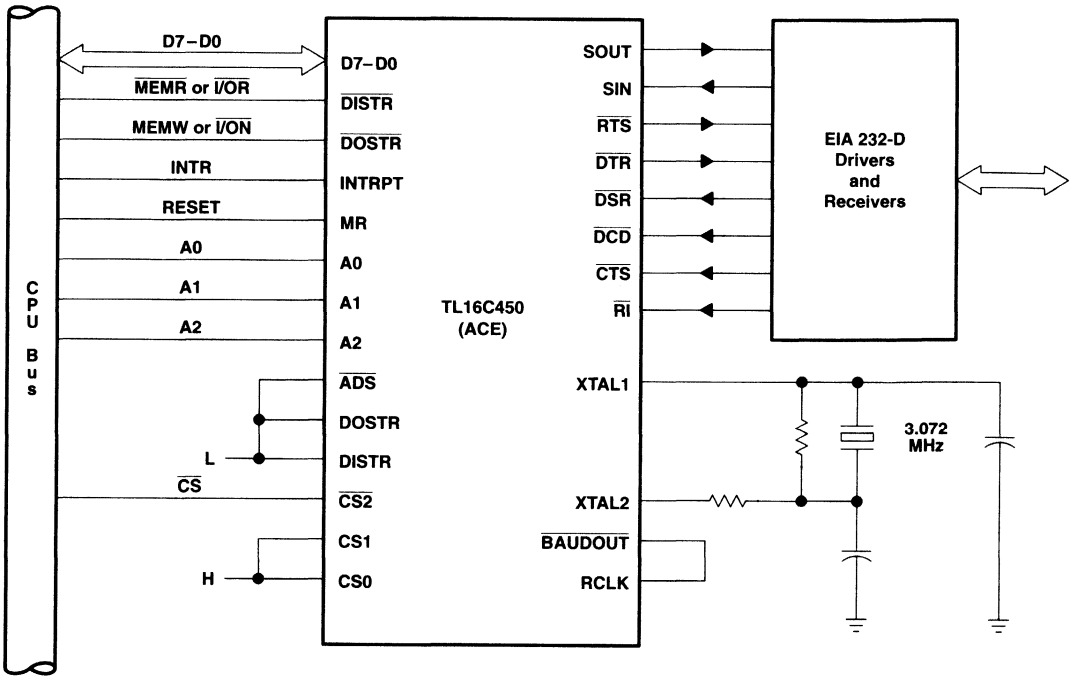


Figure 7. Basic TL16C450 Configuration

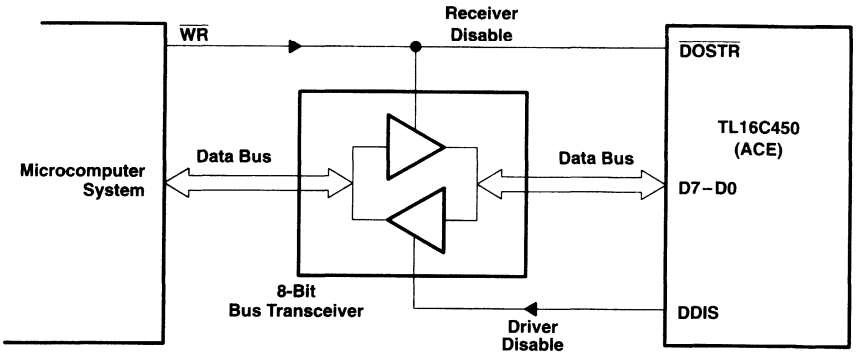


Figure 8. Typical Interface for a High-Capacity Data Bus

APPLICATION INFORMATION

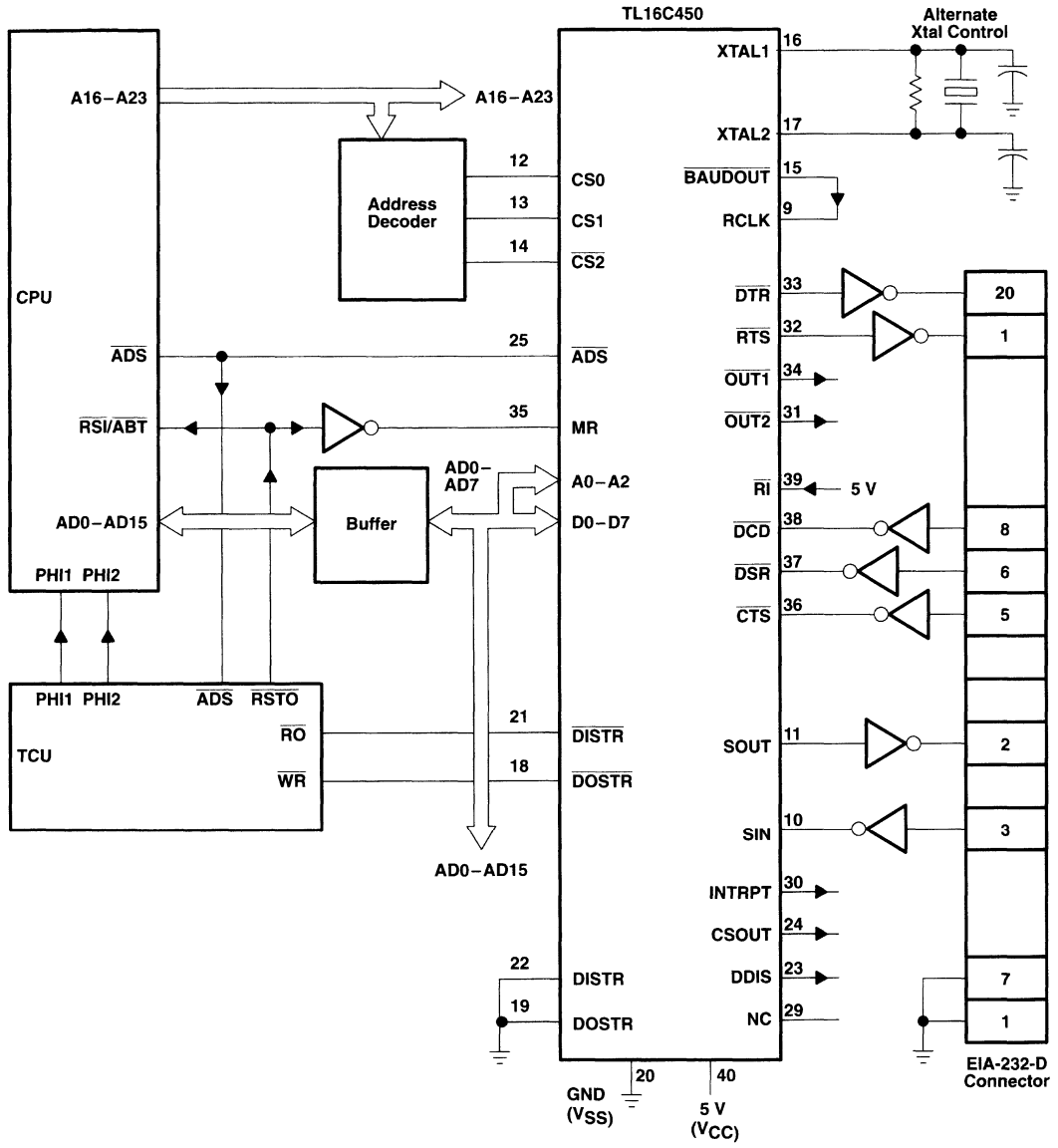


Figure 9. Typical TL16C450 Connection to a CPU

PRINCIPLES OF OPERATION

Table 1. Register Selection

DLAB†	A2	A1	A0	REGISTER
0	L	L	L	Receiver buffer (read), transmitter holding register (write)
0	L	L	H	Interrupt enable
X	L	H	L	Interrupt identification (read only)
X	L	H	H	Line control
X	H	L	L	Modem control
X	H	L	H	Line status
X	H	H	L	Modem status
X	H	H	H	Scratch
1	L	L	L	Divisor latch (LSB)
1	L	L	H	Divisor latch (MSB)

† The divisor latch access bit (DLAB) is the most significant bit of the line control register. The DLAB signal is controlled by writing to this bit location (see Table 3).

Table 2. ACE Reset Functions

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt enable register	Master reset	All bits low (0–3 forced and 4–7 permanent)
Interrupt identification register	Master reset	Bit 0 is high, bits 1 and 2 are low, and bits 3 –7 are permanently low
Line control register		All bits low
Modem control register	Master reset	All bits low
Line status register	Master reset	Bits 5 and 6 are high, all other bits are low
Modem status register	Master reset	Bits 0–3 are low, bits 4–7 are input signals
SOUT	Master reset	High
INTRPT (receiver error flag)	Read LSR/MR	Low
INTRPT (received data available)	Read RBR/MR	Low
INTRPT (transmitter holding register empty)	Read IIR/Write THR/MR	Low
INTRPT (modem status changes)	Read MSR/MR	Low
$\overline{OUT2}$	Master reset	High
$\overline{RTS}$	Master reset	High
$\overline{DTR}$	Master reset	High
$\overline{OUT1}$	Master reset	High
Scratch register	Master reset	No effect
Divisor latch (LSB and MSB) register	Master reset	No effect
Receiver buffer register	Master reset	No effect
Transmitter holding register	Master reset	No effect

PRINCIPLES OF OPERATION

accessible registers

The system programmer, using the CPU, has access to and control over any of the ACE registers that are summarized in Table 3. These registers control ACE operations, receive data, and transmit data. Descriptions of these registers follow Table 3.

Table 3. Summary of Accessible Registers

Bit No.	REGISTER ADDRESS										
	O DLAB = 0	O DLAB = 0	1 DLAB = 0	2	3	4	5	6	7	O DLAB = 1	1 DLAB = 0
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register IER	Interrupt Ident. Register (Read Only)	Line Control Register LCR	Modem Control Register	Line Status Register	Modem Status Register	Scratch Register	Divisor Latch (LSB)	Latch (MSB)
	RBR	THR	IER	IIR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Data Bit 0*	Data Bit 0	Enable Received Data Available Interrupt (ERBF)	"0" If Interrupt Pending	Word Length Select Bit 0 (WLSO)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBE)	Interrupt ID Bit (0)	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable Modem Status Interrupt (EDSSI)	0	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Data Carrier Detect (DDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

*Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

PRINCIPLES OF OPERATION

interrupt enable register (IER)

The IER enables each of the four types of interrupts (refer to Table 4) and the INTRPT output signal in response to an interrupt generation. By clearing bits 0 – 3, the IER can also disable the interrupt system. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bit 0: This bit, when set, enables the received data available interrupt.
- Bit 1: This bit, when set, enables the THRE interrupt.
- Bit 2: This bit, when set, enables the receiver line status interrupt.
- Bit 3: This bit, when set, enables the modem status interrupt.
- Bits 4 – 7: These bits in the IER are not used and are always cleared.

interrupt identification register (IIR)

The ACE has an on-chip interrupt generation and prioritization capability that permits a flexible interface with most microprocessors.

The ACE provides four prioritized levels of interrupts:

- Priority 1 – Receiver line status (highest priority)
- Priority 2 – Receiver data ready or receiver character time out
- Priority 3 – Transmitter holding register empty
- Priority 4 – Modem status (lowest priority)

When an interrupt is generated, the IIR indicates that an interrupt is pending and the type of interrupt in its three least significant bits (bits 0, 1, and 2). The contents of this register are summarized in Table 3 and described in Table 4.

- Bit 0: This bit can be used either in a hardwire prioritized or polled interrupt system. When bit 0 is cleared, an interrupt is pending. When bit 0 is set, no interrupt is pending.
- Bits 1 and 2: These two bits identify the highest priority interrupt pending as indicated in Table 4.
- Bits 3 – 7: These bits in the IIR are not used and are always clear.

PRINCIPLES OF OPERATION

interrupt identification register (IIR) (continued)

Table 4. Interrupt Control Functions

INTERRUPT IDENTIFICATION REGISTER			PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET METHOD
BIT 2	BIT 1	BIT 0				
0	0	1	None	None	None	–
1	1	0	1	Receiver line status	Overrun error, parity error, framing error or break interrupt	Reading the line status register
1	0	0	2	Received data available	Receiver data available	Reading the receiver buffer Buffer register
0	1	0	3	Transmitter holding register empty	Transmitter holding register empty	Reading the interrupt identification register (if source of interrupt) or writing into the transmitter holding register
0	0	0	4	Modem status	Clear to send, data set ready, ring indicator, or data carrier detect	Reading the modem status register

line control register (LCR)

The system programmer controls the format of the asynchronous data communication exchange through the LCR. In addition, the programmer is able to retrieve, inspect, and modify the contents of the LCR; this eliminates the need for separate storage of the line characteristics in system memory. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. These bits are encoded as shown in Table 5.

Table 5. Serial Character Word Length

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

- Bit 2: This bit specifies either one, one and one-half, or two stop bits in each transmitted character. When bit 2 is cleared, one stop bit is generated in the data. When bit 2 is set, the number of stop bits generated is dependent on the word length selected with bits 0 and 1. The receiver checks the first stop bit only, regardless of the number of stop bits selected. The number of stop bits generated, in relation to word length and bit 2, is shown in Table 6.

PRINCIPLES OF OPERATION

line control register (LCR) (continued)

Table 6. Number of Stop Bits Generated

Bit 2	Word Length Selected by Bits 1 and 2	Number of Stop Bits Generated
0	Any word length	1
1	5 bits	1 1/2
1	6 bits	2
1	7 bits	2
1	8 bits	2

- Bit 3: This bit is the parity enable bit. When bit 3 is set, a parity bit is generated in transmitted data between the last data word bit and the first stop bit. In received data, if bit 3 is set, parity is checked. When bit 3 is cleared, no parity is generated or checked.
- Bit 4: This bit is the even parity select bit. When parity is enabled (bit 3 is set) and bit 4 is set, even parity (an even number of logic 1s is in the data and parity bits) is selected. When parity is enabled (bit 3 is set) and bit 4 is clear, odd parity (an odd number of logic 1s) is selected.
- Bit 5: This is the stick parity bit. When bits 3, 4, and 5 are set, the parity bit is transmitted and checked as cleared. When bits 3 and 5 are set and bit 4 is cleared, the parity bit is transmitted and checked as set.
- Bit 6: This bit is the break control bit. Bit 6 is set to force a break condition, i.e, a condition where the serial output terminal (SOUT) is forced to the spacing (cleared) state. When bit 6 is cleared, the break condition is disabled. The break condition has no affect on the transmitter logic, it only affects the serial output.
- Bit 7: This bit is the divisor latch access bit (DLAB). Bit 7 must be set to access the divisor latches of the baud generator during a read or write. Bit 7 must be cleared during a read or write to access the receiver buffer, the THR, or the IER.

line status register (LSR)†

The LSR provides information to the CPU concerning the status of data transfers. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bit 0: This bit is the data ready (DR) indicator for the receiver. Bit 0 is set whenever a complete incoming character has been received and transferred into the RBR and is cleared by reading the RBR.
- Bit 1‡: This bit is the overrun error (OE) indicator. When bit 1 is set, it indicates that before the character in the RBR was read, it was overwritten by the next character transferred into the register. The OE indicator is cleared every time the CPU reads the contents of the LSR.
- Bit 2‡: This bit is the parity error (PE) indicator. When bit 2 is set, it indicates that the parity of the received data character does not match the parity selected in the LCR (bit 4). The PE bit is cleared every time the CPU reads the contents of the LSR.
- Bit 3‡: This bit is the framing error (FE) indicator. When bit 3 is set, it indicates that the received character does not have a valid (set) stop bit. The FE bit is cleared every time the CPU reads the contents of the LSR.
- Bit4‡: This bit is the break interrupt (BI) indicator. When bit 4 is set, it indicates that the received data input was held clear for longer than a full-word transmission time. A full-word transmission time is defined as the total time of the start, data, parity, and stop bits. The BI bit is cleared every time the CPU reads the contents of the LSR.

† The line status register is intended for read operations only; writing to this register is not recommended outside of a factory testing environment.
‡ Bits 1 through 4 are the error conditions that produce a receiver line-status interrupt.

PRINCIPLES OF OPERATION

line status register (LSR)† (continued)

- Bit 5: This bit is the THRE indicator. Bit 5 is set when the THR is empty, indicating that the ACE is ready to accept a new character. If the THRE interrupt is enabled when the THRE bit is set, then an interrupt is generated. THRE is set when the contents of the THR are transferred to the transmitted shift register. This bit is cleared concurrent with the loading of the THR by the CPU.
- Bit 6: This bit is the transmitter empty (TEMT) indicator. Bit 6 is set when the THR and the transmitter shift register are both empty. When either the THR or the transmitter shift register contains a data character, the TEMT bit is cleared.
- Bit 7: This bit is always clear.

modem control register (MCR)

The MCR is an 8-bit register that controls an interface with a modem, data set, or peripheral device that is emulating a modem. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bit 0: This bit (DTR) controls the data terminal ready ($\overline{DTR}$) output. Setting bit 0 forces the $\overline{DTR}$ output to its active state (low). When bit 0 is clear, $\overline{DTR}$ goes high.
- Bit 1: This bit (RTS) controls the request to send ($\overline{RTS}$) output in a manner identical to bit 0's control over the $\overline{DTR}$ output.
- Bit 2: This bit (OUT1) controls the output 1 ($\overline{OUT1}$) signal, a user designated output signal, in a manner identical to bit 0's control over the $\overline{DTR}$ output.
- Bit 3: This bit (OUT2) controls the output 2 ($\overline{OUT2}$) signal, a user designated output signal, in a manner identical to bit 0's control over the $\overline{DTR}$ output.
- Bit 4: This bit provides a local loopback feature for diagnostic testing of the ACE. When bit 4 is set, the following occurs:

  1. The SOUT is asserted high.
  2. The SIN is disconnected.
  3. The output of the transmitter shift register is looped back into the RSR input.
  4. The four modem control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$) are disconnected.
  5. The four modem control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT1}$, and $\overline{OUT2}$) are internally connected to the four modem control inputs.
  6. The four modem control output terminals are forced to their inactive states (high).

  In the diagnostic mode, data that is transmitted is immediately received. This allows the processor to verify the transmit and receive data paths to the ACE. The receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational but the modem control interrupt sources are now the lower four bits of the MCR instead of the four modem control inputs. All interrupts are still controlled by the IER.

- Bits 5 through 7: These bits are clear.

† The line status register is intended for read operations only; writing to this register is not recommended outside of a factory testing environment.

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modem status register (MSR)

The MSR is an 8-bit register that provides information about the current state of the control lines from the modem, data set, or peripheral device to the CPU. Additionally, four bits of this register provides change information; when a control input from the modem changes state the appropriate bit is set. All four bits are cleared when the CPU reads the MSR. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bit 0: This bit is the delta clear to send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input has changed states since the last time it was read by the CPU. When this bit is set and the modem status interrupt is enabled, a modem status interrupt is generated.
- Bit 1: This bit is the delta data set ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input has changed states since the last time it was read by the CPU. When this bit is set and the modem status interrupt is enabled, a modem status interrupt is generated.
- Bit 2: This bit is the trailing edge of ring indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from a low to a high state. When this bit is set and the modem status interrupt is enabled, a modem status interrupt is generated.
- Bit 3: This bit is the delta data carrier detect (DDCD) indicator. Bit 3 indicates that the $\overline{DCD}$ input to the chip has changed state since the last time it was read by the CPU. When this bit is set and the modem status interrupt is enabled, a modem status interrupt is generated.
- Bit 4: This bit is the complement of the clear to send ($\overline{CTS}$) input. When bit 4 (loop) of the MCR is set, this bit is equivalent to the MCR bit 1 (RTS).
- Bit 5: This bit is the complement of the data set ready ($\overline{DSR}$) input. When bit 4 (loop) of the MCR is set, this bit is equivalent to the MCR bit 0 (DTR).
- Bit 6: This bit is the complement of the ring indicator ($\overline{RI}$) input. When bit 4 (loop) of the MCR is set, this bit is equivalent to the MCRs bit 2 (OUT1).
- Bit 7: This bit is the complement of the data carrier detect ($\overline{DCD}$) input. When bit 4 (loop) of the MCR is set, this bit is equivalent to the MCRs bit 3 (OUT2).

programmable baud generator

The ACE contains a programmable baud generator that takes a clock input in the range between dc and 9 MHz and divides it by a divisor in the range between 1 and $(2^{16}-1)$. The output frequency of the baud generator is sixteen times (16×) the baud rate. The formula for the divisor is:

$$\text{divisor \#} = \text{XTAL1 frequency input} \div (\text{desired baud rate} \times 16)$$

Two 8-bit registers, called divisor latches, store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization of the ACE in order to ensure desired operation of the baud generator. When either of the divisor latches is loaded, a 16-bit baud counter is also loaded to prevent long counts on initial load.

Tables 7 and 8 illustrate the use of the baud generator with crystal frequencies of 1.8432 MHz and 3.072 MHz, respectively. For baud rates of 38.4 kilobits per second and below, the error obtained is very small. The accuracy of the selected baud rate is dependent on the selected crystal frequency.

Refer to Figure 10 for examples of typical clock circuits.

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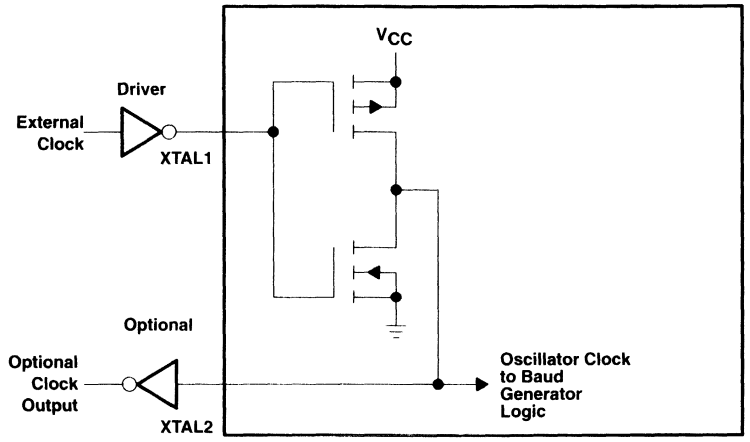
Table 7. Baud Rates Using a 1.8432-MHz Crystal

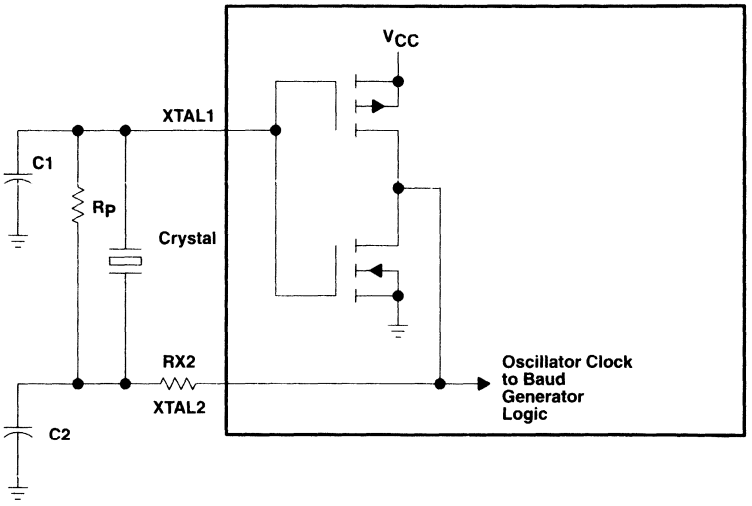
DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16× CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
1800	64	
2000	58	0.69
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19200	6	
38400	3	
56000	2	2.86

Table 8. Baud Rates Using a 3.072-MHz Crystal

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16× CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	
75	2560	
110	1745	0.026
134.5	1428	0.034
150	1280	
300	640	
600	320	
1200	160	
1800	107	0.312
2000	96	
2400	80	
3600	53	0.628
4800	40	
7200	27	1.23
9600	20	
19200	10	
38400	5	

PRINCIPLES OF OPERATION





TYPICAL CRYSTAL OSCILLATOR NETWORK

CRYSTAL	RP	RX2	C1	C2
3.1 MHz	1 MΩ	1.5 kΩ	10–30 pF	40–60 pF
1.8 MHz	1 MΩ	1.5 kΩ	10–30 pF	40–60 pF

Figure 10. Typical Clock Circuits

PRINCIPLES OF OPERATION

receiver buffer register (RBR)

The ACE receiver section consists of a receiver shift register and a RBR. Timing is supplied by the 16× receiver clock (RCLK). Receiver section control is a function of the ACE line control register.

The ACE receiver shift register receives serial data from the serial input (SIN) terminal. The receiver shift register then converts the data to a parallel form and loads it into the RBR. When a character is placed in the RBR and the received data available interrupt is enabled, an interrupt is generated. This interrupt is cleared when the data is read out of the RBR.

scratch register

The scratch register is an 8-bit register that is intended for programmer use as a scratchpad, in the sense that it temporarily holds programmer data without affecting any other ACE operation.

transmitter holding register (THR)

The ACE transmitter section consists of a THR and a transmitter shift register. Timing is supplied by the baud out ($\overline{\text{BAUDOUT}}$) clock signal. Transmitter section control is a function of the ACE line control register.

The ACE THR receives data from the internal data bus and, when the shift register is idle, moves it into the transmitter shift register. The transmitter shift register serializes the data and outputs it at the serial output (SOUT). If the THR is empty and the transmitter holding register empty (THRE) interrupt is enabled, an interrupt is generated. This interrupt is cleared when a character is loaded into the register.

SLLS053B – MAY 1989 – REVISED MARCH 1996

- **Integrates Most Communications Card Functions From the IBM PC/AT™ or Compatibles With Single- or Dual-Channel Serial Ports**
- **TL16C451 Consists of One TL16C450 Plus Centronix Printer Interface**
- **TL16C452 Consists of Two TL16C450s Plus a Centronix-Type Printer Interface**
- **Fully Programmable Serial Interface Characteristics:**
  - **5-, 6-, 7-, or 8-Bit Characters**
  - **Even-, Odd-, or No-Parity Bit Generation and Detection**
  - **1-, 1 1/2-, or 2 Stop-Bit Generation**
  - **Programmable Baud Rate (dc to 256 kbit/s)**
- **Fully Double Buffered for Reliable Asynchronous Operation**

description

The TL16C451 and TL16C452 provide single- and dual-channel (respectively) serial interfaces along with a single Centronix-type parallel-port interface. The serial interfaces provide a serial-to-parallel conversion for data received from a peripheral device or modem and a parallel-to-serial conversion for data transmitted by a CPU. The parallel interface provides a bidirectional parallel data port that fully conforms to the requirements for a Centronix-type printer interface. A CPU can read the status of the asynchronous communications element (ACE) interfaces at any point in the operation. The status includes the state of the modem signals ($\overline{CTS}$, $\overline{DSR}$, $\overline{RLSD}$, and RI) and any changes to these signals that have occurred since the last time they were read, the state of the transmitter and receiver including errors detected on received data, and printer status. The TL16C451 and TL16C452 provide control for modem signals ($\overline{RTS}$ and $\overline{DTR}$), interrupt enables, baud rate programming, and parallel-port control signals.

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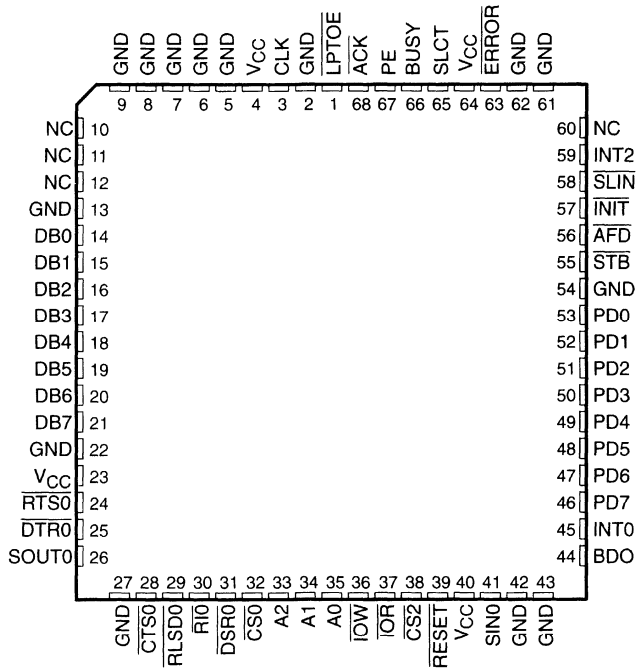
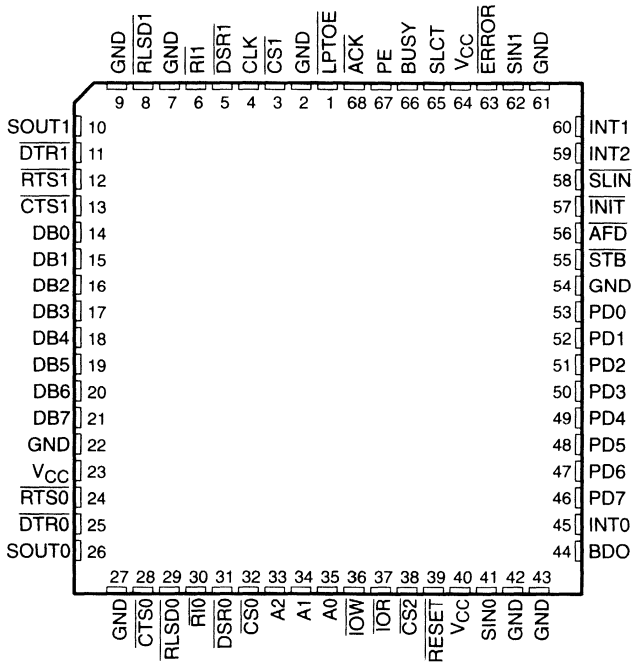
TL16C451 . . . FN PACKAGE
(TOP VIEW)

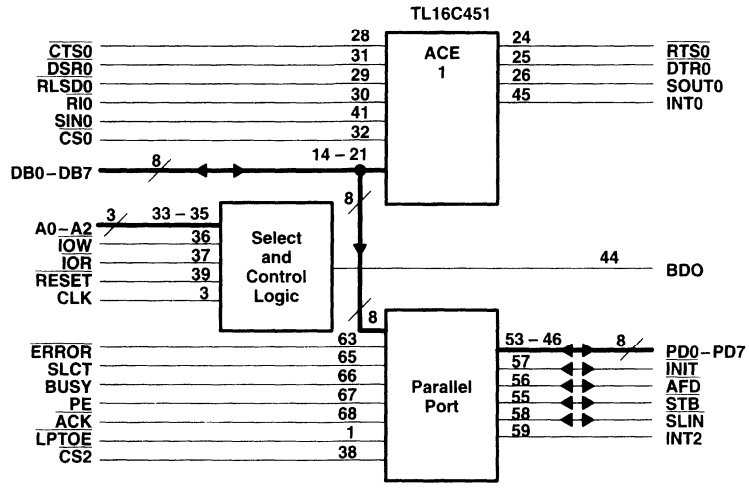


NC – No internal connection

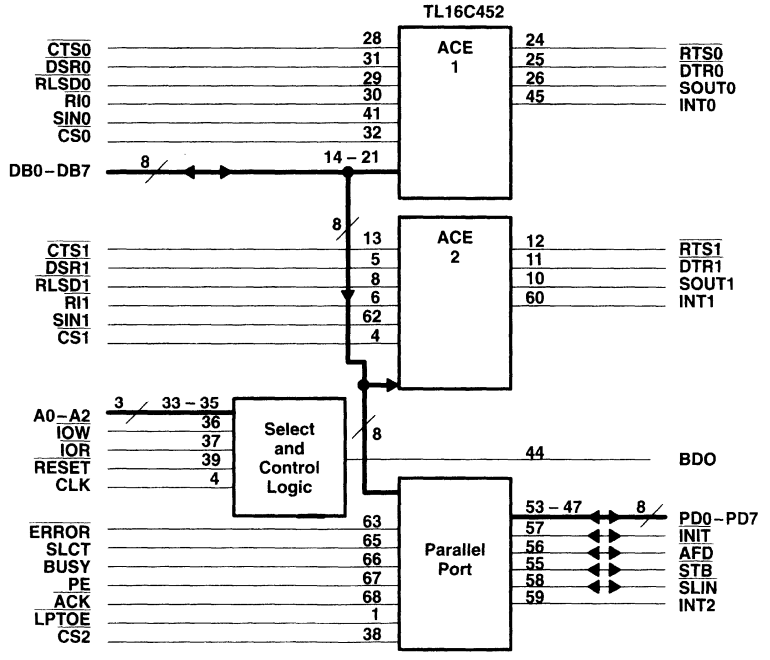
TL16C452 . . . FN PACKAGE
(TOP VIEW)



TL16C451 functional block diagram



TL16C452 functional block diagram



Terminal Functions

TERMINAL NAME†	TERMINAL NO.	I/O	DESCRIPTION
A0 A1 A2	35 34 33	I	Register select. A0, A1, and A2 are used during read and write operations to select the register to read from or write to. Refer to Table 1 for register addresses, also refer to the chip select signals ($\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$).
$\overline{ACK}$	68	I	Printer acknowledge. $\overline{ACK}$ goes low to indicate that a successful data transfer has taken place. It generates a printer port interrupt during its positive transition.
$\overline{AFD}$	56	I/O	Printer autofeed. $\overline{AFD}$ is an open-drain line that provides the printer with a low signal when continuous-form paper is to be autofed to the printer. An internal pullup is provided.
BDO	44	O	Bus buffer output. BDO is active (high) when the CPU is reading data. When active, this output can disable an external transceiver.
BUSY	66	I	Printer busy. BUSY is an input line from the printer that goes high when the printer is not ready to accept data.
CLK [V_{CC}]	4	I/O	External clock. CLK connects the ACE to the main timing reference.
$\overline{CS0}$ $\overline{CS1}$ [CLK] $\overline{CS2}$	32 3 38	I	Chip selects. Each chip select enables read and write operations to its respective channel. $\overline{CS0}$ and $\overline{CS1}$ select serial channels 0 and 1, respectively, and $\overline{CS2}$ selects the parallel port.
$\overline{CTS0}$ $\overline{CTS1}$ [GND]	28 13	I	Clear to send. $\overline{CTSx}$ is an active-low modem status signal. Its state can be checked by reading bit 4 (CTS) of the modem status register. Bit 0 (DCTS) of the modem status register indicates that this signal has changed states since the last read from the modem status register. If the modem status interrupt is enabled when $\overline{CTSx}$ changes state, an interrupt is generated.
DB0 – DB7	14 – 21	I/O	Data bus. Eight 3-state data lines provide a bidirectional path for data, control, and status information between the TL16C451/TL16C452 and the CPU. DB0 is the least significant bit (LSB).
$\overline{DSR0}$ $\overline{DSR1}$ [GND]	31 5	I	Data set ready. $\overline{DSRx}$ is an active-low modem status signal. Its state can be checked by reading bit 5 (DSR) of the modem status register. Bit 1 (DDSR) of the modem status register indicates that this signal has changed states since the last read from the modem status register. If the modem status interrupt is enabled when the $\overline{DSRx}$ changes state, an interrupt is generated.
$\overline{DTR0}$ $\overline{DTR1}$ [NC]	25 11	O	Data terminal ready. $\overline{DTRx}$, when active (low), informs a modem or data set that the ACE is ready to establish communication. $\overline{DTRx}$ is placed in the active state by setting the DTR bit of the modem control register. $\overline{DTRx}$ is placed in the inactive state either as a result of a reset or during loop mode operation or clearing bit 0 (DTR) of the modem control register.
$\overline{ERROR}$	63	I	Printer error. $\overline{ERROR}$ is an input line from the printer. The printer reports an error by holding this line low during the error condition.
$\overline{INIT}$	57	I/O	Printer initialize. $\overline{INIT}$ is an open-drain line that provides the printer with a signal that allows the printer initialization routine to be started. An internal pullup is provided.
INT0 INT1 [NC]	45 60	O	Interrupt. INTx is an active-high 3-state output that is enabled by bit 3 of the MCR. When active, INTx informs the CPU that the ACE has an interrupt to be serviced. Four conditions that cause an interrupt to be issued are: a receiver error, received data is available, the transmitter holding register is empty, and an enabled modem status interrupt. The INTx output is reset (low) either when the interrupt is serviced or as a result of a reset.
INT2	59	O	Printer port interrupt. INT2 is an active-high 3-state output generated by the positive transition of $\overline{ACK}$. It is enabled by bit 4 of the write control register.
$\overline{IOR}$	37	I	Data read strobe. When $\overline{IOR}$ input is active (low) while the ACE is selected, the CPU is allowed to read status information or data from a selected ACE register.
$\overline{IOW}$	36	I	Data write strobe. When $\overline{IOW}$ input is active (low) while the ACE is selected, the CPU is allowed to write control words or data into a selected ACE register.
$\overline{LPTOE}$	1	I	Parallel data output enable. When low, $\overline{LPTOE}$ enables the write data register to the PD0 – PD7 lines. A high puts the PD0 – PD7 lines in the high-impedance state allowing them to be used as inputs. $\overline{LPTOE}$ is usually tied low for printer operation.

† Names shown in brackets are for the TL16C451.

Terminal Functions (continued)

TERMINAL NAME†	TERMINAL NO.	I/O	DESCRIPTION
PD0–PD7	53–46	I/O	Parallel data bits (0–7). These eight lines provide a byte-wide input or output port to the system. The eight lines are held in a high-impedance state when $\overline{\text{LPTOE}}$ is high.
PE	67	I	Printer paper empty. This is an input line from the printer that goes high when the printer runs out of paper.
$\overline{\text{RESET}}$	39	I	Reset. When active (low), $\overline{\text{RESET}}$ clears most ACE registers and sets the state of various output signals. Refer to Table 2.
$\overline{\text{RI0}}$ $\overline{\text{RI1}}$ [GND]	30 6	I	Ring indicator. $\overline{\text{RIx}}$ is an active-low modem status signal. Its state can be checked by reading bit 6 (RI) of the modem status register. Bit 2 (TERI) of the modem status register indicates that the $\overline{\text{RIx}}$ input has transitioned from a low to a high state since the last read from the modem status register. If the modem status interrupt is enabled when this transition occurs, an interrupt is generated.
$\overline{\text{RLSD0}}$ $\overline{\text{RLSD1}}$ [GND]	29 8	I	Receive line signal detect. $\overline{\text{RLSDx}}$ is an active-low modem status signal. Its state can be checked by reading bit 7 of the modem status register. Bit 3 (DRLSD) of the modem status register indicates that this signal has changed states since the last read from the modem status register. If the modem status interrupt is enabled when $\overline{\text{RLSDx}}$ changes state, an interrupt is generated. This bit is low when a data carrier is detected.
$\overline{\text{RTS0}}$ $\overline{\text{RTS1}}$ [NC]	24 12	C	Request to send. When active (low), $\overline{\text{RTSx}}$ informs the modem or data set that the ACE is ready to transmit data. $\overline{\text{RTSx}}$ is set to its active state by setting the RTS modem control register bit and is set to its inactive (high) state either as a result of a reset or during loop mode operations or by clearing bit 1 (RTS) of the modem control register.
SIN0 SIN1 [GND]	41 62	I	Serial input. SINx is a serial data input from a connected communications device.
SLCT	65	I	Printer selected. SLCT is an input line from the printer that goes high when the printer has been selected.
$\overline{\text{SLIN}}$	58	I/O	Printer select. $\overline{\text{SLIN}}$ is an open-drain line that selects the printer when it is active (low). An internal pullup is provided on this line.
SOUT0 SOUT1 [NC]	26 10	I	Serial output. SOUTx is a composite serial data output to a connected communication device. SOUTx is set during a reset.
$\overline{\text{STB}}$	55	I/O	Printer strobe. $\overline{\text{STB}}$ is an open-drain line that provides communication synchronization between the TL16C451/TL16C452 and the printer. When it is active (low), it provides the printer with a signal to latch the data currently on the parallel port. An internal pullup is provided on this line.
V_{CC}	23,40, 64		5-V supply voltage
GND	2,7,9 22,27,42, 43,54,61		Supply common

† Names shown in brackets are for the TL16C451.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.5 V to 7 V
Input voltage range at any input, V_I . . . . . −0.5 V to 7 V
Output voltage range, V_O . . . . . −0.5 V to 7 V
Continuous total power dissipation . . . . . 1100 mW
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Case temperature for 10 seconds, T_C . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level Input voltage, V_{IH}	2		V_{CC}	V
Low-level Input voltage, V_{IL}	−0.5		0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −0.4 mA on DB0–DB7	2.4			V
		I_{OH} = −2 mA to 4 mA on PD0–PD7				
		I_{OH} = −0.2 mA on INIT, $\overline{AFD}$, $\overline{STB}$, and $\overline{SLIN}$				
		I_{OH} = −0.2 mA on all other outputs				
V_{OL}	Low-level output voltage	I_{OL} = 4 mA on DB0–DB7			0.4	V
		I_{OL} = 12 mA on PD0–PD7				
		I_{OL} = 10 mA on INIT, $\overline{AFD}$, $\overline{STB}$, and $\overline{SLIN}$ (see Note 2)				
		I_{OL} = 2 mA on all other outputs				
I_{lkg}	Input leakage current	V_{CC} = 5.25 V, V_{SS} = 0, V_I = 0 to 5.25 V, All other terminals floating			±10	µA
I_{oz}	High-impedance output current	V_{CC} = 5.25 V, V_{SS} = 0, V_O = 0 to 5.25 V, Chip selected and in write mode, or chip deselected			±20	µA
I_{CC}	Supply current	V_{CC} = 5.25 V, V_{SS} = 0, SIN, $\overline{DSR}$, $\overline{RLSD}$, $\overline{CTS}$, and $\overline{RI}$ at 2 V, All other inputs at 0.8 V, XTAL1 at 4 MHz, No load on outputs, Baud rate = 50 kbit/s			10	mA
C_{XTAL1}	Clock input capacitance	V_{CC} = 0, V_{SS} = 0, f = 1 MHz, T_A = 25°C, All others terminals grounded		15	20	pF
C_{XTAL2}	Clock output capacitance			20	30	pF
C_i	Input capacitance			6	10	pF
C_o	Output capacitance			10	20	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 2: $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$, and $\overline{SLIN}$ are open-collector output terminals that each have an internal pullup to V_{CC}. This generates a maximum of 2 mA of internal I_{OL} per terminal. In addition to this internal current, each terminal sinks at least 10 mA while maintaining the V_{OL} specification of 0.4 V maximum.

system timing requirements over recommended ranges of supply voltage and operating free-air temperature

	PARAMETER	FIGURE	MIN	MAX	UNIT
t_{cR}	Cycle time, read ($t_{w7} + t_{d8} + t_{d9}$)		175		ns
t_{cW}	Cycle time, write ($t_{w6} + t_{d5} + t_{d6}$)		175		ns
t_{w1}	Pulse duration, clock ↑	1	50		ns
t_{w2}	Pulse duration, clock ↓	1	50		ns
t_{w5}	Pulse duration, write strobe ($\overline{IOW}$) ↑	2	80		ns
t_{w6}	Pulse duration, read strobe ($\overline{IOR}$) ↓	3	80		ns
t_{wRST}	Pulse duration, reset		1000		ns
t_{su1}	Setup time, address (A0 – A2) valid before $\overline{IOW}$ ↓	2,3	15		ns
t_{su2}	Setup time, chip select ($\overline{CSx}$) valid before $\overline{IOW}$ ↓	2,3	15		ns
t_{su3}	Setup time, data (D0 – D7) valid before $\overline{IOW}$ ↑	2	15		ns
t_{h1}	Hold time, address (A0 – A2) valid after $\overline{IOW}$ ↑	2,3	20		ns
t_{h2}	Hold time, chip select ($\overline{CSx}$) valid after $\overline{IOW}$ ↑	2,3	20		ns
t_{h3}	Hold time, data (D0 – D7) valid before $\overline{IOW}$ ↑	2	15		ns
t_{d3}	Delay time, write cycle ($\overline{IOW}$) ↑ to $\overline{IOW}$ ↓	2	80		ns
t_{d4}	Delay time, read cycle ($\overline{IOR}$) ↑ to $\overline{IOR}$ ↓	3	80		ns

system switching characteristics over recommended ranges of supply voltage and operating free-air temperature

	PARAMETER	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d5}	Delay time, data (D0 – D7) valid before read ($\overline{IOR}$) ↑	3	C_L = 100 pF		60	ns
t_{d6}	Delay time, floating data (D0 – D7) valid after read ($\overline{IOR}$) ↑	3	C_L = 100 pF	0	60	ns
$t_{dis(R)}$	Read to driver disable, $\overline{IOR}$ ↓ to BD0 ↓	3	C_L = 100 pF		60	ns

receiver switching characteristics over recommended ranges of supply voltage and operating free-air temperature

	PARAMETER	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d7}	Delay time, RCLK ↑ to sample clock ↑	4			100	ns
t_{d8}	Delay time, stop (sample clock) ↑ to set interrupt (INTRPT) ↑	4		1	1	RCLK cycles
t_{d9}	Delay time, read RBR/LSR ($\overline{IOR}$) ↑ to reset interrupt (INTRPT) ↓	4	C_L = 100 pF		140	ns

transmitter switching characteristics over recommended ranges of supply voltage and operating free-air temperature

	PARAMETER	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d10}	Delay time, initial write THR ($\overline{IOW}$) ↑ to transmit start (SOUT) ↓	5		8	24	baudout cycles
t_{d11}	Delay time, stop (SOUT) low to interrupt (INTRPT) ↑	5		8	8	baudout cycles
t_{d12}	Delay time, write THR ($\overline{IOW}$) ↓ to reset interrupt (INTRPT) low	5	C_L = 100 pF		140	ns
t_{d13}	Delay time, initial write ($\overline{IOW}$) ↑ to THRE interrupt (INTRPT) ↑	5		16	32	baudout cycles
t_{d14}	Delay time, read IIR ($\overline{IOR}$) ↑ to reset THRE interrupt (INTRPT) low	5	C_L = 100 pF		140	ns

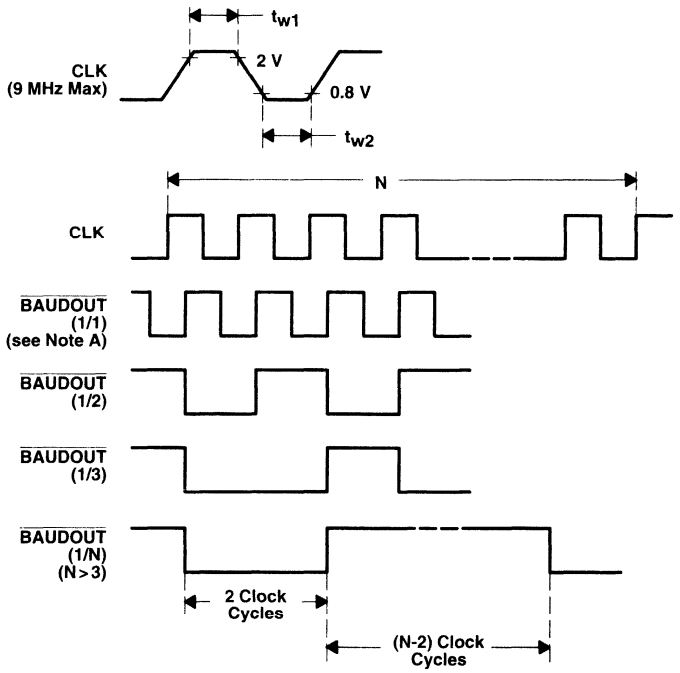
modem control switching characteristics over recommended ranges of supply voltage and operating free-air temperature

	PARAMETER	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d15}	Delay time, write MCR ($\overline{IOW}$) ↑ to output ($\overline{RTS}$, $\overline{DTS}$) ↓↑	6	C_L = 100 pF		100	ns
t_{d16}	Delay time, modem input ($\overline{CTS}$, $\overline{DSR}$, $\overline{RLSD}$) ↑ to set interrupt (INTRPT) high	6	C_L = 100 pF		170	ns
t_{d17}	Delay time, read MSR ($\overline{IOR}$) ↑ to reset interrupt (INTRPT) low	6	C_L = 100 pF		140	ns

parallel port switching characteristics over recommended ranges of supply voltage and operating free-air temperature

	PARAMETER	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d18}	Delay time, write parallel port control ($\overline{SLIN}$, $\overline{AFD}$, $\overline{STB}$, $\overline{INIT}$) ↓↑ to output ($\overline{IOW}$) high	7	C_L = 100 pF		60	ns
t_{d19}	Delay time, write parallel port data (P0 – P7) ↓↑ to output ($\overline{IOW}$) high	7	C_L = 100 pF		60	ns
t_{d20}	Delay time, output enable to data, PD0 – PD7 valid after $\overline{LPTOE}$ ↓	7	C_L = 100 pF		60	ns
t_{d21}	Delay time, $\overline{ACK}$ ↓↑ to INT2 ↓↑	7	C_L = 100 pF		100	ns

PARAMETER MEASUREMENT INFORMATION



NOTE A: $\overline{BAUDOUT}$ is an internally generated signal used in the receiver and transmitter circuits to synchronize data.

Figure 1. Baud Generator Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

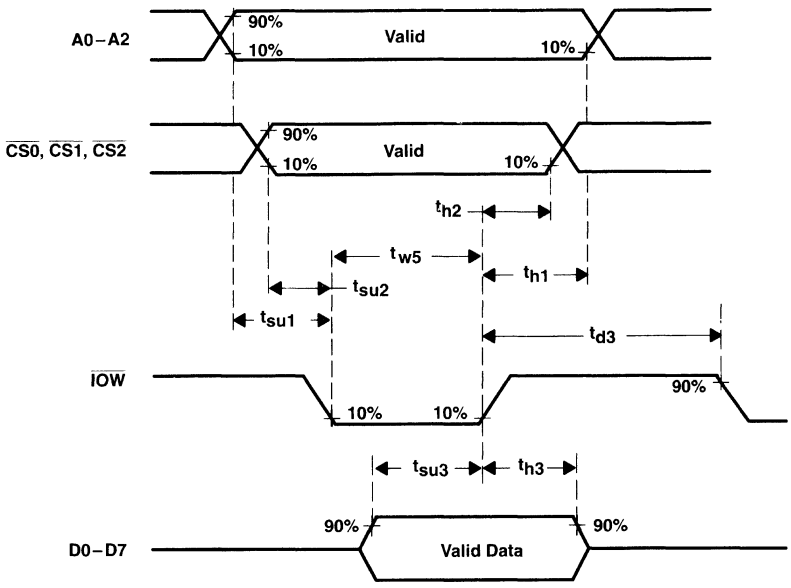


Figure 2. Write Cycle Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

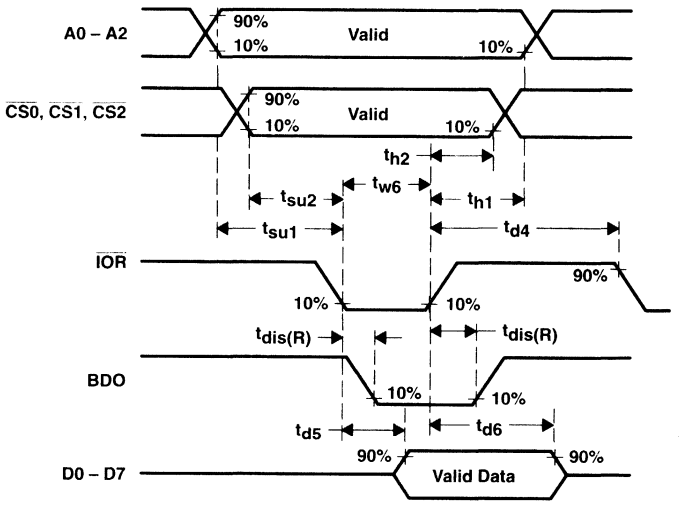


Figure 3. Read Cycle Timing Waveforms

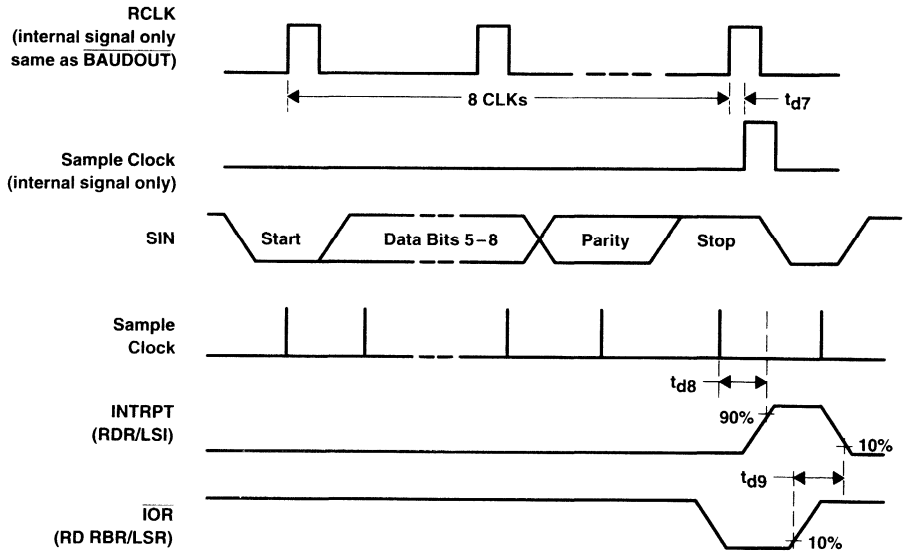


Figure 4. Receiver Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

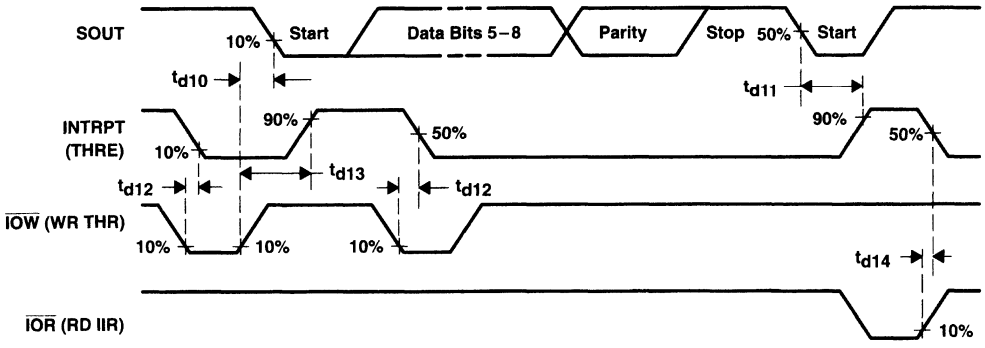


Figure 5. Transmitter Timing Waveforms

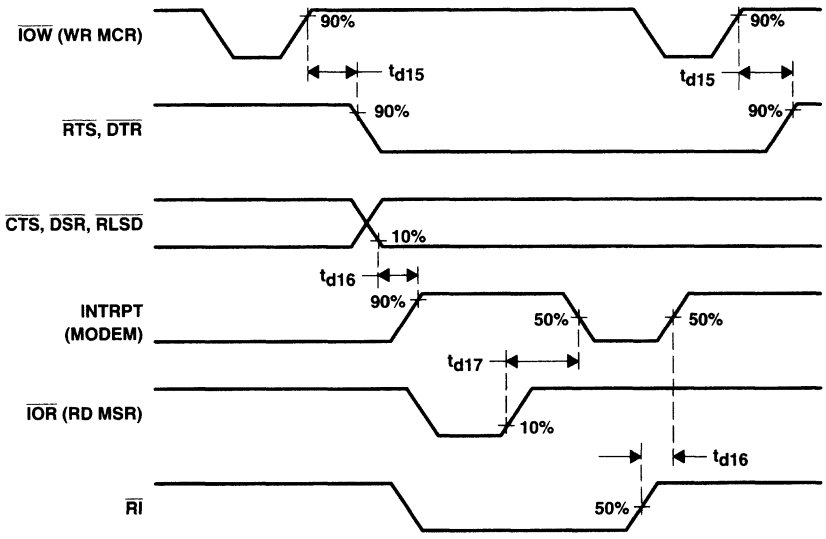


Figure 6. Modem Control Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

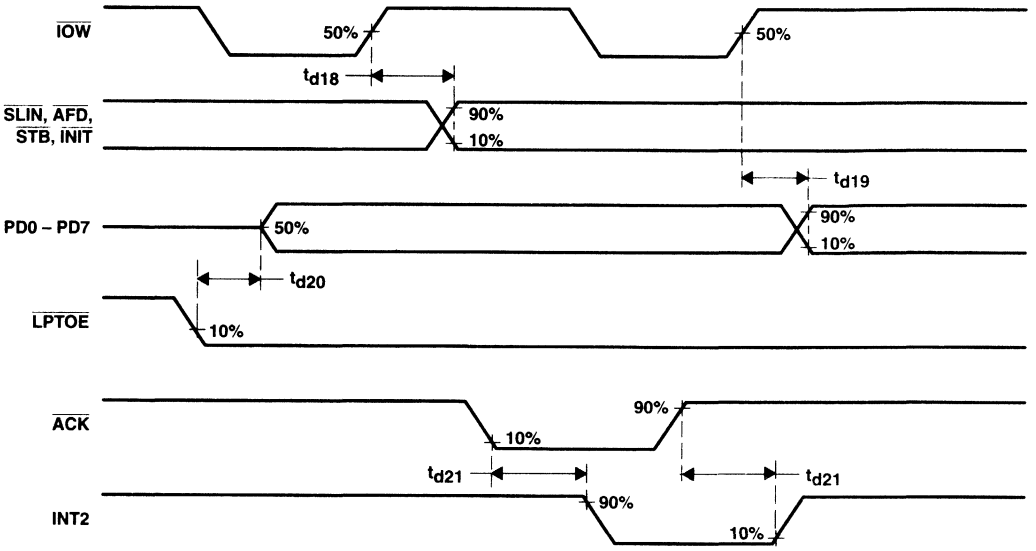


Figure 7. Parallel Port Timing Waveforms

APPLICATION INFORMATION

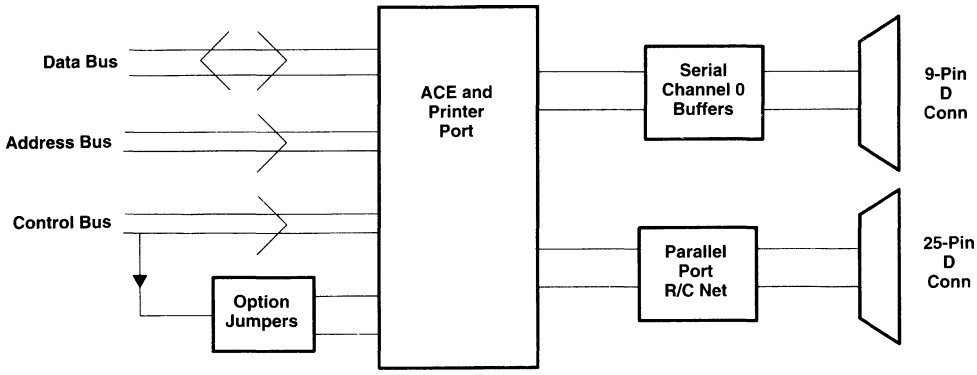


Figure 8. Basic TL16C451 Test Configuration

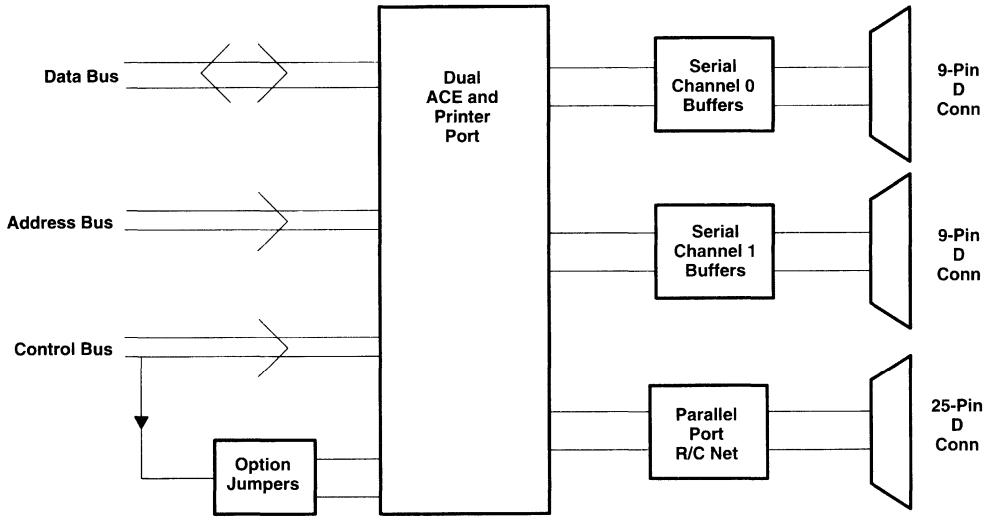


Figure 9. Basic TL16C452 Test Configuration

PRINCIPLES OF OPERATION

Table 1. Register Selection

DLAB†	A2	A1	A0	REGISTER
0	L	L	L	Receiver buffer (read), transmitter holding register (write)
0	L	L	H	Interrupt enable register
X	L	H	L	Interrupt identification register (read only)
X	L	H	H	Line control register
X	H	L	L	Modem control register
X	H	L	H	Line status register
X	H	H	L	Modem status register
X	H	H	H	Scratch register
1	L	L	L	Divisor latch (LSB)
1	L	L	H	Divisor latch (MSB)

† The divisor latch access bit (DLAB) is the most significant bit of the line control register. The DLAB signal is controlled by writing to this bit location (see Table 3).

Table 2. ACE Reset Functions

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt enable register	$\overline{\text{RESET}}$	All bits cleared (0–3 forced and 4–7 permanent)
Interrupt identification register	$\overline{\text{RESET}}$	Bit 0 is set, bits 1 and 2 are cleared, and bits 3–7 are permanently cleared
Line control register	$\overline{\text{RESET}}$	All bits cleared
Modem control register	$\overline{\text{RESET}}$	All bits cleared
Line status register	$\overline{\text{RESET}}$	Bits 5 and 6 are set, all other bits are cleared
Modem status register	$\overline{\text{RESET}}$	Bits 0–3 are cleared, bits 4–7 are input signals
SOUT	$\overline{\text{RESET}}$	High
INTRPT (receiver error flag)	Read LSR/$\overline{\text{RESET}}$	Low
INTRPT (received data available)	Read RBR/$\overline{\text{RESET}}$	Low
INTRPT (transmitter holding register empty)	Read IIR/Write THR/$\overline{\text{RESET}}$	Low
INTRPT (modem status changes)	Read MSR/$\overline{\text{RESET}}$	Low
$\overline{\text{OUT2}}$ (interrupt enable)	$\overline{\text{RESET}}$	High
$\overline{\text{RTS}}$	$\overline{\text{RESET}}$	High
$\overline{\text{DTR}}$	$\overline{\text{RESET}}$	High
$\overline{\text{OUT1}}$	$\overline{\text{RESET}}$	High
Scratch register	$\overline{\text{RESET}}$	No effect
Divisor latch (LSB and MSB) registers	$\overline{\text{RESET}}$	No effect
Receiver buffer registers	$\overline{\text{RESET}}$	No effect
Transmitter holding registers	$\overline{\text{RESET}}$	No effect

PRINCIPLES OF OPERATION

accessible registers

The system programmer, using the CPU, has access to and control over any of the ACE registers that are summarized in Table 3. These registers control ACE operations, receive data, and transmit data. Descriptions of these registers are given in Table 3.

Table 3. Summary of Accessible Registers

Bit No.	REGISTER ADDRESS										
	O DLAB = 0	O DLAB = 0	1 DLAB = 0	2	3	4	5	6	7	O DLAB = 1	1 DLAB = 0
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident. Register (Read Only)	Line Control Register	Modem Control Register	Line Status Register	Modem Status Register	Scratch Register	Divisor Latch (LSB)	Latch (MSB)
	RBR	THR	IER	IIR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Data Bit 0†	Data Bit 0	Enable Received Data Available Interrupt (ERBF)	"0" If Interrupt Pending	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBE)	Interrupt ID Bit (0)	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable Modem Status Interrupt (EDSSI)	0	Parity Enable (PEN)	Out 2 (Interrupt Enable)	Framing Error (FE)	Delta Receive Line Signal Detect (DRLSD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmit-ter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmit-ter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Receive Line Signal Detect (RLSD)	Bit 7	Bit 7	Bit 15

† Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

PRINCIPLES OF OPERATION

interrupt control logic

The interrupt control logic is shown in Figure 10.

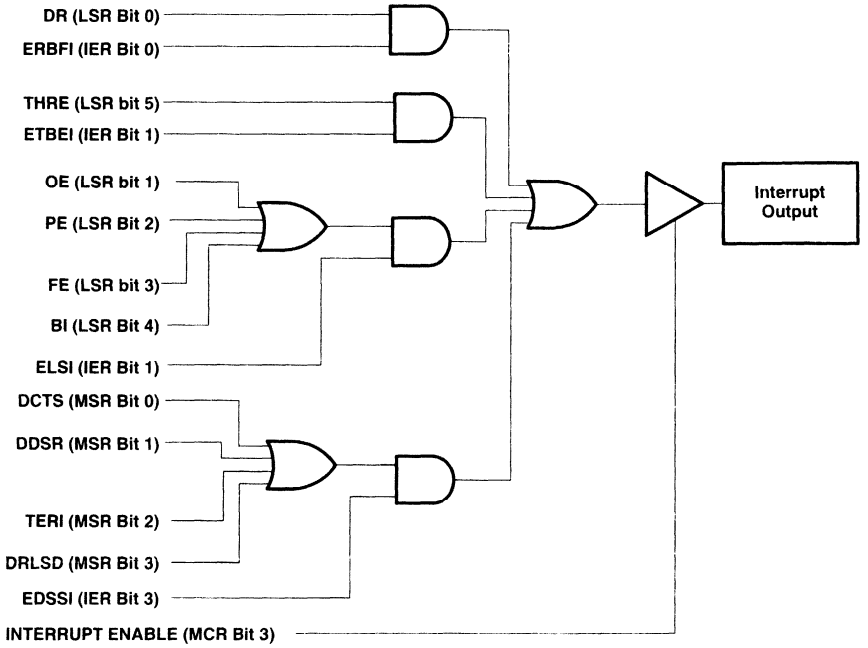


Figure 10. Interrupt Control Logic

interrupt enable register (IER)

The IER enables each of the four types of interrupts (refer to Table 4) and the INTRPT output signal in response to an interrupt generation. The IER can also disable the interrupt system by clearing bits 0 through 3. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bit 0: This bit, when set, enables the received data available interrupt.
- Bit 1: This bit, when set, enables the THRE interrupt.
- Bit 2: This bit, when set, enables the receiver line status interrupt.
- Bit 3: This bit, when set, enables the modem status interrupt.
- Bits 4 thru 7: These bits in the IER are not used and are always cleared.

PRINCIPLES OF OPERATION

interrupt identification register (IIR)

The ACE has an on-chip interrupt generation and prioritization capability that permits a flexible interface with most microprocessors.

The ACE provides four prioritized levels of interrupts:

- Priority 1 – Receiver line status (highest priority)
- Priority 2 – Receiver data ready or receiver character time out
- Priority 3 – Transmitter holding register empty
- Priority 4 – Modem status (lowest priority)

When an interrupt is generated, the IIR indicates that an interrupt is pending and indicates the type of interrupt in its three least significant bits (bits 0, 1, and 2). The contents of this register are summarized in Table 3 and described in Table 4.

- Bit 0: This bit can be used either in a hardwire prioritized or polled interrupt system. When this bit is cleared, an interrupt is pending. When bit 0 is set, no interrupt is pending.
- Bits 1 and 2: These two bits identify the highest priority interrupt pending as indicated in Table 4.
- Bits 3 – 7: These bits in the interrupt identification register are not used and are always clear.

Table 4. Interrupt Control Functions

INTERRUPT IDENTIFICATION REGISTER			PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET METHOD
BIT 2	BIT 1	BIT 0				
0	0	1	None	None	None	–
1	1	0	1	Receiver line status	Overrun error, parity error, framing error or break interrupt	Reading the line status register
1	0	0	2	Received data available	Receiver data available	Reading the receiver buffer register
0	1	0	3	Transmitter holding register empty	Transmitter holding register empty	Reading the interrupt Identification register (if source of interrupt) or writing into the transmitter holding register
0	0	0	4	Modem status	Clear to send, data set ready, ring indicator, or data carrier detect	Reading the modem status register

PRINCIPLES OF OPERATION

line control register (LCR)

The system programmer controls the format of the asynchronous data communication exchange through the LCR. In addition, the programmer is able to retrieve, inspect, and modify the contents of the LCR; this eliminates the need for separate storage of the line characteristics in system memory. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. These bits are encoded as shown in Table 5.

Table 5. Serial Character Word Length

Bit 1	Bit 0	Word Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

- Bit 2: This bit specifies either one, one and one-half, or two stop bits in each transmitted character. When bit 2 is cleared, one stop bit is generated in the data. When bit 2 is set, the number of stop bits generated is dependent on the word length selected with bits 0 and 1. The number of stop bits generated in relation to word length and bit 2 is as shown in Table 6.

Table 6. Number of Stop Bits Generated

Bit 2	Word Length Selected by Bits 1 and 2	Number of Stop Bits Generated
0	Any word length	1
1	5 bits	1 1/2
1	6 bits	2
1	7 bits	2
1	8 bits	2

- Bit 3: This bit is the parity enable bit. When bit 3 is set, a parity bit is generated in transmitted data between the last data word bit and the first stop bit. In received data, when bit 3 is set, parity is checked. When bit 3 is cleared, no parity is generated or checked.
- Bit 4: This bit is the even parity select bit. When parity is enabled (bit 3 is set) and bit 4 is set, even parity (an even number of logic is in the data and parity bits) is selected. When parity is enabled and bit 4 is cleared, odd parity (an odd number of logic 1s) is selected.
- Bit 5: This is the stick parity bit. When bits 3, 4, and 5 are set, the parity bit is transmitted and checked as cleared. When bits 3 and 5 are set and bit 4 is cleared, the parity bit is transmitted and checked as set.
- Bit 6: This bit is the break control bit. Bit 6 is set to force a break condition, i.e, a condition where SOUT terminal is forced to the spacing (cleared) state. When bit 6 is cleared, the break condition is disabled. The break condition has no affect on the transmitter logic, it only affects the serial output.
- Bit 7: This bit is the divisor latch access bit (DLAB). Bit 7 must be set to access the divisor latches of the baud generator during a read or write. Bit 7 must be cleared during a read or write to access the receiver buffer, the THR, or the IER.

PRINCIPLES OF OPERATION

line status register (LSR)†

The LSR provides information to the CPU concerning the status of data transfers. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bit 0: This bit is the data ready (DR) indicator for the receiver. Bit 0 is set whenever a complete incoming character has been received and transferred into the RBR and is cleared by reading the RBR.
- Bit 1‡: This bit is the overrun error (OE) indicator. When bit 1 is set, it indicates that before the character in the RBR was read, it was overwritten by the next character transferred into the register. The OE indicator is cleared every time the CPU reads the contents of the LSR.
- Bit 2‡: This bit is the parity error (PE) indicator. When bit 2 is set, it indicates that the parity of the received data character does not match the parity selected in the LCR (bit 4). The PE bit is cleared every time the CPU reads the contents of the LSR.
- Bit 3‡: This bit is the framing error (FE) indicator. When bit 3 is set, it indicates that the received character did not have a valid (set) stop bit. The FE bit is cleared every time the CPU reads the contents of the LSR.
- Bit 4‡: This bit is the break interrupt (BI) indicator. When bit 4 is set, it indicates that the received data input was held clear for longer than a full-word transmission time. A full-word transmission time is defined as the total time of the start, data, parity, and stop bits. The BI bit is cleared every time the CPU reads the contents of the LSR.
- Bit 5: This bit is the THRE indicator. Bit 5 is set when the THR is empty, indicating that the ACE is ready to accept a new character. If the THRE interrupt is enabled when the THRE bit is set, then an interrupt is generated. THRE is set when the contents of the THR are transferred to the transmitted shift register. This bit is cleared concurrent with the loading of the THR by the CPU.
- Bit 6: This bit is the transmitter empty (TEMT) indicator, bit 6 is set when the THR and the transmitter shift register are both empty. When either the THR or the transmitter shift register contains a data character, the TEMT bit is cleared.
- Bit 7: This bit is always clear.

† The line status register is intended for read operations only; writing to this register is not recommended outside of a factory testing environment.
‡ Bits 1 through 4 are the error conditions that produce a receiver line status interrupt.

modem control register (MCR)

The MCR is an 8-bit register that controls an interface with a modem, data set, or peripheral device that is emulating a modem. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bit 0: This bit (DTR) controls the data terminal ready ($\overline{DTR}$) output. Setting bit 0 forces the $\overline{DTR}$ output to its active state (low). When bit 0 is cleared, $\overline{DTR}$ goes high.
- Bit 1: This bit (RTS) controls the request to send ($\overline{RTS}$) output in a manner identical to bit 0's control over the $\overline{DTR}$ output.
- Bit 2: This bit (OUT 1) is a reserved location used only in the loopback mode.
- Bit 3: This bit (OUT 2) controls the output enable for the interrupt signal. When set, the interrupt is enabled. When bit 3 is cleared, the interrupt is disabled.

PRINCIPLES OF OPERATION

modem control register (MCR) (continued)

- Bit 4: This bit provides a local loopback feature for diagnostic testing of the ACE. When this bit is set, the following occurs:

  1. The SOUT is asserted high.
  2. The SIN is disconnected.
  3. The output of the transmitter shift register is looped back into the receiver shift register input.
  4. The four modem status inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{RLSD}$, and $\overline{RI}$) are disconnected.
  5. The MCR bits (DTR, RTS, OUT1, and OUT2) are connected to the modem status register bits (DSR, CTS, RI, and RLSD), respectively.
  6. The four modem control output terminals are forced to their inactive states (high).

  In the diagnostic mode, data that is transmitted is immediately received. This allows the processor to verify the transmit and receive data paths to the ACE. The receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational but the modem control interrupt sources are now the lower four bits of the MCR instead of the four modem control inputs. All interrupts are still controlled by the IER.

- Bits 5 through 7: These bits are always cleared.

modem status register (MSR)

The MSR is an 8-bit register that provides information about the current state of the control lines from the modem, data set, or peripheral device to the CPU. Additionally, four bits of this register provides change information; when a control input from the modem changes state the appropriate bit is set. All four bits are cleared when the CPU reads the MSR. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bit 0. This bit is the delta clear to send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input has changed states since the last time it was read by the CPU. When this bit is set and the modem status Interrupt is enabled, a modem status interrupt is generated.
- Bit 1. This bit is the delta data set ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input has changed states since the last time it was read by the CPU. When this bit is set and the modem status Interrupt is enabled, a modem status interrupt is generated.
- Bit 2. This bit is the trailing edge of ring indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from a low to a high state. When this bit is set and the modem status Interrupt is enabled, a modem status interrupt is generated.
- Bit 3. This bit is the delta receive line signal detect (DRLSD) indicator. Bit 3 indicates that the $\overline{RLSD}$ input to the chip has changed states since the last time it was read by the CPU. When this bit is set and the modem status interrupt is enabled, a modem status interrupt is generated.
- Bit 4. This bit is the complement of the clear to send ($\overline{CTS}$) input. When bit 4 (loop) of the MCR is set, bit 4 is equivalent to the MCR bit 1 (RTS).
- Bit 5. This bit is the complement of the data set ready ($\overline{DSR}$) input. When bit 4 (loop) of the MCR is set, bit 5 is equivalent to the MCR bit 0 (DTR).
- Bit 6. This bit is the complement of the ring indicator ($\overline{RI}$) input. When bit 4 (loop) of the MCR is set, bit 6 is equivalent to the MCR bit 2 (OUT 1).
- Bit 7. This bit is the complement of the receive line signal detect ($\overline{RLSD}$) input. When bit 4 (loop) of the MCR is set, bit 7 is equivalent to the MCR bit 3 (OUT 2).

PRINCIPLES OF OPERATION

parallel port registers

The parallel port registers interface either device to a Centronix-style printer interface. When chip select 2 ($\overline{CS2}$) is low, the parallel port is selected. Tables 7 and 8 show the registers associated with this parallel port. The read or write function of the register is controlled by the state or the read ($\overline{IOR}$) and write ($\overline{IOW}$) terminal as shown. The read data register allows the microprocessor to read the information on the parallel bus.

The read status register allows the microprocessor to read the status of the printer in the five most significant bits. The status bits are printer busy ($\overline{BUSY}$), acknowledge ($\overline{ACK}$) which is a handshake function, paper empty (PE), printer selected (SLCT), and error ($\overline{ERROR}$). The read control register allows the state of the control lines to be read. The write control register sets the state of the control lines, which are interrupt enable (IRQ ENB), select in (SLIN), initialize the printer ($\overline{INIT}$), autofeed the paper (AFD), and strobe (STB), which informs the printer of the presence of a valid byte on the parallel bus. These signals are cleared when a reset occurs. The write data register allows the microprocessor to write a byte to the parallel bus. The parallel port is completely compatible with the parallel port implementation used in the IBM serial/parallel adaptor.

Table 7. Parallel Port Registers

REGISTER	REGISTER BITS							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Read data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Read status	$\overline{BUSY}$	$\overline{ACK}$	PE	SLCT	$\overline{ERROR}$	1	1	1
Read control	1	1	1	IRQ ENB	SLIN	$\overline{INIT}$	AFD	STB
Write data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Write control	1	1	1	IRQ ENB	SLIN	$\overline{INIT}$	AFD	STB

Table 8. Parallel Port Register Select

CONTROL TERMINALS					REGISTER SELECTED
$\overline{IOR}$	$\overline{IOW}$	$\overline{CS2}$	A1	A0	
L	H	L	L	L	Read data
L	H	L	L	H	Read status
L	H	L	H	L	Read control
L	H	L	H	H	Invalid
H	L	L	L	L	Write data
H	L	L	L	H	Invalid
H	L	L	H	L	Write control
H	L	L	H	H	Invalid

PRINCIPLES OF OPERATION

programmable baud generator

The ACE contains a programmable baud generator that takes a clock input in the range between dc and 9 MHz and divides it by a divisor in the range between 1 and ($2^{16}-1$). The output frequency of the baud generator is sixteen times (16×) the baud rate. The formula for the divisor is:

$$\text{divisor \#} = \text{CLK frequency input} \div (\text{desired baud rate} \times 16)$$

Two 8-bit registers, called divisor latches, store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization of the ACE in order to ensure desired operation of the baud generator. When either of the divisor latches is loaded, a 16-bit baud counter is also loaded to prevent long counts on initial load. For baud rates of 38.4 kilobits per second and below, the error obtained is very small. The accuracy of the selected baud rate is dependent on the selected crystal frequency.

receiver buffer register (RBR)

The ACE receiver section consists of a receiver shift register and a RBR. Timing is supplied by the 16× receiver clock (RCLK). Receiver section control is a function of the ACE line control register.

The ACE receiver shift register receives serial data from the serial input (SIN) terminal. The receiver shift register then converts the data to a parallel form and loads it into the RBR. When a character is placed in the RBR and the received data available interrupt is enabled, an interrupt is generated. This interrupt is cleared when the data is read out of the RBR.

scratch register

The scratch register is an 8-bit register that is intended for programmer use as a scratchpad, in the sense that it temporarily holds programmer data without affecting any other ACE operation.

transmitter holding register (THR)

The ACE transmitter section consists of a THR and a transmitter shift register. Timing is supplied by the baud out ($\overline{\text{BAUDOUT}}$) clock signal. Transmitter section control is a function of the ACE line control register.

The ACE THR receives data off of the internal data bus and, when the shift register is idle, moves it into the transmitter shift register. The transmitter shift register serializes the data and outputs it at the serial output (SOUT). When the THR is empty and the transmitter holding register empty (THRE) interrupt is enabled, an interrupt is generated. This interrupt is cleared when a character is loaded into the register.

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- **Capable of Running With All Existing TL16C450 Software**
- **After Reset, All Registers Are Identical to the TL16C450 Register Set**
- **In the FIFO Mode, Transmitter and Receiver Are Each Buffered With 16-Byte FIFOs to Reduce the Number of Interrupts to the CPU**
- **In the TL16C450 Mode, Holding and Shift Registers Eliminate the Need for Precise Synchronization Between the CPU and Serial Data**
- **Programmable Baud Rate Generator Allows Division of Any Input Reference Clock by 1 to ($2^{16}-1$) and Generates an Internal 16× Clock**
- **Standard Asynchronous Communication Bits (Start, Stop, and Parity) Added to or Deleted From the Serial Data Stream**
- **Independent Receiver Clock Input**
- **Transmit, Receive, Line Status, and Data Set Interrupts Independently Controlled**
- **Fully Programmable Serial Interface Characteristics:**
  - **5-, 6-, 7-, or 8-Bit Characters**
  - **Even-, Odd-, or No-Parity Bit Generation and Detection**
  - **1-, 1 1/2-, or 2-Stop Bit Generation**
  - **Baud Generation (dc to 256 Kbit/s)**
- **False-Start Bit Detection**
- **Complete Status Reporting Capabilities**
- **3-State TTL Drive Capabilities for Bidirectional Data Bus and Control Bus**
- **Line Break Generation and Detection**
- **Internal Diagnostic Capabilities:**
  - **Loopback Controls for Communications Link Fault Isolation**
  - **Break, Parity, Overrun, Framing Error Simulation**
- **Fully Prioritized Interrupt System Controls**
- **Modem Control Functions ($\overline{CTS}$, $\overline{RTS}$, $\overline{DSR}$, $\overline{DTR}$, $\overline{RI}$, and $\overline{DCD}$)**
- **Faster Plug-In Replacement for National Semiconductor NS16550A**

description

The TL16C550A is a functional upgrade of the TL16C450 asynchronous communications element (ACE). Functionally identical to the TL16C450 on power up (character mode†), the TL16C550A can be placed in an alternate mode (FIFO) to relieve the CPU of excessive software overhead.

In this mode, internal FIFOs are activated allowing 16 bytes (plus 3 bits of error data per byte in the receiver FIFO) to be stored in both receive and transmit modes. To minimize system overhead and maximize system efficiency, all logic is on the chip. Two of the TL16C450 terminal functions (terminals 24 and 29 on the N package and terminals 27 and 32 on the FN package) have been changed to allow signalling of direct memory address (DMA) transfers.

The TL16C550A performs serial-to-parallel conversion on data received from a peripheral device or modem and parallel-to-serial conversion on data received from its CPU. The CPU can read and report on the status of the ACE at any point in the ACE's operation. Reported status information includes the type of transfer operation in progress, the status of the operation, and any error conditions encountered.

The TL16C550A ACE includes a programmable, on-board, baud rate generator. This generator is capable of dividing a reference clock input by divisors from 1 to ($2^{16}-1$) and producing a 16× clock for driving the internal transmitter logic. Provisions are included to use this 16× clock to drive the receiver logic. Also included in the ACE is a complete modem control capability and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link.

† The TL16C550A can also be reset to the TL16C450 mode under software control.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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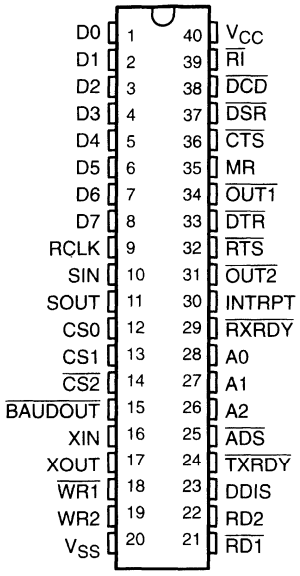
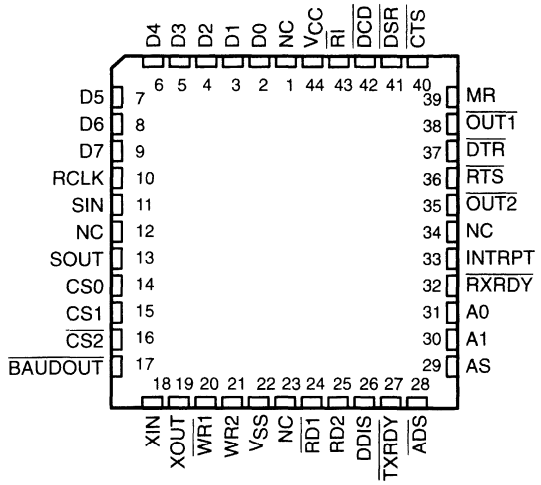
N PACKAGE
(TOP VIEW)

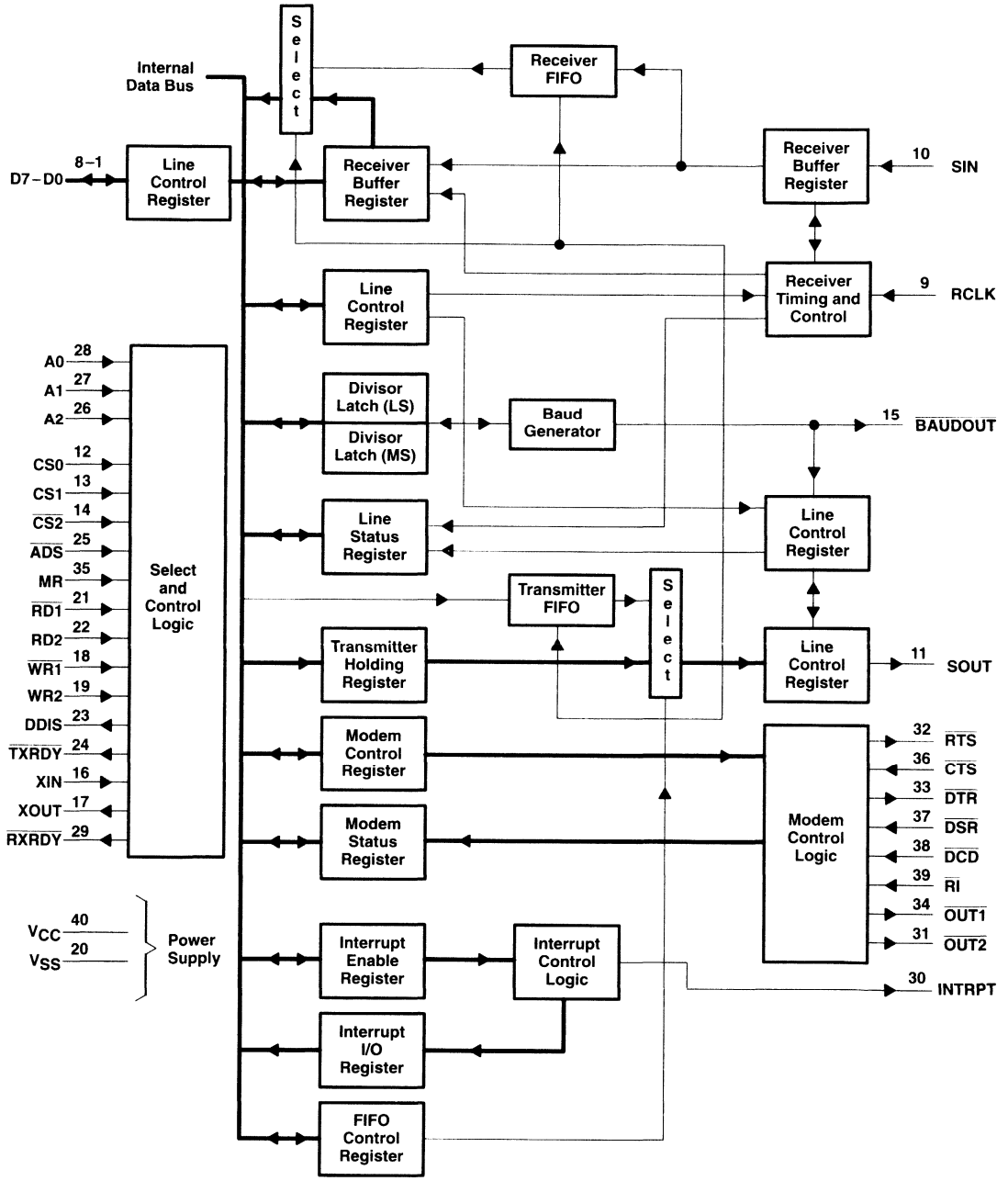


FN PACKAGE
(TOP VIEW)



NC – No internal connection

block diagram



NOTE A: Terminal numbers shown are for the N package.

Terminal Functions

TERMINAL NAME	TERMINAL NO.†	I/O	DESCRIPTION
A0 A1 A2	28 [31] 27 [30] 26 [29]	I	Register select. A0, A1, and A2 are used during read and write operations to select the ACE register to read from or write to. Refer to Table 1 for register addresses, also refer to the address strobe ($\overline{ADS}$) signal description.
$\overline{ADS}$	25 [28]	I	Address strobe. When $\overline{ADS}$ is active (low), the register select signals (A0, A1, and A2) and chip select signals (CS0, CS1, $\overline{CS2}$) drive the internal select logic directly; when high, the register select and chip select signals are held in the state they were in when the low-to-high transition of $\overline{ADS}$ occurred.
$\overline{BAUDOUT}$	15 [17]	O	Baud out. $\overline{BAUDOUT}$ is a 16× clock signal for the transmitter section of the ACE. The clock rate is established by the reference oscillator frequency divided by a divisor specified by the baud generator divisor latches. $\overline{BAUDOUT}$ may also be used for the receiver section by tying this output to the RCLK input.
CS0 CS1 $\overline{CS2}$	12 [14] 13 [15] 14 [16]	I	Chip select. When CSx is active (high, high, and low respectively), the ACE is selected. If any of these inputs are inactive, the ACE remains inactive. Refer to the $\overline{ADS}$ (address strobe) signal description.
$\overline{CTS}$	36 [40]	I	Clear to send. $\overline{CTS}$ is a modem status signal. Its condition can be checked by reading bit 4 (CTS) of the modem status register. Bit 0 (DCTS) of the modem status register indicates that this signal has changed states since the last read from the modem status register. If the modem status interrupt is enabled when $\overline{CTS}$ changes state, an interrupt is generated.
D0 – D7	1 – 8 [2 – 9]	I/O	Data bus. Eight 3-state data lines provide a bidirectional path for data, control, and status information between the ACE and the CPU.
$\overline{DCD}$	38 [42]	I	Data carrier detect. $\overline{DCD}$ is a modem status signal. Its condition can be checked by reading bit 7 (DCD) of the modem status register. Bit 3 (DDCD) of the modem status register indicates that this signal has changed states since the last read from the modem status register. If the modem status interrupt is enabled when the $\overline{DCD}$ changes state, an interrupt is generated.
DDIS	23 [26]	O	Driver disable. This output is active (high) when the CPU is not reading data. When active, this output can disable an external transceiver.
$\overline{DSR}$	37 [41]	I	Data set ready. $\overline{DSR}$ is a modem status signal. Its condition can be checked by reading bit 5 (DSR) of the modem status register. Bit 1 (DDSR) of the modem status register indicates that this signal has changed states since the last read from the modem status register. If the modem status interrupt is enabled when the $\overline{DSR}$ changes state, an interrupt is generated.
$\overline{DTR}$	33 [37]	O	Data terminal ready. When active (low), $\overline{DTR}$ informs a modem or data set that the ACE is ready to establish communication. $\overline{DTR}$ is placed in the active state by setting the DTR bit of the modem control register to a high level. $\overline{DTR}$ is placed in the inactive state either as a result of a master reset or during loop mode operation or clearing bit 0 (DTR) of the modem control register.
INTRPT	30 [33]	O	Interrupt. When active (high), INTRPT informs the CPU that the ACE has an interrupt to be serviced. Four conditions that cause an interrupt to be issued are: a receiver error, received data is available or timeout (FIFO mode only), transmitter holding register empty, or an enabled modem status interrupt. The INTRPT output is reset (deactivated) either when the interrupt is serviced or as a result of a master reset.
MR	35 [39]	I	Master reset. When active (high), MR clears most ACE registers and sets the state of various output signals. Refer to Table 2.
$\overline{OUT1}$ $\overline{OUT2}$	34 [38] 31 [35]	O	Outputs 1 and 2. $\overline{OUT1}$ and $\overline{OUT2}$ are user-designated output terminals that are set to their active states by setting their respective modem control register bits (OUT1 and OUT2) high. $\overline{OUT1}$ and $\overline{OUT2}$ are set to their inactive (high) states as a result of master reset or during loop mode operations or by clearing bit 2 (OUT1) or bit 3 (OUT2) of the modem control register.
RCLK	9 [10]	I	Receiver clock. RCLK is the 16× baud rate clock for the receiver section of the ACE.
$\overline{RD1}$ RD2	21 [24] 22 [25]	I	Read inputs. When either $\overline{RD1}$ or RD2 are active (high or low respectively) while the ACE is selected, the CPU is allowed to read status information or data from a selected ACE register. Only one of these inputs is required for the transfer of data during a read operation; the other input should be tied in its inactive state (i.e., RD2 tied low or $\overline{RD1}$ tied high).

† Terminal numbers shown in brackets are for the FN package.

Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO.†	I/O	DESCRIPTION
$\overline{RI}$	39 [43]	I	Ring indicator. $\overline{RI}$ is a modem status signal. Its condition can be checked by reading bit 6 (RI) of the modem status register. Bit 2 (TERI) of the modem status register indicates that the $\overline{RI}$ input has transitioned from a low to a high state since the last read from the modem status register. If the modem status interrupt is enabled when this transition occurs, an interrupt is generated.
$\overline{RTS}$	32 [36]	O	Request to send. When active, $\overline{RTS}$ informs the modem or data set that the ACE is ready to transmit data. $\overline{RTS}$ is set to its active state by setting the RTS modem control register bit, and is set to its inactive (high) state either as a result of a master reset or during loop mode operations or by clearing bit 1 (RTS) of the modem control register.
$\overline{RXRDY}$	29 [32]	O	Receiver ready output. Receiver direct memory access (DMA) signalling is available with $\overline{RXRDY}$. When operating in the FIFO mode, one of two types of DMA signalling can be selected with FCR3. When operating in the TL16C450 mode, only DMA mode 0 is allowed. Mode 0 supports single-transfer DMA in which a transfer is made between CPU bus cycles. Mode 1 supports multitransfer DMA in which multiple transfers are made continuously until the receiver FIFO has been emptied. In DMA mode 0 (FCR0 = 0 or FCR0 = 1, FCR3 = 0), if there is at least 1 character in the receiver FIFO or receiver holding register, $\overline{RXRDY}$ is active (low). When RXRDY has been active but there are no characters in the FIFO or holding register, $\overline{RXRDY}$ goes inactive (high). In DMA mode 1 (FCR0 = 1, FCR3 = 1), when the trigger level or the timeout has been reached, $\overline{RXRDY}$ goes active (low); when it has been active but there are no more characters in the FIFO or holding register, it goes inactive (high).
SIN	10 [11]	I	Serial input. SIN is a serial data input from a connected communications device.
SOUT	11 [13]	O	Serial output. SOUT is a composite serial data output to a connected communication device. SOUT is set to the marking (high) state as a result of master reset.
$\overline{TXRDY}$	24 [27]	O	Transmitter ready output. Transmitter DMA signalling is available with $\overline{TXRDY}$. When operating in the FIFO mode, one of two types of DMA signalling can be selected with FCR3. When operating in the TL16C450 mode, only DMA mode 0 is allowed. Mode 0 supports single-transfer DMA in which a transfer is made between CPU bus cycles. Mode 1 supports multitransfer DMA in which multiple transfers are made continuously until the transmit FIFO has been filled.
V_{CC}	40 [44]		5-V supply voltage
V_{SS}	20 [22]		Supply common
$\overline{WR1}$ WR2	18 [20] 19 [21]	I	Write inputs. When either $\overline{WR1}$ or WR2 are active (high or low respectively) while the ACE is selected, the CPU is allowed to write control words or data into a selected ACE register. Only one of these inputs is required to transfer data during a write operation; the other input should be tied in its inactive state (i.e., WR2 tied low or $\overline{WR1}$ tied high).
XIN XOUT	16 [18] 17 [19]	I/O	External clock. XIN and XOUT connect the ACE to the main timing reference (clock or crystal).

† Terminal numbers shown in brackets are for the FN package.

absolute maximum ratings over free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Input voltage range at any input, V_I ..... −0.5 V to 7 V
Output voltage range, V_O ..... −0.5 V to 7 V
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Case temperature for 10 seconds, T_C: FN package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2		V_{CC}	V
Low-level input voltage, V_{IL}	−0.5		0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}‡	High-level output voltage	I_{OH} = −1 mA	2.4			V
V_{OL}‡	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
I_{lkg}	Input leakage current	V_{CC} = 5.25 V, V_{SS} = 0, V_I = 0 to 5.25 V, All other terminals floating			±10	μA
I_{OZ}	High-impedance output current	V_{CC} = 5.25 V, V_{SS} = 0, V_O = 0 to 5.25 V, Chip selected in write mode or chip deselected			±20	μA
I_{CC}	Supply current	V_{CC} = 5.25 V, T_A = 25°C, SIN, $\overline{DSR}$, $\overline{DCD}$, $\overline{CTS}$, and $\overline{RI}$ at 2 V, All other inputs at 0.8 V, XTAL1 at 4 MHz, No load on outputs, Baud rate = 50 kbit/s			10	mA
C_{XIN}	Clock input capacitance	V_{CC} = 0, V_{SS} = 0, All other terminals grounded, f = 1 MHz, T_A = 25°C		15	20	pF
C_{XOUT}	Clock output capacitance			20	30	pF
C_i	Input capacitance			6	10	pF
C_o	Output capacitance			10	20	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ These parameters apply for all outputs except XOUT.

system timing requirements over recommended ranges of supply voltage and operating free-air temperature

		ALT. SYMBOL	FIGURE	MIN	MAX	UNIT
t_{cR}	Cycle time, read ($t_{w7} + t_{d8} + t_{d9}$)	RC		175		ns
t_{cW}	Cycle time, write ($t_{w6} + t_{d5} + t_{d6}$)	WC		175		ns
t_{w5}	Pulse duration, $\overline{ADS}$ low	t_{ADS}	2, 3	15		ns
t_{w6}	Pulse duration, write strobe	t_{WR}	2	80		ns
t_{w7}	Pulse duration, read strobe	tRD	3	80		ns
t_{w8}	Pulse duration, master reset	t_{MR}		1		ns
t_{su1}	Setup time, address valid before $\overline{ADS}\uparrow$	t_{AS}	2, 3	15		ns
t_{su2}	Setup time, CS before $\overline{ADS}\uparrow$	t_{CS}	2, 3	15		ns
t_{su3}	Setup time, data valid before $\overline{WR1}\downarrow$ or WR2$\uparrow$	t_{DS}	2	15		ns
t_{h1}	Hold time, address low after $\overline{ADS}\uparrow$	t_{AH}	2, 3	0		ns
t_{h2}	Hold time, CS valid after $\overline{ADS}\uparrow$	t_{CH}	2, 3	0		ns
t_{h3}	Hold time, CS valid after $\overline{WR1}\uparrow$ or WR2$\downarrow$	t_{WCS}	2	20		ns
t_{h4}§	Hold time, address valid after $\overline{WR1}\uparrow$ or WR2$\downarrow$	t_{WA}	2	20		ns
t_{h5}	Hold time, data valid after $\overline{WR1}\uparrow$ or WR2$\downarrow$	t_{DH}	2	15		ns
t_{h6}	Hold time, CS valid after $\overline{RD1}\uparrow$ or RD2$\downarrow$	t_{RCS}	3	20		ns
t_{h7}§	Hold time, address valid after $\overline{RD1}\uparrow$ or RD2$\downarrow$	t_{RA}	3	20		ns
t_{d4}§	Delay time, CS valid before $\overline{WR1}\downarrow$ or WR2$\uparrow$	t_{CSW}	2	15		ns
t_{d5}§	Delay time, address valid before $\overline{WR1}\downarrow$ or WR2$\uparrow$	t_{AW}	2	15		ns
t_{d6}§	Delay time, write cycle, $\overline{WR1}\uparrow$ or WR2$\downarrow$ to $\overline{ADS}\downarrow$	t_{WC}	2	80		ns
t_{d7}§	Delay time, CS valid to $\overline{RD1}\downarrow$ or RD2$\uparrow$	t_{CSR}	3	15		ns
t_{d8}§	Delay time, address valid to $\overline{RD1}\downarrow$ or RD2$\uparrow$	t_{AR}	3	15		ns
t_{d9}	Delay time, read cycle, $\overline{RD1}\uparrow$ or RD2$\downarrow$ to $\overline{ADS}\downarrow$	tRC	3	80		ns

§ Applicable only when $\overline{ADS}$ is tied low.

system switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 2)

	PARAMETER	ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{w1}	Pulse duration, clock high	t_{XH}	1	f = 9 MHz maximum	50		ns
t_{w2}	Pulse duration, clock low	t_{XL}	1	f = 9 MHz maximum	50		ns
t_{d10}	Delay time, $\overline{RD1}\downarrow$ or RD2$\uparrow$ to data valid	t_{RVD}	3	C_L = 100 pF		60	ns
t_{d11}	Delay time, $\overline{RD1}\uparrow$ or RD2$\downarrow$ to floating data	t_{HZ}	3	C_L = 100 pF	0	60	ns
$t_{dis(R)}$	Disable time, $\overline{RD1}\downarrow\uparrow$ or RD2$\uparrow\downarrow$ to DDIS$\uparrow\downarrow$	t_{RDD}	3	C_L = 100 pF		60	ns

NOTE 2: Charge and discharge time is determined by V_{OL}, V_{OH}, and external loading.

baud generator switching characteristics over recommended ranges of supply voltage and operating free-air temperature

	PARAMETER	ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{w3}	Pulse duration, $\overline{BAUDOUT}$ low	t_{LW}	1	f = 9 MHz, CLK ÷ 2, C_L = 100 pF	80		ns
t_{w4}	Pulse duration, $\overline{BAUDOUT}$ high	t_{HW}	1	f = 9 MHz, CLK ÷ 2, C_L = 100 pF	100		ns
t_{d1}	Delay time, XIN$\uparrow$ to $\overline{BAUDOUT}\uparrow$	t_{BLD}	1	C_L = 100 pF		125	ns
t_{d2}	Delay time, XIN$\uparrow\downarrow$ to $\overline{BAUDOUT}\downarrow$	t_{BHD}	1	C_L = 100 pF		125	ns

receiver switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 3)

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d12}	Delay time, RCLK to sample clock	t_{SCD}	4			100	ns
t_{d13}	Delay time, stop to set RCV error interrupt or read RBR to LSI interrupt or stop to $\overline{RXRDY}\downarrow$	t_{SINT}	4,5,6,7,8			1	RCLK cycles
t_{d14}	Delay time, read RBR/LSR to reset interrupt	t_{RINT}	4,5,6,7,8	C_L = 100 pF		150	ns

NOTE 3: In FIFO mode RC = 425 ns (minimum) between reads of the receiver FIFO and the status registers (interrupt identification register or line status register).

transmitter switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d15}	Delay time, INTRPT to transmit start	t_{IRS}	9		8	24	baudout cycles
t_{d16}	Delay time, start to interrupt	t_{STI}	9		8	8	baudout cycles
t_{d17}	Delay time, WR THR to reset interrupt	t_{HR}	9	C_L = 100 pF		140	ns
t_{d18}	Delay time, initial write to interrupt (THRE)	t_{SI}	9		16	32	baudout cycles
t_{d19}	Delay time, read IIR to reset interrupt (THRE)	t_{IR}	9	C_L = 100 pF		140	ns
t_{d20}	Delay time, write to TXRDY inactive	t_{WXI}	10,11	C_L = 100 pF		195	ns
t_{d21}	Delay time, start to TXRDY active	t_{SXA}	10,11	C_L = 100 pF		8	baudout cycles

modem control switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d22}	Delay time, WR MCR to output	t_{MDO}	12	C_L = 100 pF		100	ns
t_{d23}	Delay time, modem interrupt to set interrupt	t_{SIM}	12	C_L = 100 pF		170	ns
t_{d24}	Delay time, RD MSR to reset interrupt	t_{RIM}	12	C_L = 100 pF		140	ns

PARAMETER MEASUREMENT INFORMATION

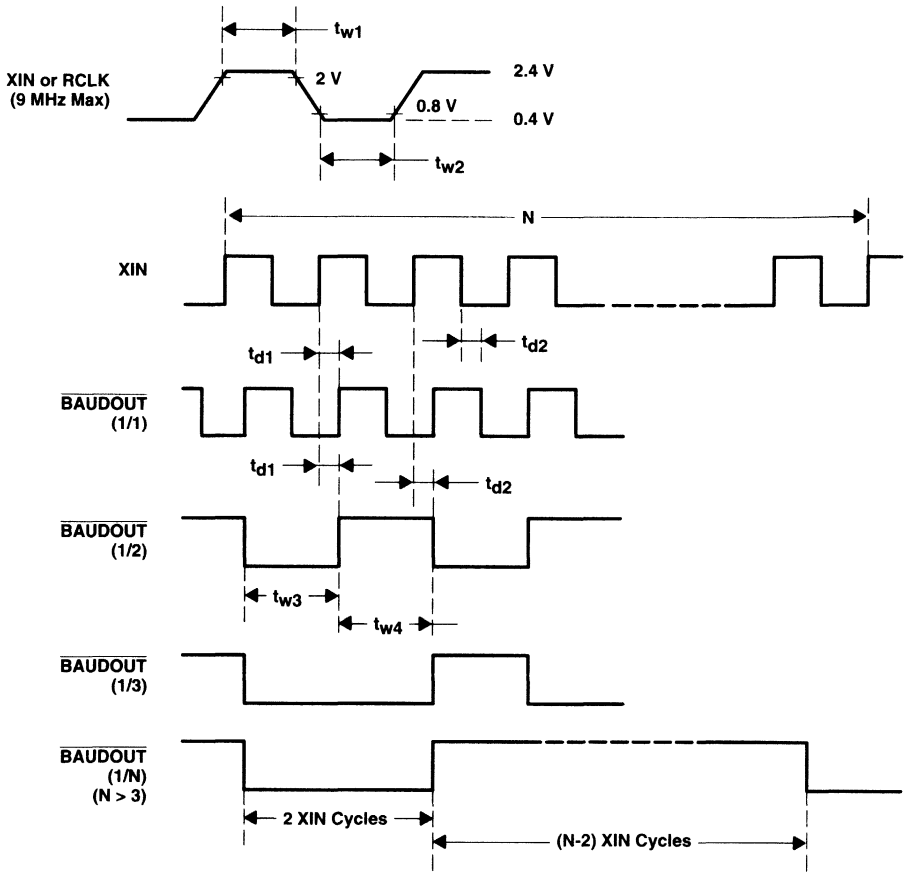
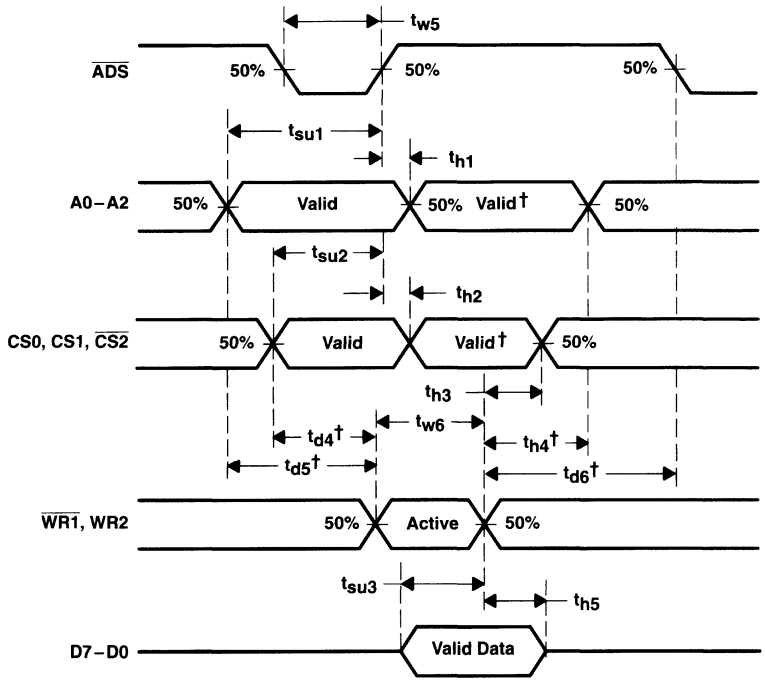


Figure 1. Baud Generator Timing Waveforms

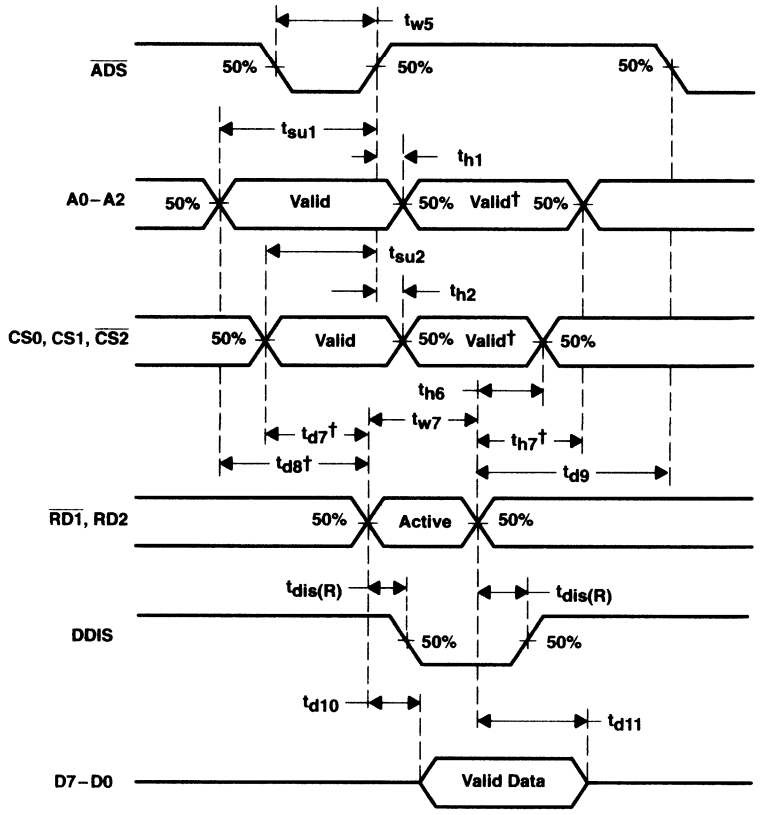
PARAMETER MEASUREMENT INFORMATION



† Applicable only when $\overline{ADS}$ is tied low.

Figure 2. Write Cycle Timing Waveforms

PARAMETER MEASUREMENT INFORMATION



† Applicable only when ADS is tied low.

Figure 3. Read Cycle Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

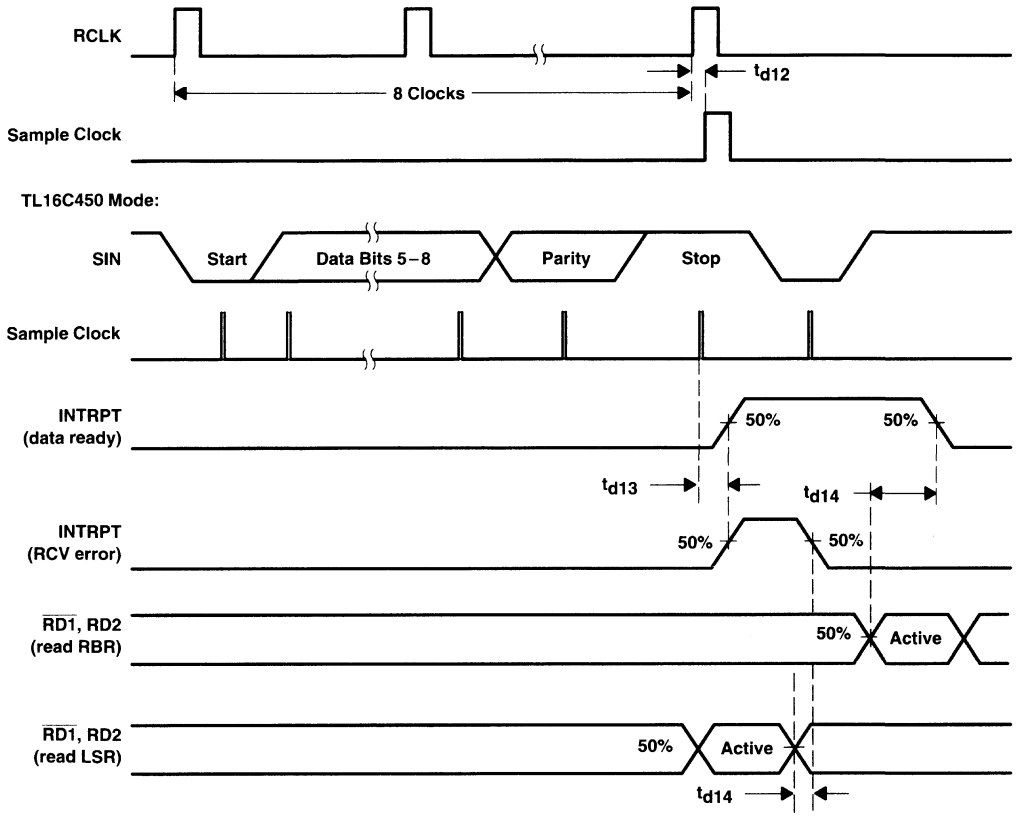
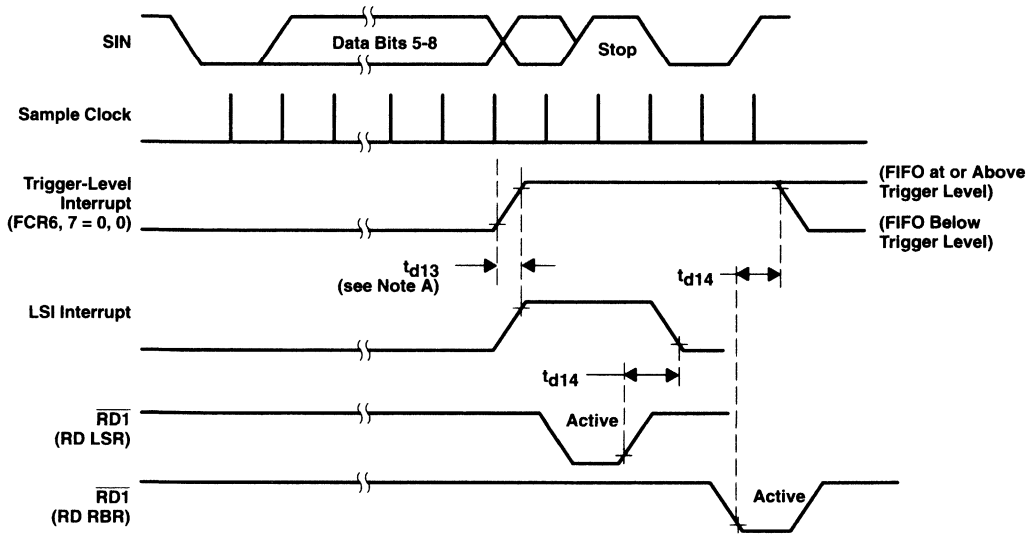


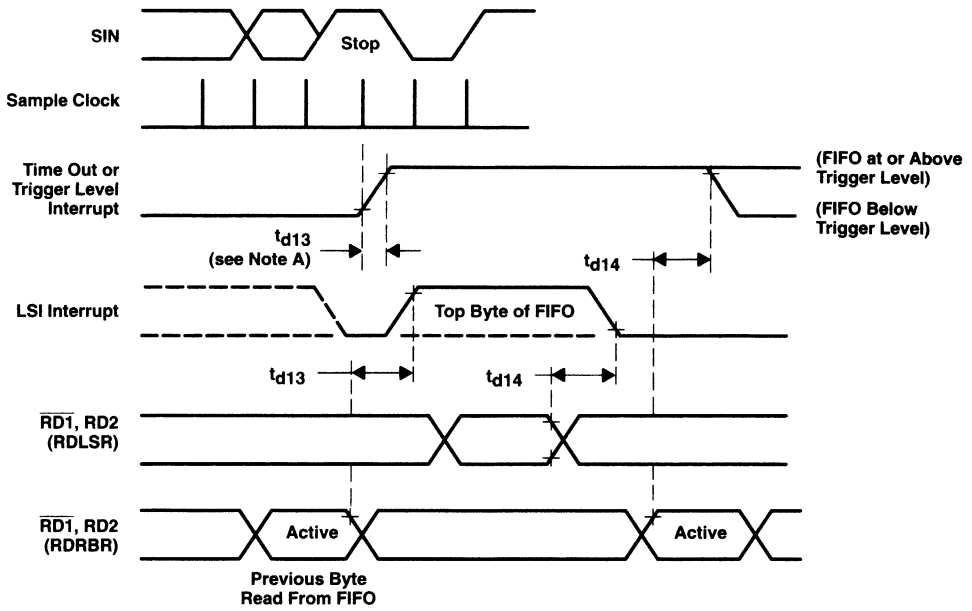
Figure 4. Receiver Timing Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: For a timeout interrupt, t_{d13} = 8 RCLKs.

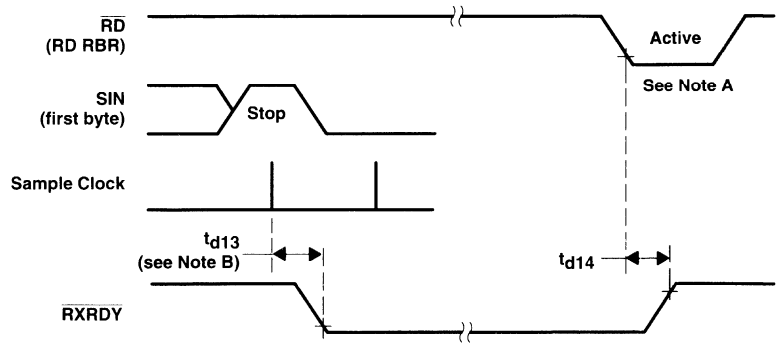
Figure 5. Receiver FIFO First Byte (Sets DR Bit) Waveforms



NOTE A: For a timeout interrupt, t_{d13} = 8 RCLKs.

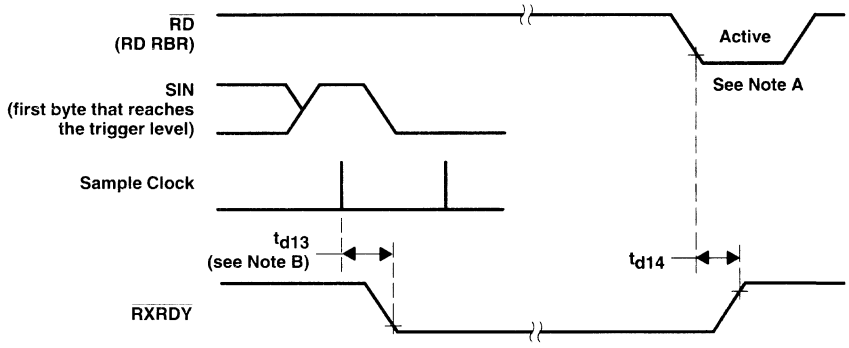
Figure 6. Receiver FIFO Bytes Other Than the First Byte (DR Internal Bit Already Set) Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. This is the reading of the last byte in the FIFO.
B. For a timeout interrupt, t_{d13} = 8 RCLKs.

Figure 7. Receiver Ready ($\overline{RXRDY}$) Waveforms, FCR0 = 0 or FCR0 = 1 and FCR3 = 0 (mode 0)



NOTES: A. This is the reading of the last byte in the FIFO.
B. For a timeout interrupt, t_{d13} = 8 RCLKs.

Figure 8. Receiver Ready ($\overline{RXRDY}$) Waveforms, FCR = 1 or FCR3 = 1 (mode 1)

PARAMETER MEASUREMENT INFORMATION

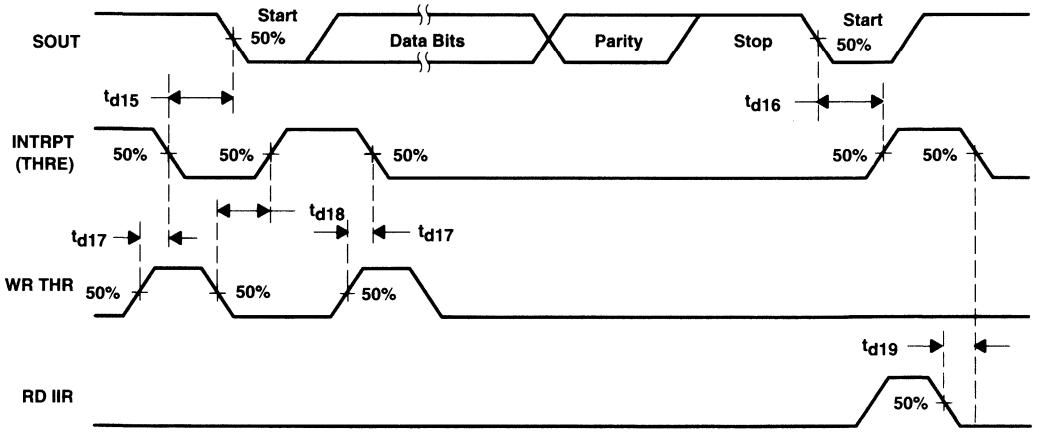


Figure 9. Transmitter Timing Waveforms

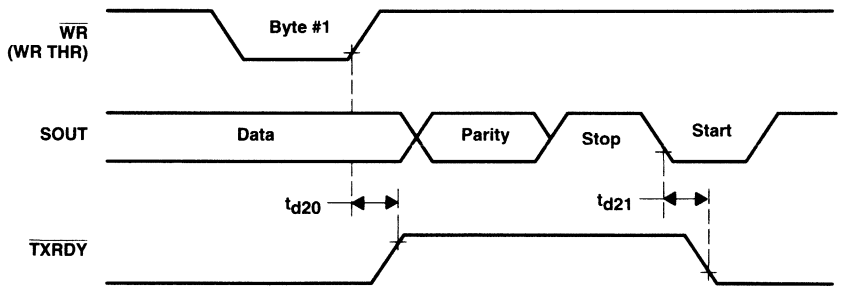


Figure 10. Transmitter Ready ($\overline{\text{TXRDY}}$) Waveforms, FCR0 = 0 or FCR0 = 1 and FCR3 = 0 (mode 0)

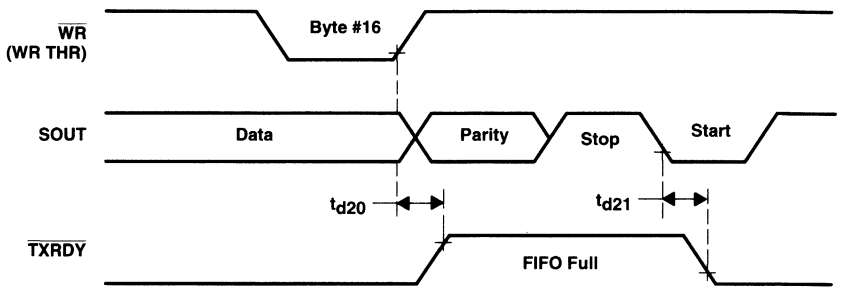


Figure 11. Transmitter Ready ($\overline{\text{TXRDY}}$) Waveforms, FCR0 = 1 and FCR3 = 1 (mode 1)

PARAMETER MEASUREMENT INFORMATION

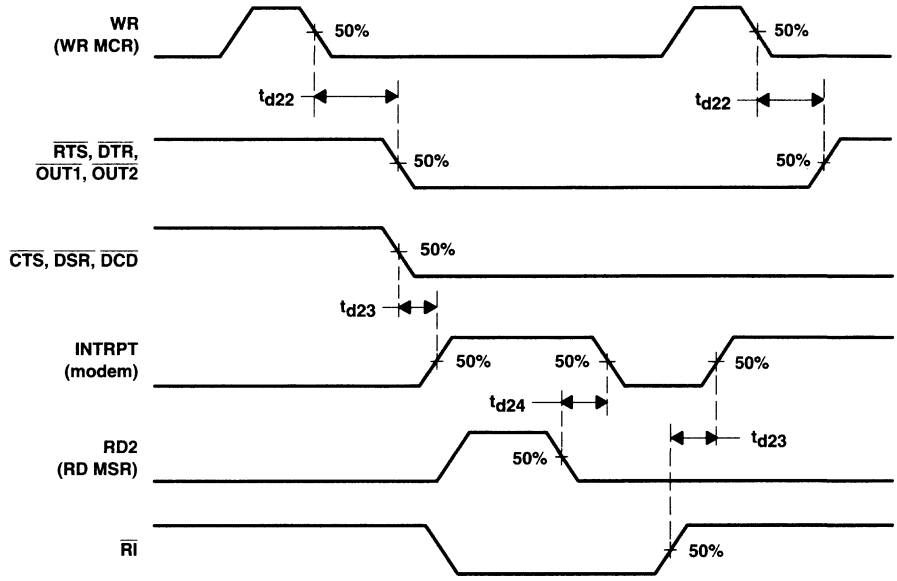


Figure 12. Modem Control Timing Waveforms

APPLICATION INFORMATION

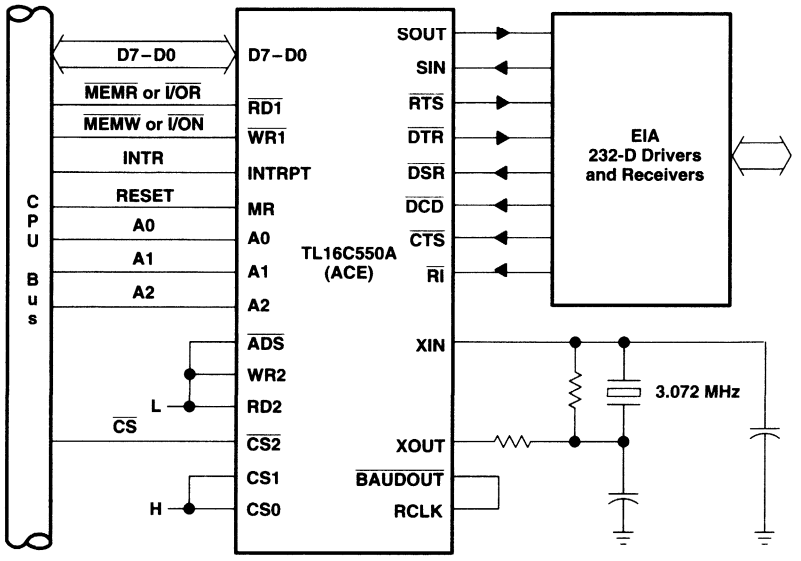


Figure 13. Basic TL16C550A Configuration

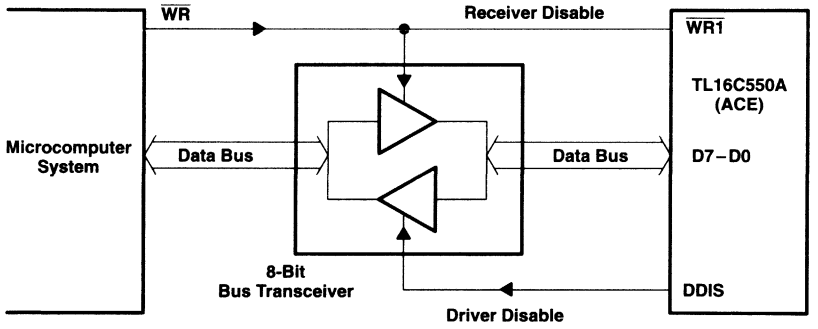
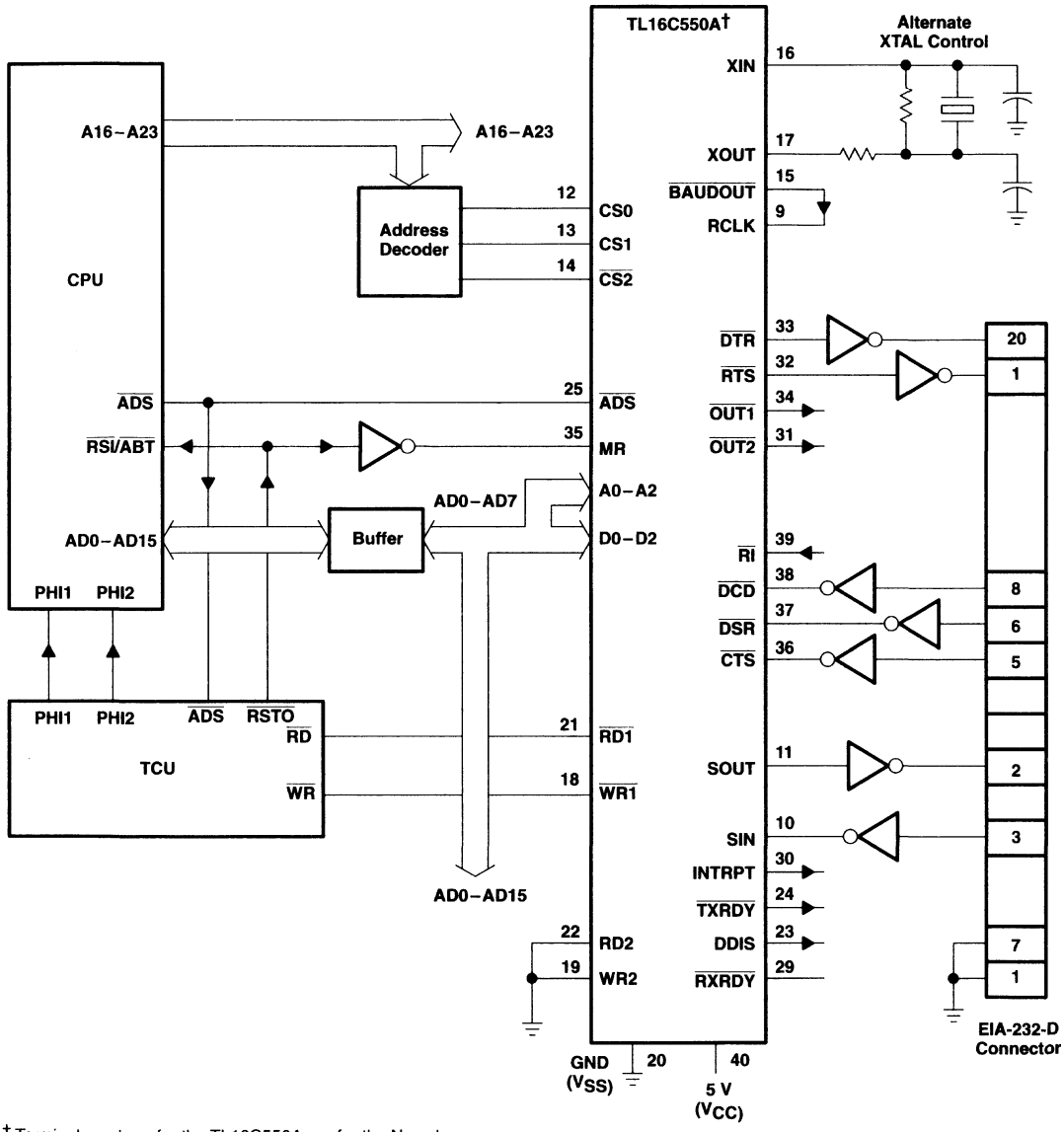


Figure 14. Typical Interface for a High-Capacity Data Bus

APPLICATION INFORMATION



† Terminal numbers for the TL16C550A are for the N package.

Figure 15. Typical TL16C550A Connection to a CPU

PRINCIPLES OF OPERATION

Table 1. Register Selection

DLAB†	A2	A1	A0	REGISTER
0	L	L	L	Receiver buffer (read), transmitter holding register (write)
0	L	L	H	Interrupt enable register
X	L	H	L	Interrupt identification register (read only)
X	L	H	L	FIFO control register (write)
X	L	H	H	Line control register
X	H	L	L	Modem control register
X	H	L	H	Line status register
X	H	H	L	Modem status register
X	H	H	H	Scratch register
1	L	L	L	Divisor latch (LSB)
1	L	L	H	Divisor latch (MSB)

† The divisor latch access bit (DLAB) is the most significant bit of the line control register. The DLAB signal is controlled by writing to this bit location (see Table 3).

Table 2. ACE Reset Functions

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	Master Reset	All bits cleared (0–3 forced and 4–7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is set, bits 1–3 are cleared, and bits 4–7 are permanently cleared
FIFO Control Register	Master Reset	All bits cleared
Line Control Register	Master Reset	All bits cleared
Modem Control Register	Master Reset	All bits cleared (5–7 permanent)
Line Status Register	Master Reset	Bits 5 and 6 are set, all other bits are cleared
Modem Status Register	Master Reset	Bits 0–3 are cleared, bits 4–7 are input signals
SOUT	Master Reset	High
INTRPT (receiver error flag)	Read LSR/MR	Low
INTRPT (received data available)	Read RBR/MR	Low
INTRPT (transmitter holding register empty)	Read IR/Write THR/MR	Low
INTRPT (modem status changes)	Read MSR/MR	Low
$\overline{OUT2}$	Master Reset	High
$\overline{RTS}$	Master Reset	High
$\overline{DTR}$	Master Reset	High
$\overline{OUT1}$	Master Reset	High
Scratch Register	Master Reset	No effect
Divisor Latch (LSB and MSB) Registers	Master Reset	No effect
Receiver Buffer Registers	Master Reset	No effect
Transmitter Holding Registers	Master Reset	No effect
RCVR FIFO	MR/FCR1-FCR0/ ΔFCR0	All bits low
XMIT FIFO	MR/FCR2-FCR0/ ΔFCR0	All bits low

PRINCIPLES OF OPERATION

accessible registers

The system programmer, using the CPU, has access to and control over any of the ACE registers that are summarized in Table 3. These registers control ACE operations, receive data, and transmit data. Descriptions of these registers follow Table 3.

Table 3. Summary of Accessible Registers

Bit No.	REGISTER ADDRESS											
	0 DLAB = 0	0 DLAB = 0	1 DLAB = 0	2	2	3	4	5	6	7	0 DLAB = 1	1 DLAB = 1
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident. Register (Read Only)	FIFO Control Register (Write Only)	Line Control Register	Modem Control Register	Line Status Register	Modem Status Register	Scratch Register	Divisor Latch (LSB)	Latch (MSB)
	RBR	THR	IER	IIR	FCR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Data Bit 0†	Data Bit 0	Enable Received Data Available Interrupt (ERB)	"0" If Interrupt Pending	FIFO Enable	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (ΔCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit 0	Receiver FIFO Reset	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (ΔDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Transmitter FIFO Reset	Number of Stop Bits (STB)	Out1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable Modem Status Interrupt (EDSSI)	Interrupt ID Bit (2) (Note 4)	DMA Mode Select	Parity Enable (PEN)	Out2	Framing Error (FE)	Delta Data Carrier Detect (ΔDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	FIFOs Enabled (Note 4)	Receiver Trigger (LSB)	Set Break	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	FIFOs Enabled (Note 4)	Receiver Trigger (MSB)	Divisor Latch Access Bit (DLAB)	0	Error in RCVR FIFO (Note 4)	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

† Bit 0 is the least significant bit. It is the first bit serially transmitted or received.
NOTE 4: These bits are always cleared in the TL16C450 mode.

PRINCIPLES OF OPERATION

FIFO control register (FCR)

The FCR is a write-only register at the same location as the IIR, which is a read-only register. The FCR enables the FIFOs, clears the FIFOs, sets the receiver FIFO trigger level, and selects the type of DMA signalling.

- Bit 0: This bit (FCR0), when set, enables the transmit and receive FIFOs. Bit 0 must be set when other FCR bits are written to or they are not programmed. Changing this bit clears the FIFOs.
- Bit 1: This bit (FCR1), when set, clears all bytes in the receiver FIFO and clears its counter. The shift register is not cleared. The 1 that is written to this bit position is self clearing.
- Bit 2: This bit (FCR2), when set, clears all bytes in the transmit FIFO and clears its counter. The shift register is not cleared. The 1 that is written to this bit position is self clearing.
- Bit 3: When this bit (FCR0) and FCR3 are set, $\overline{\text{RXRDY}}$ and $\overline{\text{TXRDY}}$ change from mode 0 to mode 1.
- Bits 4 and 5: These two bits (FCR4 and FCR5) are reserved for future use.
- Bits 6 and 7: These two bits (FCR6 and FCR7) set the trigger level for the receiver FIFO interrupt. Table 4 shows the trigger level for the receiver FIFO interrupt.

Table 4. Receiver FIFO Trigger Level

BIT 7	BIT 6	RECEIVER FIFO TRIGGER LEVEL (BYTES)
0	0	01
0	1	04
1	0	08
1	1	14

FIFO interrupt mode operation

When the receiver FIFO and receiver interrupts are enabled (FCR0 = 1, IER0 = 1) receiver interrupts occur as follows:

1. The receive data available interrupt is issued to the microprocessor when the FIFO has reached its programmed trigger level. It is cleared as soon as the FIFO drops below its programmed trigger level.
2. The IIR receive data available indication also occurs when the FIFO trigger level is reached, and, like the interrupt, it is cleared when the FIFO drops below the trigger level.
3. The receiver line status interrupt (IIR = 06), as before, has higher priority than the received data available (IIR = 04) interrupt.
4. The data ready bit (LSR0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is cleared when the FIFO is empty.

When the receiver FIFO and receiver interrupts are enabled, receiver FIFO timeout interrupts occur as follows:

PRINCIPLES OF OPERATION

FIFO interrupt mode operation (continued)

1. FIFO timeout interrupt occurs when the following conditions exist:
   a. At least one character is in the FIFO.
   b. The most recent serial character received was longer than 4 continuous character times ago (when 2 stop bits are programmed, the second one is included in this time delay).
   c. The most recent microprocessor read of the FIFO was longer than 4 continuous character times ago. This causes a maximum character received to interrupt issued delay of 160 ms at 300 baud with 12-bit characters.
2. Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baud rate).
3. When a timeout interrupt has occurred, it is cleared and the timer reset when the microprocessor reads one character from the receiver FIFO.
4. When a timeout interrupt has not occurred, the timeout timer is reset after a new character is received or after the microprocessor reads the receiver FIFO.

When the transmit FIFO and transmitter interrupts are enabled (FCR0 = 1, IER1 = 1), transmit interrupts occur as follows:

1. The THR interrupt (02) occurs when the transmit FIFO is empty. It is cleared as soon as the THR is written to (1 to 16 characters may be written to the transmit FIFO while servicing this interrupt) or the IIR is read.
2. The transmit FIFO empty indications are delayed 1 character time minus the last stop bit time when the following occurs: THRE = 1 and there have not been at least two bytes at the same time in the transmit FIFO since the last THRE = 1. The first transmitter interrupt after changing FCR0 is immediate, if it is enabled.

Character timeout interrupt and receiver FIFO trigger level interrupts have the same priority as the current received data available interrupt. The transmit FIFO empty interrupt has the same priority as the current THRE interrupt.

FIFO polled mode operation

When FCR0 is set, clearing IER0, IER1, IER2, IER3, or all four puts the ACE in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately, either one or both can be in the polled mode of operation.

In this mode, the user program checks the receiver and transmitter status using the LSR.

- LSR0 is set as long as there is one byte in the receiver FIFO.
- LSR1 – LSR4 specify which error(s) have occurred. Character error status is handled the same way as when in the interrupt mode and the IIR is not affected since IER2 = 0.
- LSR5 indicates when the transmit FIFO is empty.
- LSR6 indicates that both the transmit FIFO and shift registers are empty.
- LSR7 indicates whether there are any errors in the receiver FIFO.

There is no trigger level reached or timeout conditions indicated in the FIFO polled mode. However, the receiver and transmitter FIFOs are still fully capable of holding characters.

PRINCIPLES OF OPERATION

interrupt enable register (IER)

The IER enables each of the four types of interrupts (refer to Table 5) and the INTRPT output signal in response to an interrupt generation. The IER can also disable the interrupt system by clearing bits 0 through 3. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bit 0: This bit, when set, enables the received data available interrupt.
- Bit 1: This bit, when set, enables the THRE interrupt.
- Bit 2: This bit, when set, enables the receiver line status interrupt.
- Bit 3: This bit, when set, enables the modem status interrupt.
- Bits 4 – 7: These bits in the IER are not used and are always cleared.

interrupt identification register (IIR)

The ACE has an on-chip interrupt generation and prioritization capability that permits a flexible interface with most popular microprocessors.

The ACE provides four prioritized levels of interrupts:

- Priority 1 – Receiver line status (highest priority)
- Priority 2 – Receiver data ready or receiver character time out
- Priority 3 – Transmitter holding register empty
- Priority 4 – Modem status (lowest priority)

When an interrupt is generated, the IIR indicates that an interrupt is pending and the type of interrupt is defined by the interrupt's three least significant bits (bits 0, 1, and 2). The contents of this register are summarized in Table 3 and described in Table 4. Details of each bit are as follows:

- Bit 0: This bit can be used either in a hardwire prioritized or polled interrupt system. When this bit is cleared, an interrupt is pending. When bit 0 is set, no interrupt is pending.
- Bits 1 and 2: These two bits identify the highest priority interrupt pending as indicated in Table 5.
- Bit 3: This bit is always cleared in the TL16C450 mode. In FIFO mode, this bit is set with bit 2 to indicate that a timeout interrupt is pending.
- Bits 4 thru 5: These two bits are not used and are always cleared.
- Bits 6 and 7: These two bits are always cleared in the TL16C450 mode. They are set when bit 0 of the FCR is set.

PRINCIPLES OF OPERATION

interrupt identification register (IIR) (continued)

Table 5. Interrupt Control Functions

INTERRUPT IDENTIFICATION REGISTER (IIR)				PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET METHOD
BIT 3	BIT 2	BIT 1	BIT 0				
0	0	0	1	None	None	None	–
0	1	1	0	1	Receiver line status	Overrun error, parity error, framing error, or break interrupt	Reading the line status register (LSR)
0	1	0	0	2	Received data available	Receiver data available in the TL16C450 mode or trigger level reached in the FIFO mode.	Reading the receiver buffer register (RBR)
1	1	0	0	2	Character timeout indication	No characters have been removed from or input to the receiver FIFO during the last four character times and there is at least one character in it during this time	Reading the receiver buffer register (RBR)
0	0	1	0	3	Transmitter holding register empty	Transmitter holding register empty	Reading the interrupt identification register (IIR) (if source of interrupt) or writing into the transmitter holding register (THR)
0	0	0	0	4	Modem status	Clear to send, data set ready, ring indicator, or data carrier detect	Reading the modem status register (MSR)

line control register (LCR)

The system programmer controls the format of the asynchronous data communication exchange through the LCR. In addition, the programmer is able to retrieve, inspect, and modify the contents of the LCR; this eliminates the need for separate storage of the line characteristics in system memory. The contents of this register are summarized in Table 3 and described in the following bulleted list.

- Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. These bits are encoded as shown in Table 6.

Table 6. Serial Character Word Length

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

- Bit 2: This bit specifies either one, one and one-half, or two stop bits in each transmitted character. When bit 2 is cleared, one stop bit is generated in the data. When bit 2 is set, the number of stop bits generated is dependent on the word length selected with bits 0 and 1. The receiver clocks the first stop bit only, regardless of the number of stop bits selected. The number of stop bits generated, in relation to word length and bit 2, is shown in Table 7.

PRINCIPLES OF OPERATION

line control register (LCR) (continued)

Table 7. Number of Stop Bits Generated

Bit 2	Word Length Selected by Bits 1 and 2	Number of Stop Bits Generated
0	Any word length	1
1	5 bits	1 1/2
1	6 bits	2
1	7 bits	2
1	8 bits	2

- Bit 3: This bit is the parity enable bit. When bit 3 is set, a parity bit is generated in the transmitted data between the last data word bit and the first stop bit. In received data, when bit 3 is set, parity is checked. When bit 3 is cleared, no parity is generated or checked.
- Bit 4: This bit is the even parity select bit. When parity is enabled (bit 3 is set) and bit 4 is set, even parity (an even number of logic 1's in the data and parity bits) is selected. When parity is enabled and bit 4 is cleared, odd parity (an odd number of logic 1s) is selected.
- Bit 5: This is the stick parity bit. When bits 3, 4, and 5 are set, the parity bit is transmitted and checked as cleared. When bits 3 and 5 are set and bit 4 is cleared, the parity bit is transmitted and checked as set. When bit 5 is cleared, stick parity is disabled.
- Bit 6: This bit is the break control bit. Bit 6 is set to force a break condition, i.e., a condition where the serial output (SOUT) terminal is forced to the spacing (low) state. When bit 6 is cleared, the break condition is disabled. The break condition has no affect on the transmitter logic; it only affects the serial output.
- Bit 7: This bit is the divisor latch access bit (DLAB). Bit 7 must be set to access the divisor latches of the baud generator during a read or write. Bit 7 must be cleared during a read or write to access the receiver buffer, the THR, or the IER.

line status register (LSR)†

The LSR provides information to the CPU concerning the status of data transfers. The contents of this register are described in the following bulleted list and summarized in Table 3.

- Bit 0: This bit is the data ready (DR) indicator for the receiver. Bit 0 is set whenever a complete incoming character has been received and transferred into the RBR or the FIFO and is cleared by reading all of the data in the RBR or the FIFO.
- Bit 1‡: This bit is the overrun error (OE) indicator. When bit 1 is set, it indicates that before the character in the RBR was read, it was overwritten by the next character transferred into the register. The OE indicator is cleared every time the CPU reads the contents of the LSR. If the FIFO mode data continues to fill the FIFO beyond the trigger level, an overrun error occurs only after the FIFO is full and the next character has been completely received in the shift register. OE is indicated to the CPU as soon as it happens. The character in the shift register is overwritten but is not transferred to the FIFO.

† The line status register is intended for read operations only; writing to this register is not recommended outside of a factory testing environment
‡ Bits 1 through 4 are the error conditions that produce a receiver line status Interrupt.

PRINCIPLES OF OPERATION

line status register (LSR)† (continued)

- Bit 2‡: This bit is the parity error (PE) indicator. When bit 2 is set, it indicates that the parity of the received data character does not match the parity selected in the LCR (bit 4). The PE bit is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO.
- Bit 3‡: This bit is the framing error (FE) indicator. When bit 3 is set, it indicates that the received character did not have a valid (set) stop bit. The FE bit is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. The ACE tries to resynchronize after a framing error. To accomplish this, it is assumed that the framing error is due to the next start bit. The ACE then samples this start bit twice and then accepts the input data.
- Bit 4‡: This bit is the break interrupt (BI) indicator. When bit 4 is set, it indicates that the received data input was held clear for longer than a full-word transmission time. A full-word transmission time is defined as the total time of the start, data, parity, and stop bits. The BI bit is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. When break occurs, only the 0 character is loaded into the FIFO. The next character transfer is enabled after SIN goes to the marking state and receives the next valid start bit.
- Bit 5: This bit is the THRE indicator. Bit 5 is set when the THR is empty, indicating that the ACE is ready to accept a new character. If the THRE interrupt is enabled when the THRE bit is set, then an interrupt is generated. THRE is set when the contents of the THR are transferred to the transmitted shift register. This bit is cleared concurrent with the loading of the THR by the CPU. In the FIFO mode, this bit is set when the transmit FIFO is empty; it is cleared when at least 1 byte is written to the transmit FIFO.
- Bit 6: This bit is the transmitter empty (TEMT) indicator. Bit 6 is set when the THR and the TSR are both empty. When either the THR or the TSR contains a data character, the TEMT bit is cleared. In the FIFO mode, this bit is set when the transmitter FIFO and shift register are both empty.
- Bit 7: In the TL16C550A, this bit is always cleared. In the TL16C450 mode, this bit is cleared. In the FIFO mode, LSR7 is set when there is at least one parity, framing, or break error in the FIFO. It is cleared when the microprocessor reads the LSR and there are no subsequent errors in the FIFO.

modem control register (MCR)

The MCR is an 8-bit register that controls an interface with a modem, data set, or peripheral device that is emulating a modem. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bit 0: This bit (DTR) controls the data terminal ready ($\overline{DTR}$) output. Setting bit 0 forces the $\overline{DTR}$ output to its low state. When bit 0 is cleared, $\overline{DTR}$ goes high.
- Bit 1: This bit (RTS) controls the request to send ($\overline{RTS}$) output in a manner identical to bit 0's control over the $\overline{DTR}$ output.
- Bit 2: This bit (OUT1) controls the output 1 ($\overline{OUT1}$) signal, a user-designated output signal, in a manner identical to bit 0's control over the $\overline{DTR}$ output.

† The line status register is intended for read operations only; writing to this register is not recommended outside of a factory testing environment
‡ Bits 1 through 4 are the error conditions that produce a receiver line status interrupt.

PRINCIPLES OF OPERATION

modem control register (MCR) (continued)

- Bit 3: This bit (OUT2) controls the output 2 ($\overline{OUT2}$) signal, a user-designated output signal, in a manner identical to bit 0's control over the $\overline{DTR}$ output.
- Bit 4: This bit provides a local loopback feature for diagnostic testing of the ACE. When bit 4 is set, the following occurs:

  1. The SOUT is set high.
  2. The SIN is disconnected.
  3. The output of the TSR is looped back into the RSR input.
  4. The four modem control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$) are disconnected.
  5. The four modem control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT1}$, and $\overline{OUT2}$) are internally connected to the four modem control inputs.
  6. The four modem control output terminals are forced to their inactive states (high).

  In the diagnostic mode, data that is transmitted is immediately received. This allows the processor to verify the transmit and receive data paths to the ACE. The receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational but the modem control interrupt's sources are now the lower four bits of the MCR instead of the four modem control inputs. All interrupts are still controlled by the IER.

- Bit 5 – 7: These bits are permanently cleared.

modem status register (MSR)

The MSR is an 8-bit register that provides information about the current state of the control lines from the modem, data set, or peripheral device to the CPU. Additionally, four bits of this register provide change information; when a control input from the modem changes state, the appropriate bit is set. All four bits are cleared when the CPU reads the MSR. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bit 0: This bit is the change in clear to send (ΔCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input has changed states since the last time it was read by the CPU . When this bit is set and the modem status interrupt is enabled, a modem status interrupt is generated.
- Bit 1: This bit is the change in data set ready (ΔDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input has changed states since the last time it was read by the CPU. When this bit is set and the modem status interrupt is enabled, a modem status interrupt is generated.
- Bit 2: This bit is the trailing edge of ring indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from a low to a high state. When this bit is set and the modem status interrupt is enabled, a modem status interrupt is generated.
- Bit 3: This bit is the change in data carrier detect (ΔDCD) indicator. Bit 3 indicates that the $\overline{DCD}$ input to the chip has changed states since the last time it was read by the CPU. When this bit is set and the modem status interrupt is enabled, a modem status interrupt is generated.
- Bit 4: This bit is the compliment of the clear to send ($\overline{CTS}$) input. When bit 4 (loop) of the MCR is set, bit 4 is equivalent to the MCR bit 1 (RTS).
- Bit 5: This bit is the compliment of the data set ready ($\overline{DSR}$) input. When bit 4 (loop) of the MCR is set, bit 5 is equivalent to the MCR bit 1 (DTR).

PRINCIPLES OF OPERATION

modem status register (MSR) (continued)

- Bit 6: This bit is the compliment of the ring indicator ($\overline{RI}$) input. When bit 4 (loop) of the MCR is set, bit 6 is equivalent to the MCR bit 2 (OUT1).
- Bit 7: This bit is the compliment of the data carrier detect ($\overline{DCD}$) input. When bit 4 (loop) of the MCR is set, bit 7 is equivalent to the MCR bit 3 (OUT2).

programmable baud generator

The ACE contains a programmable baud generator that takes a clock input in the range between dc and 8 MHz and divides it by a divisor in the range between 1 and (2^{16}–1). The output frequency of the baud generator is 16× the baud rate. The formula for the divisor is:

divisor # = XIN frequency input ÷ (desired baud rate × 16)

Two 8-bit registers, called divisor latches, store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization of the ACE in order to ensure desired operation of the baud generator. When either of the divisor latches is loaded, a 16-bit baud counter is also loaded to prevent long counts on initial load.

Tables 8 and 9, which follow, illustrate the use of the baud generator with crystal frequencies of 1.8432 MHz and 3.072 MHz, respectively For baud rates of 38.4 kbit/s and below, the error obtained is very small. The accuracy of the selected baud rate is dependent on the selected crystal frequency.

Refer to Figure 16 for examples of typical clock circuits.

Table 8. Baud Rates Using a 1.8432-MHz Crystal

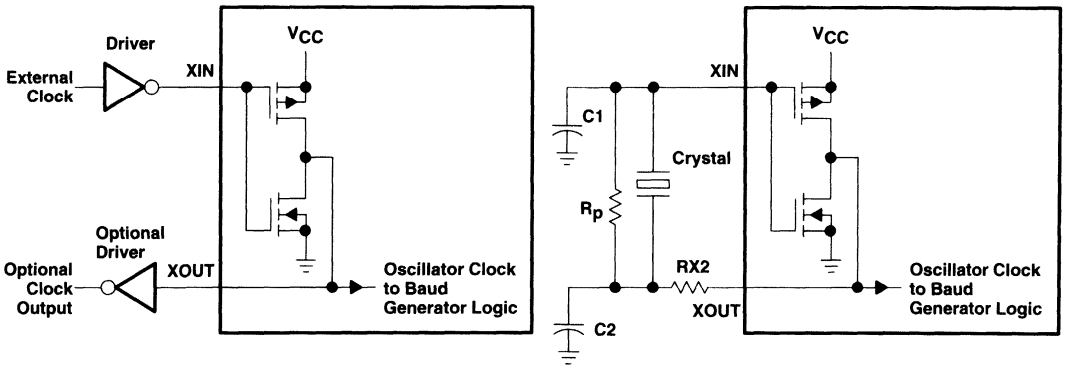
DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16× CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
1800	64	
2000	58	0.69
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19200	6	
38400	3	
56000	2	2.86

PRINCIPLES OF OPERATION

programmable baud generator (continued)

Table 9. Baud Rates Using a 3.072-MHz Crystal

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16× CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	
75	2560	
110	1745	0.026
134.5	1428	0.034
150	1280	
300	640	
600	320	
1200	160	
1800	107	0.312
2000	96	
2400	80	
3600	53	0.628
4800	40	
7200	27	1.23
9600	20	
19200	10	
38400	5	



TYPICAL CRYSTAL OSCILLATOR NETWORK

CRYSTAL	Rp	RX2	C1	C2
3.1 MHz	1 MΩ	1.5 kΩ	10–30 pF	40–60 pF
1.8 MHz	1 MΩ	1.5 kΩ	10–30 pF	40–60 pF

Figure 16. Typical Clock Circuits

receiver buffer register (RBR)

The ACE receiver section consists of a receiver shift register (RSR) and a RBR. The RBR is actually a 16-byte FIFO. Timing is supplied by the 16× receiver clock (RCLK). Receiver section control is a function of the ACE line control register.

The ACEs RSR receives serial data from the SIN terminal. The RSR then deserializes the data and moves it into the RBR FIFO. In the TL16C450 mode, when a character is placed in the RBR and the received data available interrupt is enabled, an interrupt is generated. This interrupt is cleared when the data is read out of the RBR. in the FIFO mode, the interrupts are generated based on the control setup in the FIFO control register.

scratch register

The scratch register is an 8-bit register that is intended for the programmer's use as a scratchpad in the sense that it temporarily holds the programmer's data without affecting any other ACE operation.

transmitter holding register (THR)

The ACE transmitter section consists of a THR and a transmitter shift register (TSR). The THR is actually a 16-byte FIFO. Timing is suppled by the baud out ($\overline{\text{BAUDOUT}}$) clock signal. Transmitter section control is a function of the ACE line control register.

The ACE THR receives data off the internal data bus and, when the shift register is idle, moves it into the TSR. The TSR serializes the data and outputs it at the serial output (SOUT). In the TL16C450 mode, when the THR is empty and the transmitter holding register empty (THRE) interrupt is enabled, an interrupt is generated. This interrupt is cleared when a character is loaded into the register. In the FIFO mode, the interrupts are generated based on the control setup in the FIFO control register.

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- **Capable of Running With All Existing TL16C450 Software**
- **After Reset, All Registers Are Identical to the TL16C450 Register Set**
- **In the FIFO Mode, Transmitter and Receiver Are Each Buffered With 16-Byte FIFOs to Reduce the Number of Interrupts to the CPU**
- **In the TL16C450 Mode, Hold and Shift Registers Eliminate the Need for Precise Synchronization Between the CPU and Serial Data**
- **Programmable Baud Rate Generator Allows Division of Any Input Reference Clock by 1 to ($2^{16}-1$) and Generates an Internal 16× Clock**
- **Standard Asynchronous Communication Bits (Start, Stop, and Parity) Added to or Deleted From the Serial Data Stream**
- **Independent Receiver Clock Input**
- **Transmit, Receive, Line Status, and Data Set Interrupts Independently Controlled**
- **Fully Programmable Serial Interface Characteristics:**
  - **5-, 6-, 7-, or 8-Bit Characters**
  - **Even-, Odd-, or No-Parity Bit Generation and Detection**
  - **1-, 1 1/2-, or 2-Stop Bit Generation**
  - **Baud Generation (DC to 256 Kbit/s)**
- **False-Start Bit Detection**
- **Complete Status Reporting Capabilities**
- **3-State Outputs Provide TTL Drive Capabilities for Bidirectional Data Bus and Control Bus**
- **Line Break Generation and Detection**
- **Internal Diagnostic Capabilities:**
  - **Loopback Controls for Communications Link Fault Isolation**
  - **Break, Parity, Overrun, Framing Error Simulation**
- **Fully Prioritized Interrupt System Controls**
- **Modem Control Functions ($\overline{CTS}$, $\overline{RTS}$, $\overline{DSR}$, $\overline{DTR}$, $\overline{RI}$, and $\overline{DCD}$)**
- **Faster Plug-In Replacement for National Semiconductor NS16550A**

description

The TL16C550B is a functional upgrade of the TL16C450 asynchronous communications element (ACE). Functionally identical to the TL16C450 on power up (character mode†), the TL16C550B can be placed in an alternate mode (FIFO) to relieve the CPU of excessive software overhead.

In this alternate FIFO mode, internal FIFOs are activated allowing 16 bytes (plus 3 bits of error data per byte in the receiver FIFO) to be stored in both receive and transmit modes. To minimize system overhead and maximize system efficiency, all logic is on the chip. Two of the TL16C450 terminal functions ($\overline{RXRDY}$ and $\overline{TXRDY}$) have been changed to allow signalling of DMA transfers.

The TL16C550B performs serial-to-parallel conversion on data received from a peripheral device or modem and parallel-to-serial conversion on data received from its CPU. The CPU can read and report on the status of the ACE at any point in the ACE operation. Reported status information includes: the type of transfer operation in progress, the status of the operation, and any error conditions encountered.

The TL16C550B ACE includes a programmable, on-board, baud rate generator. This generator is capable of dividing a reference clock input by divisors from 1 to ($2^{16}-1$) and producing a 16× clock for driving the internal transmitter logic. Provisions are included to use this 16× clock to drive the receiver logic. Also included in the ACE is a complete modem control capability and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link.

The TL16C550B is available in a 40-pin DIP (N) package, a 44-pin PLCC (FN) package, and a 48-pin TQFP (PT) package.

† The TL16C550B can also be reset to the TL16C450 mode under software control.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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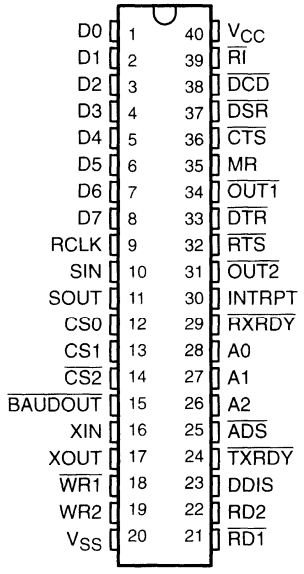
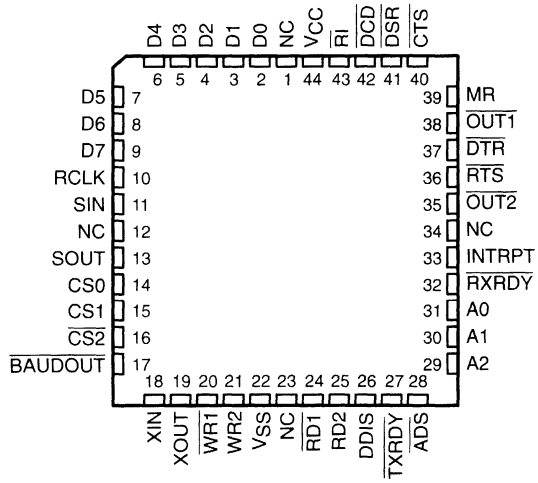
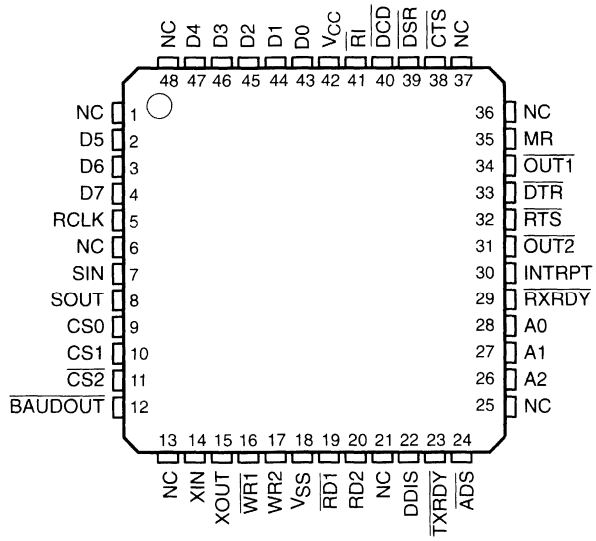
N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)

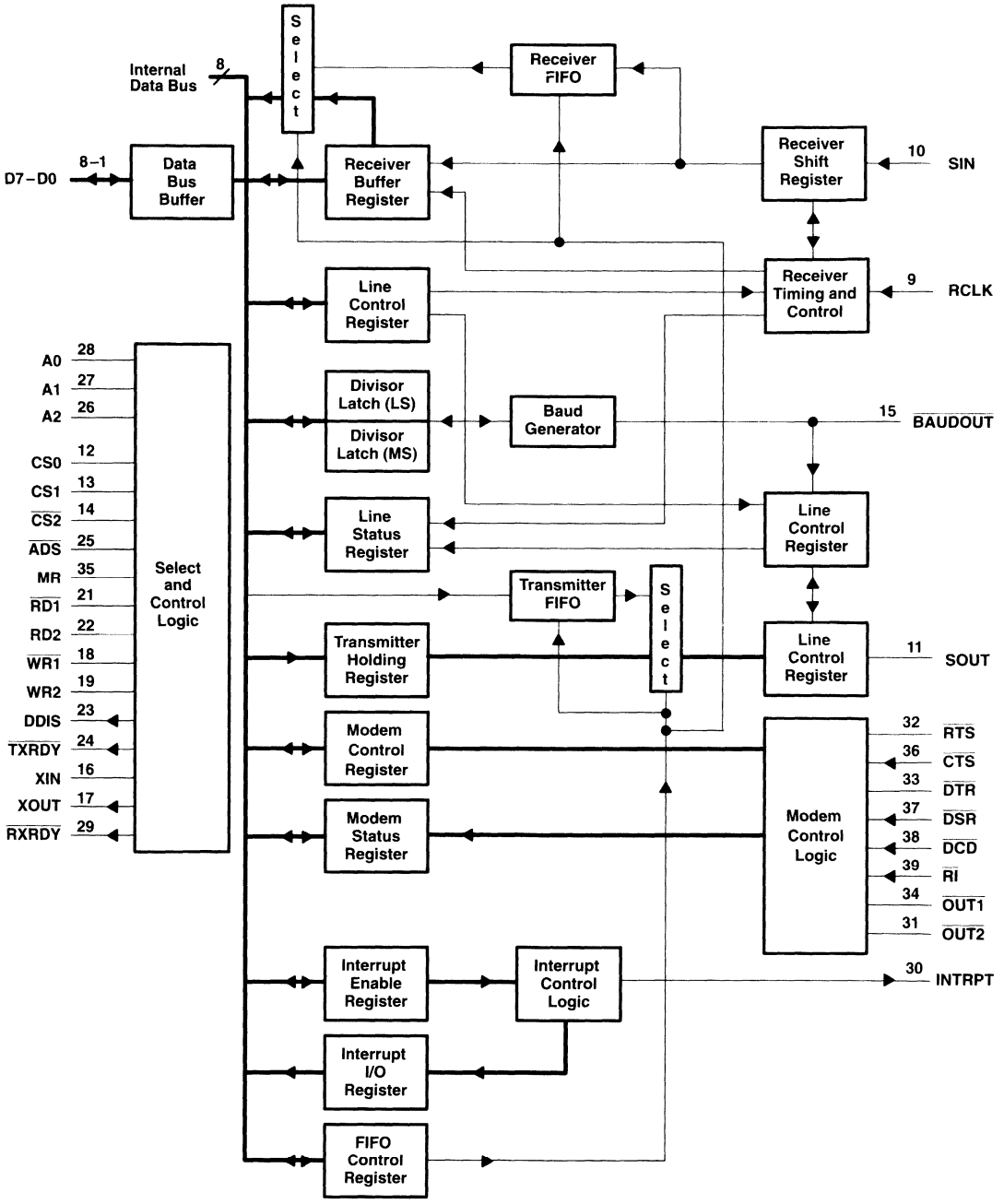


PT PACKAGE
(TOP VIEW)



NC – No internal connection

functional block diagram



Terminal numbers shown are for the N package.

Terminal Functions

TERMINAL NAME	NO. N	NO. FN	NO. PT	I/O	DESCRIPTION
A0 A1 A2	28 27 26	31 30 29	28 27 26	I	Register select. A0–A2 are used during read and write operations to select the ACE register to read from or write to. Refer to Table 1 for register addresses, and refer to the address strobe ($\overline{ADS}$) signal description.
$\overline{ADS}$	25	28	24	I	Address strobe. When $\overline{ADS}$ is active (low), the register select signals (A0, A1, and A2) and chip select signals (CS0, CS1, $\overline{CS2}$) drive the internal select logic directly; when high, the register select and chip select signals are held in the state they are in when the low-to-high transition of $\overline{ADS}$ occurs.
$\overline{BAUDOUT}$	15	17	12	O	Baud out. $\overline{BAUDOUT}$ is a 16× clock signal for the transmitter section of the ACE. The clock rate is established by the reference oscillator frequency divided by a divisor specified by the baud generator divisor latches. $\overline{BAUDOUT}$ can also be used for the receiver section by tying this output to RCLK.
CS0 CS1 $\overline{CS2}$	12 13 14	14 15 16	9 10 11	I	Chip select. When CS0 = high, CS1 = high, and $\overline{CS2}$ = low, these three inputs select the ACE. When any of these inputs are inactive, the ACE remains inactive. Refer to the $\overline{ADS}$ signal description.
$\overline{CTS}$	36	40	38	I	Clear to send. $\overline{CTS}$ is a modem status signal. Its condition can be checked by reading bit 4 (CTS) of the modem status register. Bit 0 (ΔCTS) of the modem status register indicates that this signal has changed states since the last read from the modem status register. If the modem status interrupt is enabled when $\overline{CTS}$ changes state, an interrupt is generated.
D0 D1 D2 D3 D4 D5 D6 D7	1 2 3 4 5 6 7 8	2 3 4 5 6 7 8 9	43 44 45 46 47 2 3 4	I/O	Data bus. Eight data lines with 3-state outputs provide a bidirectional path for data, control, and status information between the ACE and the CPU.
$\overline{DCD}$	38	42	40	I	Data carrier detect. $\overline{DCD}$ is a modem status signal. Its condition can be checked by reading bit 7 (DCD) of the modem status register. Bit 3 (ΔDCD) of the modem status register indicates that this signal has changed states since the last read from the modem status register. If the modem status interrupt is enabled when $\overline{DCD}$ changes state, an interrupt is generated.
DDIS	23	26	22	O	Driver disable. This output is active (high) when the CPU is not reading data. When active, this output can disable an external transceiver.
$\overline{DSR}$	37	41	39	I	Data set ready. $\overline{DSR}$ is a modem status signal. Its condition can be checked by reading bit 5 (DSR) of the modem status register. Bit 1 (ΔDSR) of the modem status register indicates this signal has changed states since the last read from the modem status register. If the modem status interrupt is enabled when $\overline{DSR}$ changes state, an interrupt is generated.
$\overline{DTR}$	33	37	33	O	Data terminal ready. When active (low), $\overline{DTR}$ informs a modem or data set that the ACE is ready to establish communication. $\overline{DTR}$ is placed in the active state by setting the DTR bit of the modem control register to a high level. $\overline{DTR}$ is placed in the inactive state either as a result of a master reset, during loop mode operation, or clearing the DTR bit.
INTRPT	30	33	30	O	Interrupt. When active (high), INTRPT informs the CPU that the ACE has an interrupt to be serviced. Four conditions that cause an interrupt to be issued are: a receiver error, received data is available or timed out (FIFO mode only), the transmitter holding register is empty, or an enabled modem status interrupt. The INTRPT output is reset (deactivated) either when the interrupt is serviced or as a result of a master reset.
MR	35	39	35	I	Master reset. When active (high), MR clears most ACE registers and sets the state of various output signals. Refer to Table 2.
$\overline{OUT1}$ $\overline{OUT2}$	34 31	38 35	34 31	O	Outputs 1 and 2. User-designated outputs that are set to their active low states by setting their respective modem control register bits (OUT1 and OUT2) high. $\overline{OUT1}$ and $\overline{OUT2}$ are set to their inactive (high) states as a result of master reset, during loop mode operations, or by clearing bit 2 (OUT1) or bit 3 (OUT2) of the modem control register.
RCLK	9	10	5	I	Receiver clock. RCLK is the 16× baud rate clock for the receiver section of the ACE.

Terminal Functions (Continued)

TERMINAL NAME	NO. N	NO. FN	NO. PT	I/O	DESCRIPTION
$\overline{RD1}$ RD2	21 22	24 25	19 20	I	Read inputs. When either input is active (low or high respectively) while the ACE is selected, the CPU is allowed to read status information or data from a selected ACE register. Only one of these inputs is required for the transfer of data during a read operation; the other input should be tied in its inactive state (i.e., RD2 tied low or $\overline{RD1}$ tied high).
$\overline{RI}$	39	43	41	I	Ring indicator. $\overline{RI}$ is a modem status signal. Its condition can be checked by reading bit 6 (RI) of the modem status register. Bit 2 (TERI) of the modem status register indicates that the $\overline{RI}$ input has transitioned from a low to a high state since the last read from the modem status register. If the modem status interrupt is enabled when this transition occurs, an interrupt is generated.
$\overline{RTS}$	32	36	32	O	Request to send. When active, $\overline{RTS}$ informs the modem or data set that the ACE is ready to receive data. $\overline{RTS}$ is set to its active state by setting the RTS modem control register bit and is set to its inactive (high) state either as a result of a master reset or during loop mode operations or by clearing bit 1 (RTS) of the MCR.
$\overline{RXRDY}$	29	32	29	O	Receiver ready output. Receiver direct memory access (DMA) signalling is available with this terminal. When operating in the FIFO mode, one of two types of DMA signalling can be selected using the FIFO control register bit 3 (FCR3). When operating in the TL16C450 mode, only DMA mode 0 is allowed. Mode 0 supports single-transfer DMA in which a transfer is made between CPU bus cycles. Mode 1 supports multitransfer DMA in which multiple transfers are made continuously until the receiver FIFO has been emptied. In DMA mode 0 (FCR0 = 0 or FCR0 = 1, FCR3 = 0), when there is at least one character in the receiver FIFO or receiver holding register, $\overline{RXRDY}$ is active low. When RXRDY has been active but there are no characters in the FIFO or holding register, $\overline{RXRDY}$ goes inactive (high). In DMA mode 1 (FCR0 = 1, FCR3 = 1), when the trigger level or the time out has been reached, $\overline{RXRDY}$ goes active (low); when it has been active but there are no more characters in the FIFO or holding register, it goes inactive (high).
SIN	10	11	7	I	Serial data input. Input from a connected communications device
SOUT	11	13	8	O	Composite serial data output. Output to a connected communication device. SOUT is set to the marking (set) state as a result of master reset.
$\overline{TXRDY}$	24	27	23	O	Transmitter ready output. Transmitter DMA signalling is available with this terminal. When operating in the FIFO mode, one of two types of DMA signalling can be selected using FCR3. When operating in the TL16C450 mode, only DMA mode 0 is allowed. Mode 0 supports single-transfer DMA in which a transfer is made between CPU bus cycles. Mode 1 supports multitransfer DMA in which multiple transfers are made continuously until the transmit FIFO has been filled.
V_{CC}	40	44	42		5-V supply voltage
V_{SS}	20	22	18		Supply common
$\overline{WR1}$ WR2	18 19	20 21	16 17	I	Write inputs. When either input is active (high or low respectively) and while the ACE is selected, the CPU is allowed to write control words or data into a selected ACE register. Only one of these inputs is required to transfer data during a write operation; the other input should be tied in its inactive state (i.e., WR2 tied low or $\overline{WR1}$ tied high).
XIN XOUT	16 17	18 19	14 15	I/O	External clock. XIN and XOUT connect the ACE to the main timing reference (clock or crystal).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Input voltage range at any input, V_I ..... −0.5 V to 7 V
Output voltage range, V_O ..... −0.5 V to 7 V
Operating free-air temperature range, T_A ..... 0°C to 70°C
Continuous total power dissipation at (or below) 70°C ..... 300 mW
Storage temperature range, T_{stg} ..... −65°C to 150°C
Case temperature for 10 seconds, T_C: FN package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N or PT package ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS} (ground).

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2		V_{CC}	V
Low-level input voltage, V_{IL}	−0.5		0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}‡	High-level output voltage	I_{OH} = −1 mA	2.4			V
V_{OL}‡	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
I_I	Input current	V_{CC} = 5.25 V, V_{SS} = 0, V_I = 0 to 5.25 V, All other terminals floating			10	µA
I_{OZ}	High-impedance-state output current	V_{CC} = 5.25 V, V_{SS} = 0, V_O = 0 to 5.25 V, Chip selected in write mode or chip deselect			±20	µA
I_{CC}	Supply current	V_{CC} = 5.25 V, T_A = 25°C, SIN, $\overline{DSR}$, $\overline{DCD}$, $\overline{CTS}$, and $\overline{RI}$ at 2 V, All other inputs at 0.8 V, XTAL1 at 4 MHz, No load on outputs, Baud rate = 50 kbit/s			10	mA
$C_{i(CLK)}$	Clock input capacitance	V_{CC} = 0, V_{SS} = 0, f = 1 MHz, T_A = 25°C, All other terminals grounded		15	20	pF
$C_{o(CLK)}$	Clock output capacitance			20	30	pF
C_i	Input capacitance			6	10	pF
C_o	Output capacitance			10	20	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ These parameters apply for all outputs except XOUT.

system timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{cR}	Cycle time, read ($t_{w7} + t_{d8} + t_{d9}$)	RC			87		ns
t_{cW}	Cycle time, write ($t_{w6} + t_{d5} + t_{d6}$)	WC			87		ns
t_{w1}	Pulse duration, clock high	t_{XH}	1	f = 9 MHz maximum	40		ns
t_{w2}	Pulse duration, clock low	t_{XL}	1	f = 9 MHz maximum	40		ns
t_{w5}	Pulse duration, address strobe low	t_{ADS}	2,3		9		ns
t_{w6}	Pulse duration, write strobe	t_{WR}	2		40		ns
t_{w7}	Pulse duration, read strobe	tRD	3		40		ns
t_{w8}	Pulse duration, master reset	t_{MR}			1		µs
t_{su1}	Setup time, address valid before $\overline{ADS}\uparrow$	t_{AS}	2,3		8		ns
t_{su2}	Setup time, chip select valid before $\overline{ADS}\uparrow$	t_{CS}	2,3		8		ns
t_{su3}	Setup time, data valid before $\overline{WR1}\downarrow$ or WR2$\uparrow$	t_{DS}	2		15		ns
t_{h1}	Hold time, address low after $\overline{ADS}\uparrow$	t_{AH}	2,3		0		ns
t_{h2}	Hold time, chip select valid after $\overline{ADS}\uparrow$	t_{CH}	2,3		0		ns
t_{h3}	Hold time, chip select valid after $\overline{WR1}\uparrow$ or WR2$\downarrow$	t_{WCS}	2		10		ns
t_{h4}	Hold time, address valid after $\overline{WR1}\uparrow$ or WR2$\downarrow$	t_{WA}	2		10		ns
t_{h5}	Hold time, data valid after $\overline{WR1}\uparrow$ or WR2$\downarrow$	t_{DH}	2		5		ns
t_{h6}	Hold time, chip select valid after $\overline{RD1}\uparrow$ or RD2$\downarrow$	t_{RCS}	3		10		ns
t_{h7}	Hold time, address valid after $\overline{RD1}\uparrow$ or RD2$\downarrow$	t_{RA}	3		20		ns
t_{d4}†	Delay time, chip select valid before $\overline{WR1}\downarrow$ or WR2$\uparrow$	t_{CSW}	2		7		ns
t_{d5}†	Delay time, address valid before $\overline{WR1}\downarrow$ or WR2$\uparrow$	t_{AW}	2		7		ns
t_{d6}†	Delay time, write cycle, $\overline{WR1}\uparrow$ or WR2$\downarrow$ to $\overline{ADS}\downarrow$	t_{WC}	2		40		ns
t_{d7}†	Delay time, chip select valid to $\overline{RD1}\downarrow$ or RD2$\uparrow$	t_{CSR}	3		7		ns
t_{d8}†	Delay time, address valid to $\overline{RD1}\downarrow$ or RD2$\uparrow$	t_{AR}	3		7		ns
t_{d9}	Delay time, read cycle, $\overline{RD1}\uparrow$ or RD2$\downarrow$ to $\overline{ADS}\downarrow$	tRC	3		40		ns
t_{d10}	Delay time, $\overline{RD1}\downarrow$ or RD2$\uparrow$ to data valid	t_{RVD}	3	C_L = 75 pF	45		ns
t_{d11}	Delay time, $\overline{RD1}\uparrow$ or RD2$\downarrow$ to floating data	t_{HZ}	3	C_L = 75 pF	20		ns

† Only applies when $\overline{ADS}$ is low

system switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 2)

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$t_{dis(R)}$	Disable time, $\overline{RD1}\uparrow\downarrow$ or RD2$\downarrow\uparrow$ to DDIS$\uparrow\downarrow$	t_{RDD}	3	C_L = 75 pF	20		ns

NOTE 2: Charge and discharge time is determined by V_{OL}, V_{OH}, and external loading.

baud generator switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 75 pF

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{w3}	Pulse duration, $\overline{BAUDOUT}$ low	t_{LW}	1	f = 9 MHz, CLK ÷ 2	80		ns
t_{w4}	Pulse duration, $\overline{BAUDOUT}$ high	t_{HW}	1	f = 9 MHz, CLK ÷ 2	80		ns
t_{d1}	Delay time, XIN$\uparrow$ to $\overline{BAUDOUT}\uparrow$	t_{BLD}	1			75	ns
t_{d2}	Delay time, XIN$\uparrow\downarrow$ to $\overline{BAUDOUT}\downarrow$	t_{BHD}	1			65	ns

receiver switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 3)

	PARAMETER	ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d12}	Delay time, RCLK to sample	t_{SCD}	4			10	ns
t_{d13}	Delay time, stop to set interrupt or read RBR to LSI interrupt or stop to $\overline{RXRDY}\downarrow$	t_{SINT}	4,5,6,7,8			1	RCLK cycle
t_{d14}	Delay time, read RBR/LSR to reset interrupt low	t_{RINT}	4,5,6,7,8	C_L = 75 pF		40	ns

NOTE 3: In the FIFO mode, the read cycle (RC) = 425 ns (minimum) between reads of the receiver FIFO and the status registers (interrupt identification register or line status register).

transmitter switching characteristics over recommended ranges of supply voltage and operating free-air temperature

	PARAMETER	ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d15}	Delay time, initial write (INTRPT low) to transmit start (SOUT low)	t_{IRS}	9		8	24	baudout cycles
t_{d16}	Delay time, stop (SOUT low) to interrupt (INTRPT high)	t_{STI}	9		8	9	baudout cycles
t_{d17}	Delay time, WR THR high to reset interrupt (INTRPT low)	t_{HR}	9	C_L = 75 pF		50	ns
t_{d18}	Delay time, initial WR THR low to THRE interrupt (INTRPT high)	t_{SI}	9		16	32	baudout cycles
t_{d19}	Delay time, RD IIR low to reset THRE interrupt (INTRPT low)	t_{IR}	9	C_L = 75 pF		35	ns
t_{d20}	Delay time, WR THR high to $\overline{TXRDY}$ high (inactive)	t_{WXI}	10,11	C_L = 75 pF		35	ns
t_{d21}	Delay time, start (SOUT low) to $\overline{TXRDY}$ low (active)	t_{SXA}	10,11	C_L = 75 pF		8	baudout cycles

modem control switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 75 pF

	PARAMETER	ALT. SYMBOL	FIGURE	MIN	MAX	UNIT
t_{d22}	Delay time, WR MCR low to output ($\overline{RTS}$, $\overline{DTR}$, $\overline{OUT1}$, $\overline{OUT2}$) low or high	t_{MDO}	12		50	ns
t_{d23}	Delay time, modem interrupt ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$) low to set interrupt (INTRPT) high	t_{SIM}	12		35	ns
t_{d24}	Delay time, RD MSR low to reset interrupt (INTRPT) low	t_{RIM}	12		40	ns

PARAMETER MEASUREMENT INFORMATION

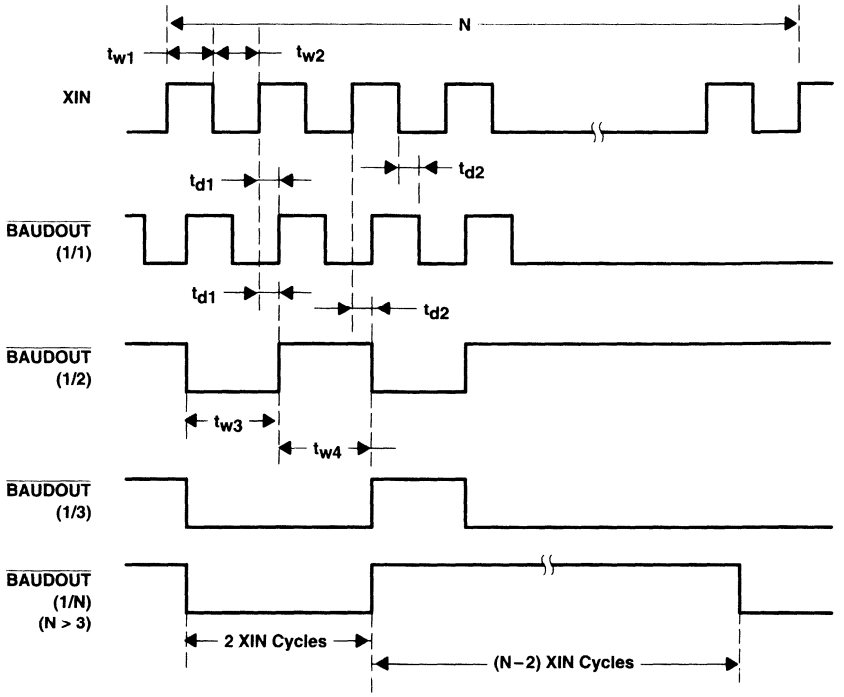
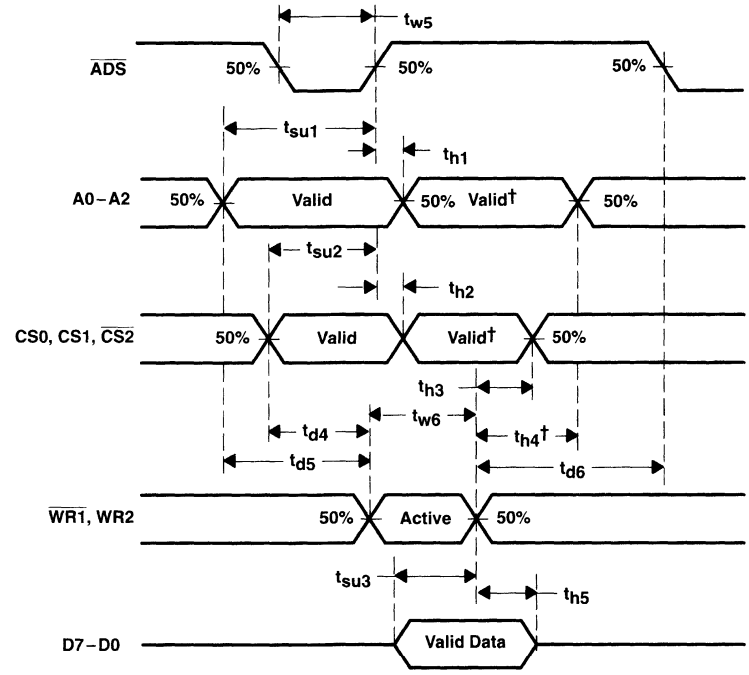


Figure 1. Baud Generator Timing Waveforms

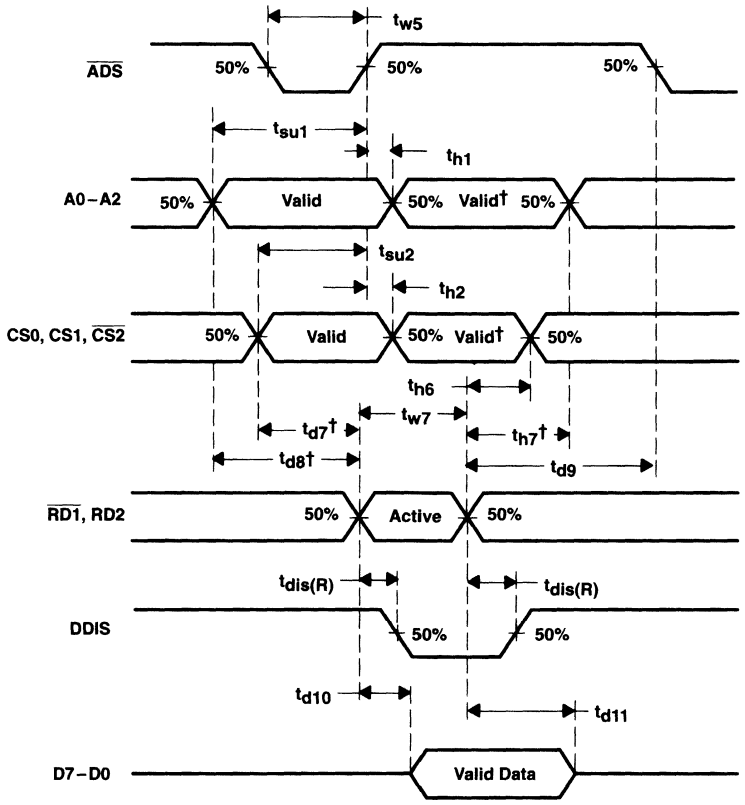
PARAMETER MEASUREMENT INFORMATION



† Applicable only when $\overline{ADS}$ is low.

Figure 2. Write Cycle Timing Waveforms

PARAMETER MEASUREMENT INFORMATION



† Applicable only when ADS is low.

Figure 3. Read Cycle Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

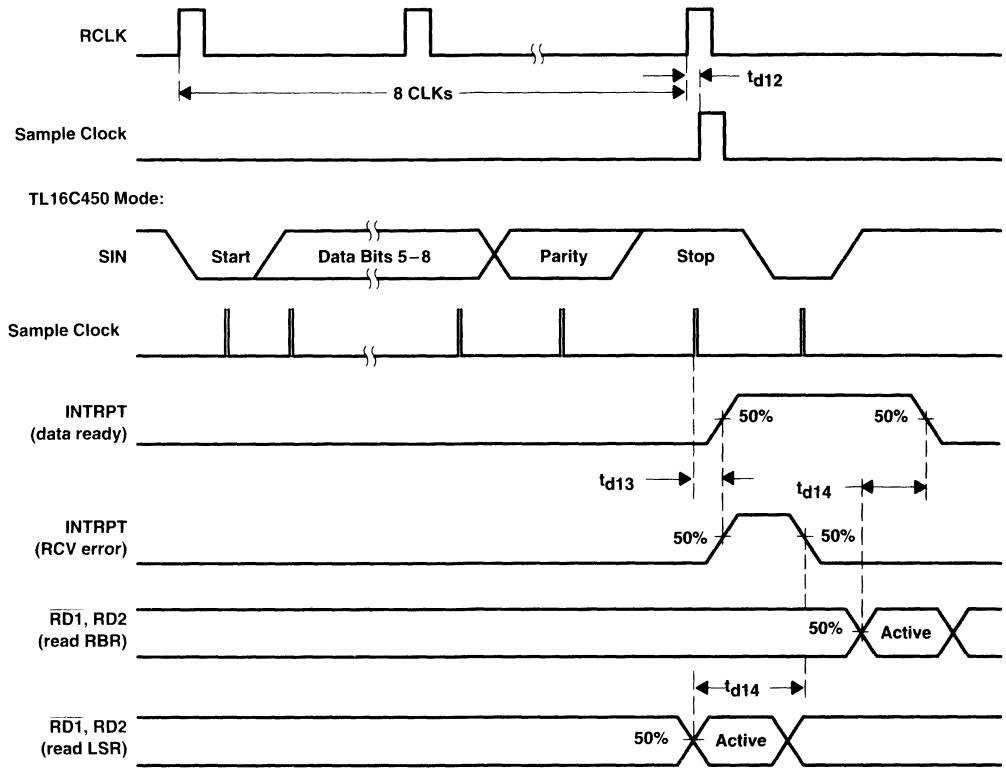


Figure 4. Receiver Timing Waveforms

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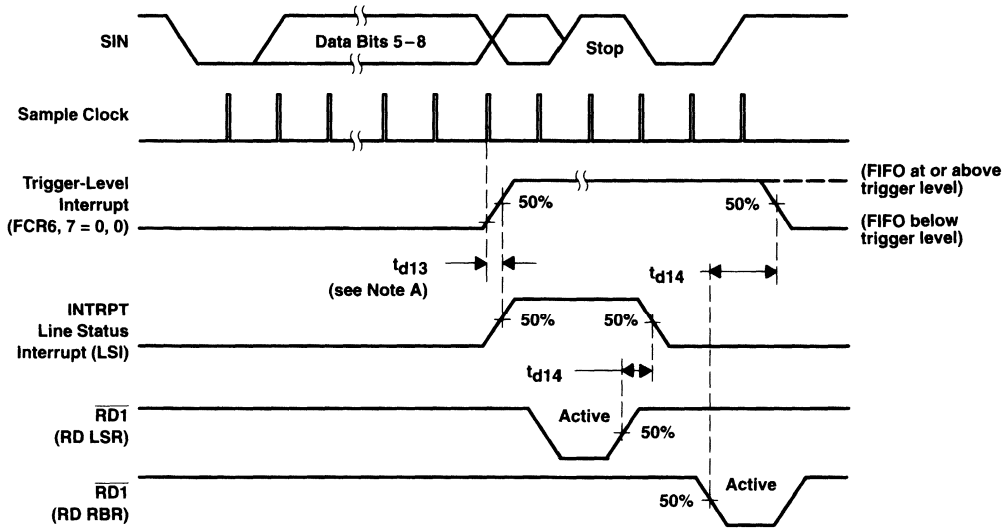
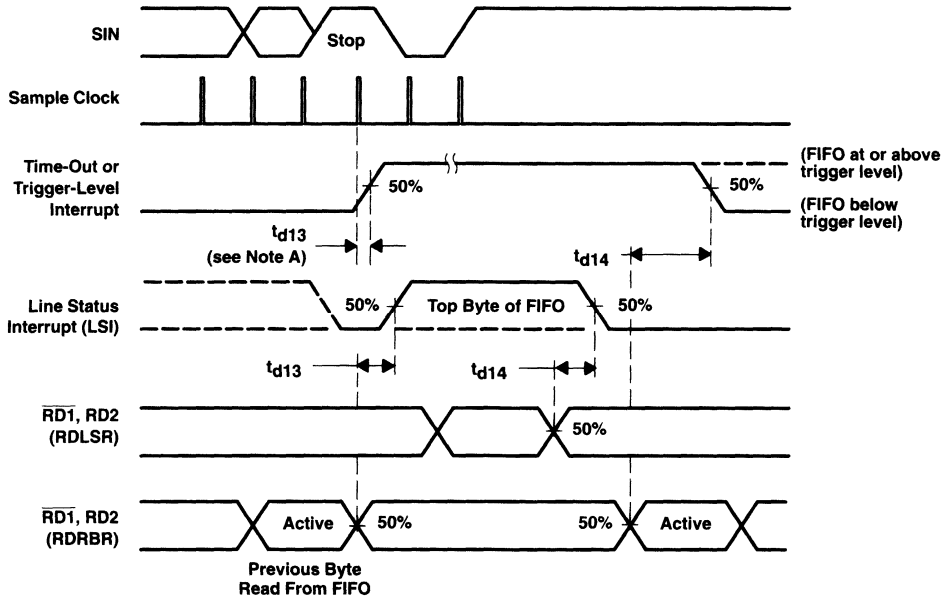
PARAMETER MEASUREMENT INFORMATION



NOTE A: For a time out interrupt, t_{d13} = 8 RCLKs.

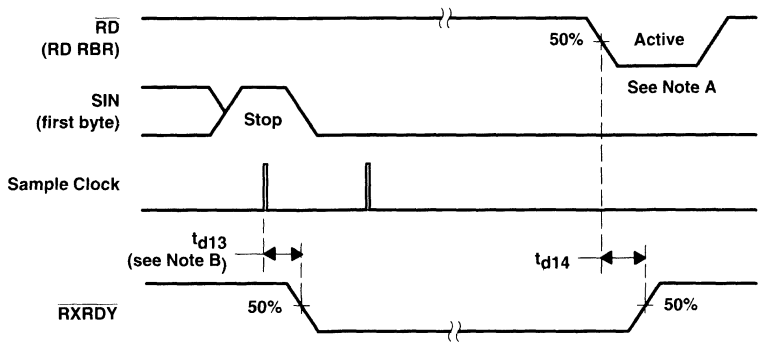
Figure 5. Receiver FIFO First Byte (Sets DR Bit) Waveforms



NOTE A: For a time out interrupt, t_{d13} = 8 RCLKs.

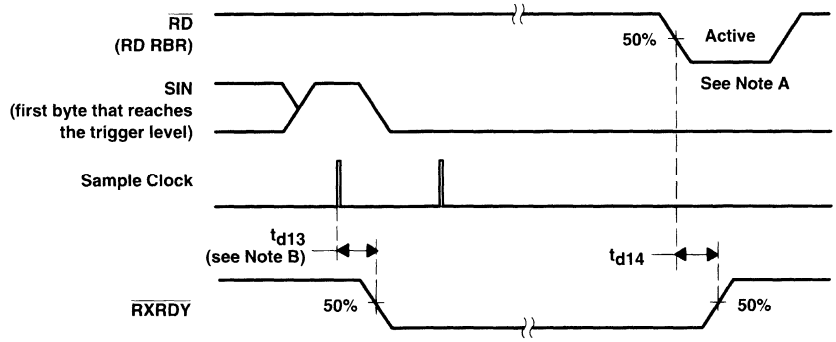
Figure 6. Receiver FIFO Bytes Other Than the First Byte (DR Internal Bit Already Set) Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. This is the reading of the last byte in the FIFO.
B. For a time out interrupt, t_{d13} = 8 RCLKs.

Figure 7. Receiver Ready ($\overline{RXRDY}$) Waveforms, FCR0 = 0 or FCR0 = 1 and FCR3 = 0 (Mode 0)



NOTES: A. This is the reading of the last byte in the FIFO.
B. For a time out interrupt, t_{d13} = 8 RCLKs.

Figure 8. Receiver Ready ($\overline{RXRDY}$) Waveforms, FCR = 1 or FCR3 = 1 (Mode 1)

PARAMETER MEASUREMENT INFORMATION

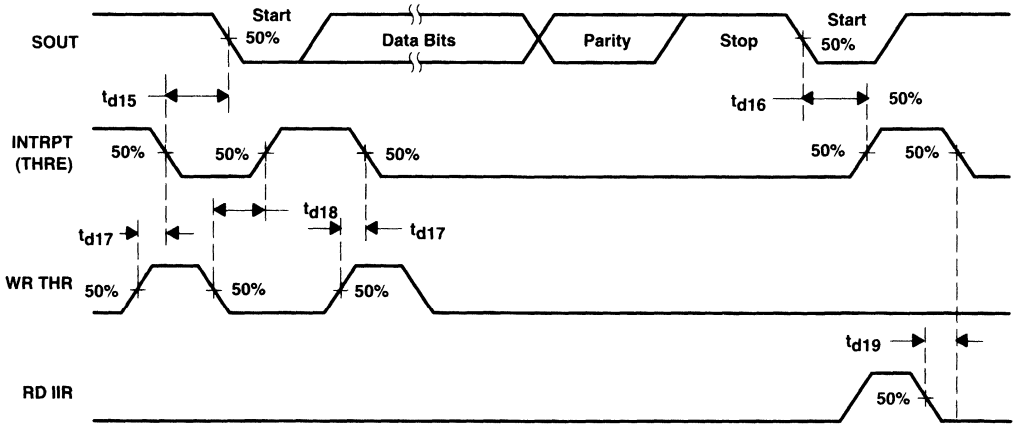


Figure 9. Transmitter Timing Waveforms

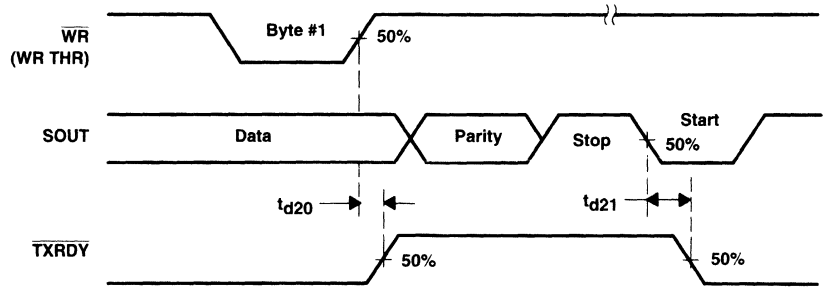


Figure 10. Transmitter Ready ($\overline{TXRDY}$) Waveforms, FCR0 = 0 or FCR0 = 1 and FCR3 = 0 (Mode 0)

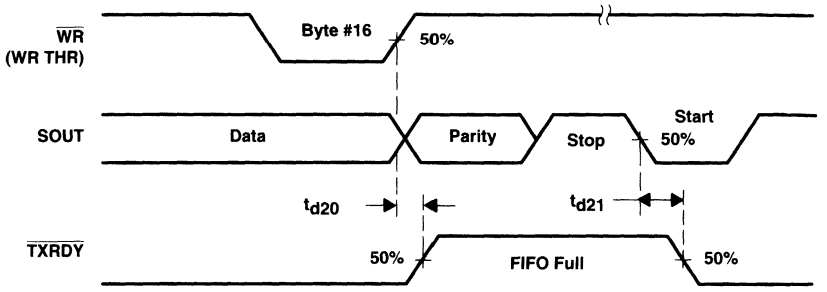


Figure 11. Transmitter Ready ($\overline{TXRDY}$) Waveforms, FCR0 = 1 and FCR3 = 1 (Mode 1)

PARAMETER MEASUREMENT INFORMATION

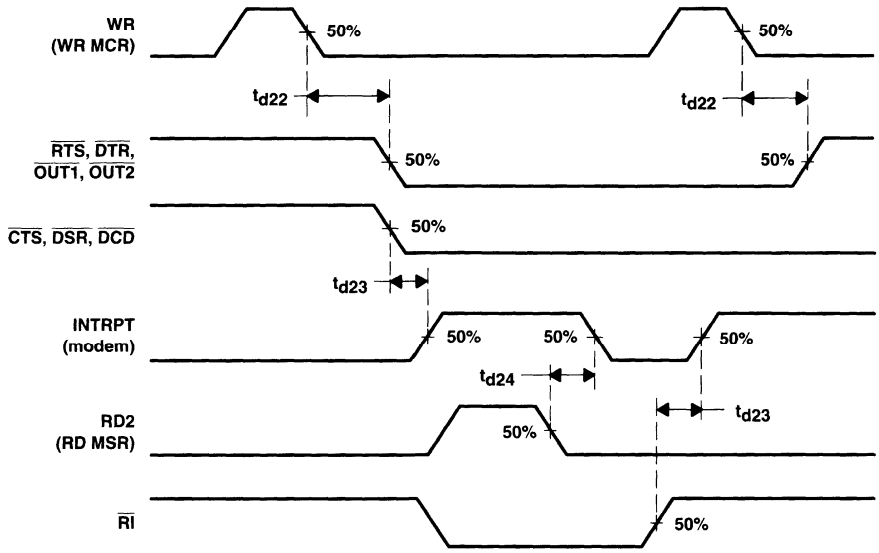


Figure 12. Modem Control Timing Waveforms

APPLICATION INFORMATION

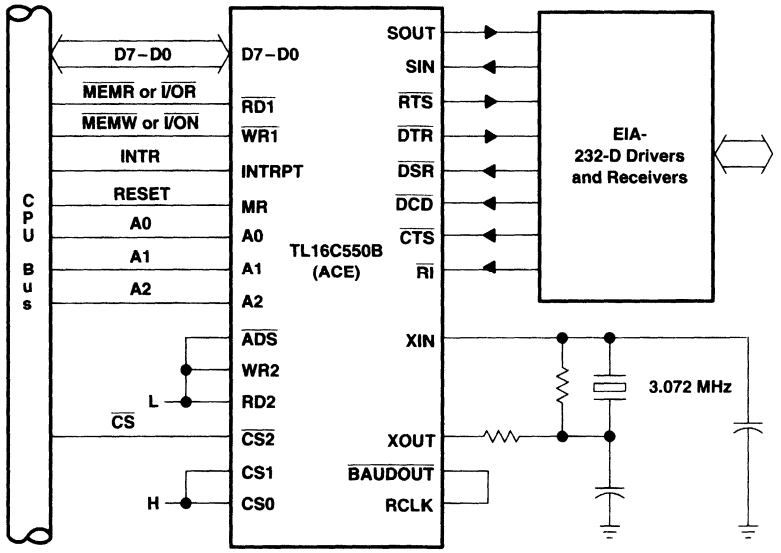


Figure 13. Basic TL16C550B Configuration

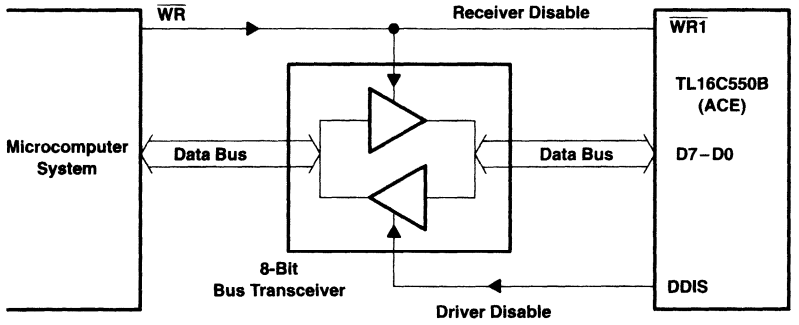
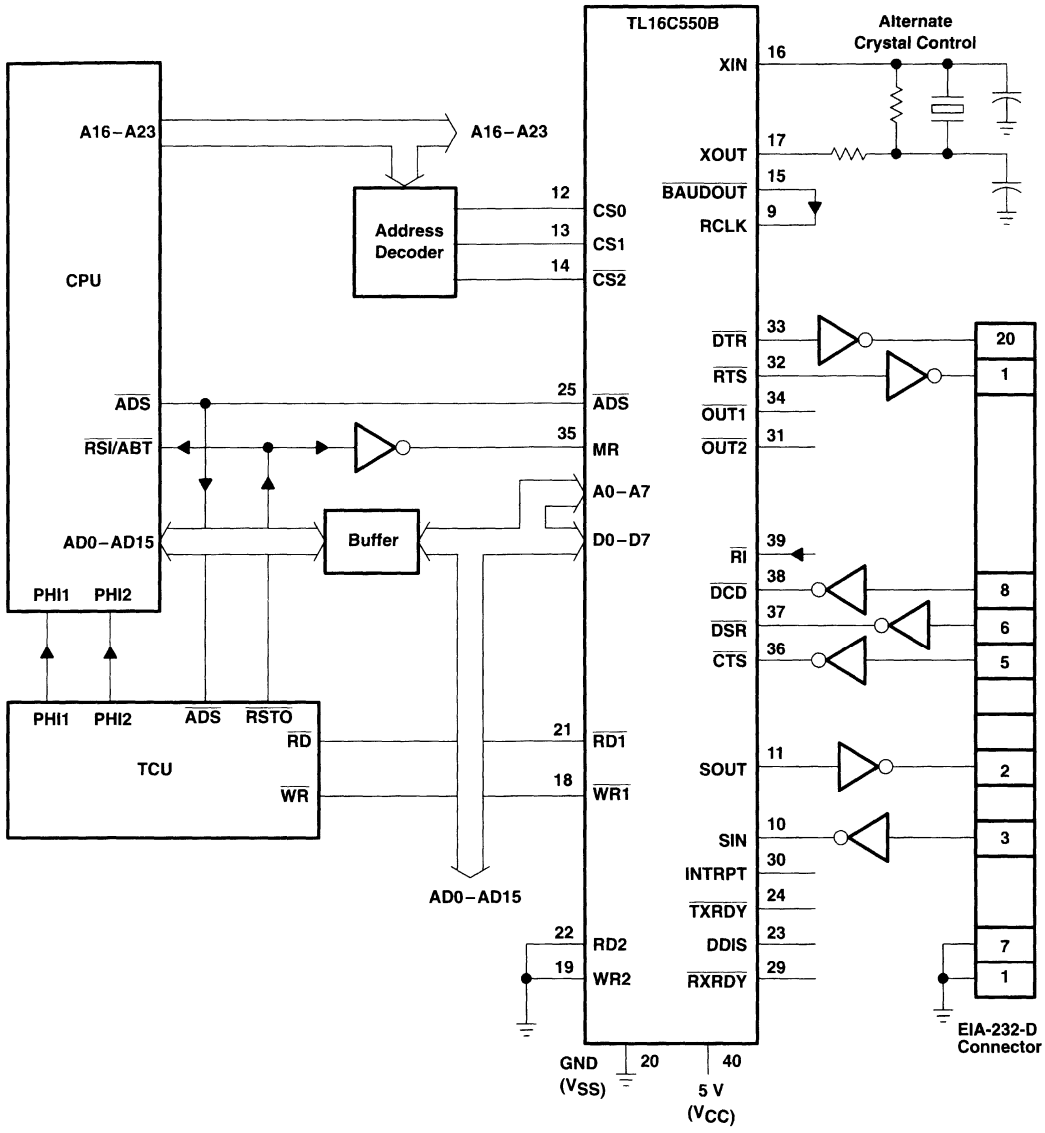


Figure 14. Typical Interface for a High-Capacity Data Bus

APPLICATION INFORMATION



Terminal numbers shown are for the N package.

Figure 15. Typical TL16C550B Connection to a CPU

PRINCIPLES OF OPERATION

Table 1. Register Selection

DLAB†	A2	A1	A0	REGISTER
0	L	L	L	Receiver buffer (read), transmitter holding (write)
0	L	L	H	Interrupt enable register
X	L	H	L	Interrupt identification register (read only)
X	L	H	L	FIFO control register (write)
X	L	H	H	Line control register
X	H	L	L	Modem control register
X	H	L	H	Line status register
X	H	H	L	Modem status register
X	H	H	H	Scratch register
1	L	L	L	Divisor latch (LSB)
1	L	L	H	Divisor latch (MSB)

† The divisor latch access bit (DLAB) is the most significant bit of the line control register. The DLAB signal is controlled by writing to this bit location (see Table 3).

Table 2. ACE Reset Functions

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	Master Reset	All bits cleared (bits 0–3 forced and bits 4–7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is set, bits 1–3 are cleared, and bits 4–7 are permanently cleared
FIFO Control Register	Master Reset	All bits cleared
Line Control Register	Master Reset	All bits cleared
Modem Control Register	Master Reset	All bits cleared (5–7 permanent)
Line Status Register	Master Reset	Bits 5 and 6 are set, all other bits are cleared
Modem Status Register	Master Reset	Bits 0–3 are cleared, bits 4–7 are input signals
SOUT	Master Reset	High
INTRPT (receiver error flag)	Read LSR/MR	Low
INTRPT (received data available)	Read RBR/MR	Low
INTRPT (transmitter holding register empty)	Read IR/Write THR/MR	Low
INTRPT (modem status changes)	Read MSR/MR	Low
$\overline{OUT2}$	Master Reset	High
$\overline{RTS}$	Master Reset	High
$\overline{DTR}$	Master Reset	High
$\overline{OUT1}$	Master Reset	High
Scratch Register	Master Reset	No effect
Divisor Latch (LSB and MSB) Registers	Master Reset	No effect
Receiver Buffer Registers	Master Reset	No effect
Transmitter Holding Registers	Master Reset	No effect
RCVR FIFO	MR/FCR1–FCR0/ ΔFCR0	All bits low
XMIT FIFO	MR/FCR2–FCR0/ ΔFCR0	All bits low

PRINCIPLES OF OPERATION

accessible registers

The system programmer, using the CPU, has access to and control over any of the ACE registers that are summarized in Table 3. These registers control ACE operations, receive data, and transmit data. Descriptions of these registers follow Table 3.

Table 3. Summary of Accessible Registers

Bit No.	REGISTER ADDRESS											
	0 DLAB = 0	0 DLAB = 0	1 DLAB = 0	2	2	3	4	5	6	7	0 DLAB = 1	1 DLAB = 1
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident. Register (Read Only)	FIFO Control Register (Write Only)	Line Control Register	Modem Control Register	Line Status Register	Modem Status Register	Scratch Register	Divisor Latch (LSB)	Latch (MSB)
	RBR	THR	IER	IIR	FCR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Data Bit 0†	Data Bit 0	Enable Received Data Available Interrupt (ERBI)	0 if Interrupt Pending	FIFO Enable	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (ΔCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (1)	Receiver FIFO Reset	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (ΔDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (2)	Transmitter FIFO Reset	Number of Stop Bits (STB)	OUT1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable Modem Status Interrupt (EDSSI)	Interrupt ID Bit (2) (see Note 4)	DMA Mode Select	Parity Enable (PEN)	OUT2	Framing Error (FE)	Delta Data Carrier Detect (ΔDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	FIFOs Enabled (see Note 4)	Receiver Trigger (LSB)	Break Control	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	FIFOs Enabled (see Note 4)	Receiver Trigger (MSB)	Divisor Latch Access Bit (DLAB)	0	Error in RCVR FIFO (see Note 4)	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

† Bit 0 is the least significant bit. It is the first bit serially transmitted or received.
NOTE 4: These bits are always 0 in the TL16C450 mode.

PRINCIPLES OF OPERATION

FIFO control register (FCR)

The FCR is a write-only register at the same location as the IIR, which is a read-only register. The FCR enables the FIFOs, clears the FIFOs, sets the receiver FIFO trigger level, and selects the type of DMA signalling.

Bit 0: FCR0, when set, enables the transmit and receive FIFOs. This bit must be set when other FCR bits are written to or they are not programmed. Changing this bit clears the FIFOs.

- Bit 1: FCR1, when set, clears all bytes in the receiver FIFO and clears its counter. The shift register is not cleared. The one that is written to this bit position is self clearing.
- Bit 2: FCR2, when set, clears all bytes in the transmit FIFO and clears its counter. The shift register is not cleared. The one that is written to this bit position is self clearing.
- Bit 3: When FCR0 is set, setting FCR3 causes the $\overline{\text{RXRDY}}$ and $\overline{\text{TXRDY}}$ to change from mode 0 to mode 1.
- Bits 4 and 5: FCR4 and FCR5 are reserved for future use.
- Bits 6 and 7: FCR6 and FCR7 set the trigger level for the receiver FIFO interrupt (see Table 5).

Table 4. Receiver FIFO Trigger Level

BIT 7	BIT 6	RECEIVER FIFO TRIGGER LEVEL (BYTES)
0	0	01
0	1	04
1	0	08
1	1	14

FIFO interrupt mode operation

When the receiver FIFO and receiver interrupts are enabled (FCR0 = 1, IER0 = 1) receiver interrupt occur as follows:

1. The receive data available interrupt is issued to the microprocessor when the FIFO has reached its programmed trigger level. It is cleared when the FIFO drops below its programmed trigger level.
2. The IIR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt, it is cleared when the FIFO drops below the trigger level.
3. The receiver line status interrupt (IIR = 0110) has higher priority than the received data available interrupt (IIR = 0100).
4. The data ready bit (LSR0) is set when a character is transferred from the shift register to the receiver FIFO. It is cleared when the FIFO is empty.

PRINCIPLES OF OPERATION

FIFO interrupt mode operation (continued)

When the receiver FIFO and receiver interrupts are enabled, receiver FIFO time-out interrupt occurs as follows:

1. FIFO time-out interrupt occurs when the following conditions exist:
   a. At least one character is in the FIFO.
   b. The most recent serial character received is longer than four continuous character times ago (when two stop bits are programmed, the second one is included in this time delay).
   c. The most recent microprocessor read of the FIFO is longer than four continuous character times ago. This causes a maximum character received to interrupt an issued delay of 160 ms at 300 baud with a 12-bit character.
2. Character times are calculated by using the RCLK input for a clock signal (makes the delay proportional to the baud rate).
3. When a time-out interrupt has occurred, it is cleared and the timer is reset when the microprocessor reads one character from the receiver FIFO.
4. When a time-out interrupt has not occurred, the time-out timer is reset after a new character is received or after the microprocessor reads the receiver FIFO.

When the transmit FIFO and transmitter interrupts are enabled (FCR0 = 1, IER1 = 1), transmit interrupts occur as follows:

1. The transmitter holding register interrupt (02) occurs when the transmit FIFO is empty. It is cleared as soon as the THR is written to (1 to 16 characters may be written to the transmit FIFO while servicing this interrupt) or the IIR is read.
2. The transmit FIFO empty indications are delayed one character time minus the last stop bit time when the following occurs: THRE = 1 and there have not been at least two bytes at the same time in the transmit FIFO since the last THRE = 1. The first transmitter interrupt after changing FCR0 is immediate when it is enabled.

Character time-out and receiver FIFO trigger level interrupts have the same priority as the current received data available interrupt; transmit FIFO empty has the same priority as the current THRE interrupt.

FIFO polled mode operation

When FCR0 is set, clearing IER0, IER1, IER2, IER3, or all four puts the ACE in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately, either one or both can be in the polled mode of operation.

In this mode, the user program checks receiver and transmitter status via the LSR. As stated previously:

- LSR0 is set as long as there is one byte in the receiver FIFO.
- LSR1 – LSR4 specify which error(s) have occurred. Character error status is handled the same way as when in the interrupt mode; the IIR is not affected since IER2 = 0.
- LSR5 indicates when the transmit FIFO is empty.
- LSR6 indicates that both the transmit FIFO and shift registers are empty.
- LSR7 indicates whether there are any errors in the receiver FIFO.

There is no trigger level reached or time-out condition indicated in the FIFO polled mode. However, the receiver and transmit FIFOs are still fully capable of holding characters.

PRINCIPLES OF OPERATION

interrupt enable register (IER)

The IER enables each of the five types of interrupts (refer to Table 4) and the INTRPT output signal in response to an interrupt generation. The IER can also disable the interrupt system by clearing bits 0 through 3. The contents of this register are summarized in Table3 and are described in the following bulleted list.

- Bit 0: This bit when set enables the received data available interrupt.
- Bit 1: This bit when set enables the THRE interrupt.
- Bit 2: This bit when set enables the receiver line status interrupt.
- Bit 3: This bit when set enables the modem status interrupt.
- Bits 4 – 7: These bits in the IER are not used and are always cleared.

interrupt identification register (IIR)

The ACE has an on-chip interrupt generation and prioritization capability that permits a flexible interface with most popular microprocessors. The ACE provides four prioritized levels of interrupts:

- Priority 1 – Receiver line status (highest priority)
- Priority 2 – Receiver data ready or receiver character time out
- Priority 3 – Transmitter holding register empty
- Priority 4 – Modem status (lowest priority)

When an interrupt is generated, the IIR indicates that an interrupt is pending and the type of that interrupt in its three least significant bits (bits 0, 1, and 2). The contents of this register are summarized in Table 3 and described in Table 4. Detail on each bit are as follows:

- Bit 0: This bit can be used either in a hardwire prioritized or polled interrupt system. When this bit is cleared, an interrupt is pending. When bit 0 is set, no interrupt is pending.
- Bits 1 and 2: These two bits identify the highest priority interrupt pending, as indicated in Table 4.
- Bit 3. This bit is always cleared in the TL16C450 mode. In FIFO mode, this bit is set with bit 2 to indicate that a time out interrupt is pending.
- Bits 4 – 5: These two bits are not used and are always cleared.
- Bits 6 and 7: These two bits are always cleared in the TL16C450 mode. They are set when bit 0 of the FIFO control register is set.

PRINCIPLES OF OPERATION

interrupt identification register (IIR) (continued)

Table 5. Interrupt Control Functions

INTERRUPT IDENTIFICATION REGISTER				PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET METHOD
BIT 3	BIT 2	BIT 1	BIT 0				
0	0	0	1	None	None	None	None
0	1	1	0	1	Receiver line status	Overrun error, parity error, framing error or break interrupt	Reading the line status register
0	1	0	0	2	Received data available	Receiver data available in the TL16C450 mode or trigger level reached in the FIFO mode.	Reading the receiver buffer register
1	1	0	0	2	Character time out indication	No characters have been removed from or input to the receiver FIFO during the last four character times, and there is at least one character in it during this time	Reading the receiver buffer register
0	0	1	0	3	Transmitter holding register empty	Transmitter holding register–empty	Reading the interrupt identification register (if source of interrupt) or writing into the transmitter holding register
0	0	0	0	4	Modem status	Clear to send, data set ready, ring indicator, or data carrier detect	Reading the modem status register

line control register (LCR)

The system programmer controls the format of the asynchronous data communication exchange through the LCR. In addition, the programmer is able to retrieve, inspect, and modify the contents of the LCR; this eliminates the need for separate storage of the line characteristics in system memory. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. These bits are encoded in Table 6.

Table 6. Serial Character Word Length

BIT 1	BIT 0	WORD LENGTH
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

- Bit 2: This bit specifies either one, one and one-half, or two stop bits in each transmitted character. When bit 2 is cleared, one stop bit is generated in the data. When bit 2 is set, the number of stop bits generated is dependent on the word length selected with bits 0 and 1. The receiver clocks only the first stop bit, regardless of the number of stop bits selected. The number of stop bits generated, in relation to word length and bit 2, is shown in Table 7.

PRINCIPLES OF OPERATION

line control register (LCR) (continued)

Table 7. Number of Stop Bits Generated

BIT 2	WORD LENGTH SELECTED BY BITS 1 AND 2	NUMBER OF STOP BITS GENERATED
0	Any word length	1
1	5 bits	1 1/2
1	6 bits	2
1	7 bits	2
1	8 bits	2

- Bit 3: This bit is the parity enable bit. When bit 3 is set, a parity bit is generated in transmitted data between the last data word bit and the first stop bit. In received data, when bit 3 is set, parity is checked. When bit 3 is cleared, no parity is generated or checked.
- Bit 4: This bit is the even parity select bit. When parity is enabled (bit 3 is set) and bit 4 is set, even parity (an even number of logic 1s in the data and parity bits) is selected. When parity is enabled and bit 4 is cleared, odd parity (an odd number of logic 1s) is selected.
- Bit 5: This is the stick parity bit. When bits 3, 4, and 5 are set, the parity bit is transmitted and checked as cleared. When bits 3 and 5 are set and bit 4 is cleared, the parity bit is transmitted and checked as set. When bit 5 is cleared, stick parity is disabled.
- Bit 6: This bit is the break control bit. Bit 6 is set to force a break condition; i.e., a condition where SOUT is forced to the spacing (cleared) state. When bit 6 is cleared, the break condition is disabled and has no affect on the transmitter logic; it only effects the serial output.
- Bit 7: This bit is the divisor latch access bit (DLAB). Bit 7 must be set to access the divisor latches of the baud generator during a read or write. Bit 7 must be cleared during a read or write to access the receiver buffer, the THR, or the IER.

line status register (LSR)†

The LSR provides information to the CPU concerning the status of data transfers. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bit 0: This bit is the data ready (DR) indicator for the receiver. Bit 0 is set whenever a complete incoming character has been received and transferred into the RBR or the FIFO. Bit 0 is cleared by reading all of the data in the RBR or the FIFO.
- Bit 1‡: This bit is the overrun error (OE) indicator. When bit 1 is set, it indicates that before the character in the RBR is read, it is overwritten by the next character transferred into the register. The OE indicator is cleared every time the CPU reads the contents of the LSR. If the FIFO mode data continues to fill the FIFO beyond the trigger level, an overrun error occurs only after the FIFO is full and the next character has been completely received in the shift register. An OE is indicated to the CPU as soon as it happens. The character in the shift register is overwritten, but it is not transferred to the FIFO.

† The line status register is intended for read operations only; writing to this register is not recommended outside of a factory testing environment.
‡ Bits 1 through 4 are the error conditions that produce a receiver line status interrupt.

PRINCIPLES OF OPERATION

line status register (LSR) (continued)†

- Bit 2‡: This bit is the parity error (PE) indicator. When bit 2 is set, it indicates that the parity of the received data character does not match the parity selected in the LCR (bit 4). The PE bit is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO.
- Bit 3‡: This bit is the framing error (FE) indicator. When bit 3 is set, it indicates that the received character did not have a valid (set) stop bit. The FE bit is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. The ACE tries to resynchronize after a framing error. To accomplish this, it is assumed that the framing error is due to the next start bit. The ACE samples this start bit twice and then accepts the input data.
- Bit 4‡: This bit is the break interrupt (BI) indicator. When bit 4 is set, it indicates that the received data input was held cleared for longer than a full-word transmission time. A full-word transmission time is defined as the total time of the start, data, parity, and stop bits. The BI bit is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. When a break occurs, only one 0 character is loaded into the FIFO. The next character transfer is enabled after SIN goes to the marking state and receives the next valid start bit.
- Bit 5: This bit is the THRE indicator. Bit 5 is set when the THR is empty, indicating that the ACE is ready to accept a new character. If the THRE interrupt is enabled when the THRE bit is set, an interrupt is generated. THRE is set when the contents of the THR are transferred to the transmitted shift register. This bit is cleared concurrent with the loading of the THR by the CPU. In the FIFO mode, this bit is set when the transmit FIFO is empty; it is cleared when at least one byte is written to the transmit FIFO.
- Bit 6: This bit is the transmitter empty (TEMT) indicator. Bit 6 is set when the THR and the TSR are both empty. When either the THR or the TSR contains a data character, the TEMT bit is cleared. In the FIFO mode, this bit is set when the transmitter FIFO and shift register are both empty.
- Bit 7: In the TL16C550B mode, this bit is always cleared. In the TL16C450 mode, this bit is always cleared. In the FIFO mode, LSR7 is set when there is at least one parity, framing, or break error in the FIFO. It is cleared when the microprocessor reads the LSR and there are no subsequent errors in the FIFO.

modem control register (MCR)

The MCR is an 8-bit register that controls an interface with a modem, data set, or peripheral device that is emulating a modem. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bit 0: This bit (DTR) controls the data terminal ready ($\overline{DTR}$) output. Setting bit 0 forces the $\overline{DTR}$ output to its low state. When bit 0 is cleared, $\overline{DTR}$ goes high.
- Bit 1: This bit (RTS) controls the request to send ($\overline{RTS}$) output in a manner identical to bit 0's control over the $\overline{DTR}$ output.
- Bit 2: This bit (OUT1) controls the output 1 ($\overline{OUT1}$) signal, a user-designated output signal, in a manner identical to bit 0's control over the $\overline{DTR}$ output.

† The line status register is intended for read operations only; writing to this register is not recommended outside of a factory testing environment.
‡ Bits 1 through 4 are the error conditions that produce a receiver line status interrupt.

PRINCIPLES OF OPERATION

modem control register (MCR) (continued)

- Bit 3: This bit (OUT2) controls the output 2 ($\overline{OUT2}$) signal, a user-designated output signal, in a manner identical to bit 0's control over the $\overline{DTR}$ output.
- Bit 4: This bit provides a local loop back feature for diagnostic testing of the ACE. When this bit is set, the following occurs:
  - The SOUT is set high.
  - The SIN is disconnected.
  - The output of the TSR is looped back into the receiver shift register input.
  - The four modem control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$) are disconnected.
  - The four modem control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT1}$, and $\overline{OUT2}$) are internally connected to the four modem control inputs.
  - The four modem control outputs are forced to their inactive (high) states.

  In the diagnostic mode, data that is transmitted is immediately received. This allows the processor to verify the transmit and receive data paths to the ACE. The receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational, but the modem control interrupt's sources are now the lower four bits of the MCR instead of the four modem control inputs. All interrupts are still controlled by the IER.
- Bits 5 – 7: These bits are permanently cleared.

modem status register (MSR)

The MSR is an 8-bit register that provides information about the current state of the control lines from the modem, data set, or peripheral device to the CPU. Additionally, four bits of this register provide change information; when a control input from the modem changes state, the appropriate bit is set. All four bits are cleared when the CPU reads the MSR. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bit 0: This bit is the change in clear-to-send (ΔCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input has changed states since the last time it was read by the CPU . When this bit is set and the modem status interrupt is enabled, a modem status interrupt is generated.
- Bit 1: This bit is the change in data set ready (ΔDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input has changed states since the last time it was read by the CPU. When this bit is set and the modem status interrupt is enabled, a modem status interrupt is generated.
- Bit 2: This bit is the trailing edge of the ring indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from a low to a high state. When this bit is set and the modem status interrupt is enabled, a modem status interrupt is generated.
- Bit 3: This bit is the change in data carrier detect (ΔDCD) indicator. Bit 3 indicates that the $\overline{DCD}$ input to the chip has changed states since the last time it was read by the CPU. When this bit is set and the modem status interrupt is enabled, a modem status interrupt is generated.
- Bit 4: This bit is the complement of the clear-to-send ($\overline{CTS}$) input. When bit 4 (loop) of the MCR is set, bit 4 is equivalent to the MCR bit 1 (RTS).
- Bit 5: This bit is the complement of the data set ready ($\overline{DSR}$) input. When bit 4 (loop) of the MCR is set, bit 5 is equivalent to the MCR bit 1 (DTR).

PRINCIPLES OF OPERATION

modem status register (MSR) (continued)

- Bit 6: This bit is the complement of the ring indicator ($\overline{RI}$) input. When bit 4 (loop) of the MCR is set, bit 6 is equivalent to the MCRs bit 2 (OUT1).
- Bit 7: This bit is the complement of the data carrier detect ($\overline{DCD}$) input. When bit 4 (loop) of the MCR is set, bit 7 is equivalent to the MCRs bit 3 (OUT2).

programmable baud generator

The ACE contains a programmable baud generator that takes a clock input in the range between dc and 8 MHz and divides it by a divisor in the range between 1 and (2^{16}–1). The output frequency of the baud generator is 16× the baud rate. The formula for the divisor is:

$$\text{divisor \#} = \text{XIN frequency input} \div (\text{desired baud rate} \times 16)$$

Two 8-bit registers, called divisor latches, store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization of the ACE in order to ensure desired operation of the baud generator. When either of the divisor latches is loaded, a 16-bit baud counter is also loaded to prevent long counts on initial load.

Tables 8 and 9 illustrate the use of the baud generator with crystal frequencies of 1.8432 MHz and 3.072 MHz respectively. For baud rates of 38.4 kbit/s and below, the error obtained is very small. The accuracy of the selected baud rate is dependent on the selected crystal frequency. Refer to Figure 16 for examples of typical clock circuits.

Table 8. Baud Rates Using a 1.8432-MHz Crystal

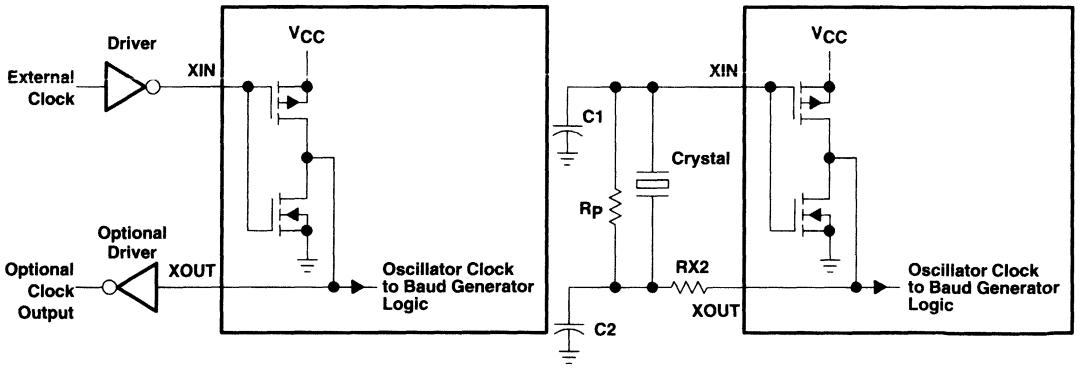
DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16× CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
1800	64	
2000	58	0.69
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19200	6	
38400	3	
56000	2	2.86

PRINCIPLES OF OPERATION

programmable baud generator (continued)

Table 9. Baud Rates Using a 3.072-MHz Crystal

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16× CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	
75	2560	
110	1745	0.026
134.5	1428	0.034
150	1280	
300	640	
600	320	
1200	160	
1800	107	0.312
2000	96	
2400	80	
3600	53	0.628
4800	40	
7200	27	1.23
9600	20	
19200	10	
38400	5	



TYPICAL CRYSTAL OSCILLATOR NETWORK

CRYSTAL	Rp	RX2	C1	C2
3.1 MHz	1 MΩ	1.5 kΩ	10-30 pF	40-60 pF
1.8 MHz	1 MΩ	1.5 kΩ	10-30 pF	40-60 pF

Figure 16. Typical Clock Circuits

PRINCIPLES OF OPERATION

receiver buffer register (RBR)

The ACE receiver section consists of a receiver shift register (RSR) and a RBR. The RBR is actually a 16-byte FIFO. Timing is supplied by the 16× receiver clock (RCLK). Receiver section control is a function of the ACE line control register.

The ACE RSR receives serial data from the SIN terminal. The RSR then deserializes the data and moves it into the RBR FIFO. In the TL16C450 mode, when a character is placed in the receiver buffer register and the received data available interrupt is enabled, an interrupt is generated. This interrupt is cleared when the data is read out of the RBR. In the FIFO mode, the interrupts are generated based on the control setup in the FIFO control register.

scratch register

The scratch register is an 8-bit register that is intended for the programmer's use as a scratchpad in the sense that it temporarily holds the programmer's data without affecting any other ACE operation.

transmitter holding register (THR)

The ACE transmitter section consists of a THR and a transmitter shift register (TSR). The THR is actually a 16-byte FIFO. Timing is supplied by the baud out ($\overline{\text{BAUDOUT}}$) clock signal. Transmitter section control is a function of the ACE's line control register.

The ACE THR receives data off the internal data bus and when the shift register is idle, moves it into the TSR. The TSR serializes the data and outputs it at the SOUT. In the TL16C450 mode, when the THR is empty and the transmitter holding register empty (THRE) interrupt is enabled, an interrupt is generated. This interrupt is cleared when a character is loaded into the register. In the FIFO mode, the interrupts are generated based on the control setup in the FIFO control register.

- Programmable Auto-$\overline{RTS}$ and Auto-$\overline{CTS}$
- In Auto-$\overline{CTS}$ Mode, $\overline{CTS}$ Controls Transmitter
- In Auto-$\overline{RTS}$ Mode, RCV FIFO Contents and Threshold Control $\overline{RTS}$
- Serial and Modem Control Outputs Drive a RJ11 Cable Directly When Equipment Is on the Same Power Drop
- Capable of Running With All Existing TL16C450 Software
- After Reset, All Registers Are Identical to the TL16C450 Register Set
- Up to 16-MHz Clock Rate for Up to 1-Mbaud Operation
- In the TL16C450 Mode, Hold and Shift Registers Eliminate the Need for Precise Synchronization Between the CPU and Serial Data
- Programmable Baud Rate Generator Allows Division of Any Input Reference Clock by 1 to ($2^{16}-1$) and Generates an Internal 16× Clock
- Standard Asynchronous Communication Bits (Start, Stop, and Parity) Added to or Deleted From the Serial Data Stream
- Independent Receiver Clock Input
- Transmit, Receive, Line Status, and Data Set Interrupts Independently Controlled
- Fully Programmable Serial Interface Characteristics:
  - 5-, 6-, 7-, or 8-Bit Characters
  - Even-, Odd-, or No-Parity Bit Generation and Detection
  - 1-, 1 1/2-, or 2-Stop Bit Generation
  - Baud Generation (dc to 1 Mbit/s)
- False-Start Bit Detection
- Complete Status Reporting Capabilities
- 3-State Output TTL Drive Capabilities for Bidirectional Data Bus and Control Bus
- Line Break Generation and Detection
- Internal Diagnostic Capabilities:
  - Loopback Controls for Communications Link Fault Isolation
  - Break, Parity, Overrun, and Framing Error Simulation
- Fully Prioritized Interrupt System Controls
- Modem Control Functions ($\overline{CTS}$, $\overline{RTS}$, $\overline{DSR}$, $\overline{DTR}$, $\overline{RI}$, and $\overline{DCD}$)

description

The TL16C550C is a functional upgrade of the TL16C550B asynchronous communications element (ACE), which in turn is a functional upgrade of the TL16C450. Functionally equivalent to the TL16C450 on power up (character or TL16C450 mode), the TL16C550C, like the TL16C550B, can be placed in an alternate mode (FIFO mode). This relieves the CPU of excessive software overhead by buffering received and transmitted characters. The receiver and transmitter FIFOs store up to 16 bytes including three additional bits of error status per byte for the receiver FIFO. In the FIFO mode, there is a selectable autoflow control feature that can significantly reduce software overload and increase system efficiency by automatically controlling serial data flow using $\overline{RTS}$ output and $\overline{CTS}$ input signals.

The TL16C550C performs serial-to-parallel conversion on data received from a peripheral device or modem and parallel-to-serial conversion on data received from its CPU. The CPU can read the ACE status at any time. The ACE includes complete modem control capability and a processor interrupt system that can be tailored to minimize software management of the communications link.

The TL16C550C ACE includes a programmable baud rate generator capable of dividing a reference clock by divisors from 1 to 65535 and producing a 16× reference clock for the internal transmitter logic. Provisions are included to use this 16× clock for the receiver logic. The ACE accommodates a 1-Mbaud serial rate (16-MHz input clock) so that a bit time is 1 µs and a typical character time is 10 µs (start bit, 8 data bits, stop bit).

Two of the TL16C450 terminal functions on the TL16C550C have been changed to $\overline{TXRDY}$ and $\overline{RXRDY}$, which provide signaling to a DMA controller.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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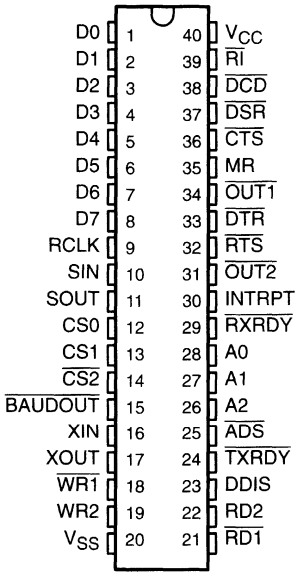
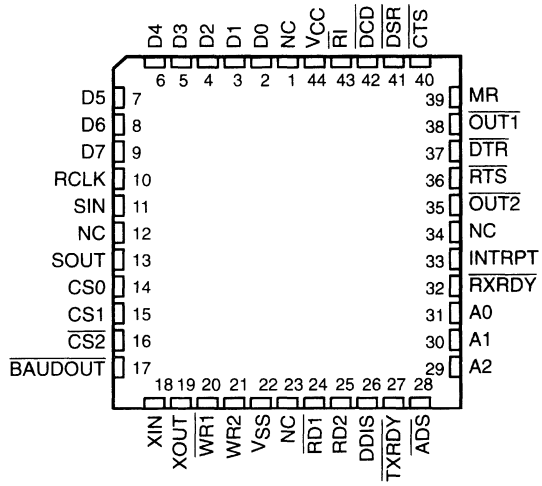
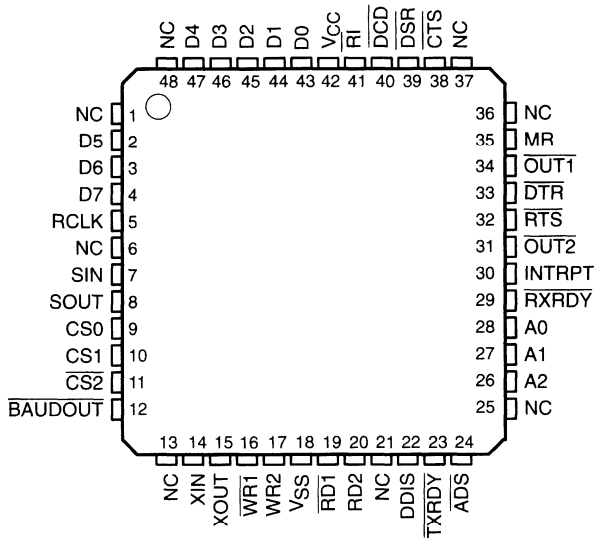
N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



PT PACKAGE
(TOP VIEW)



NC – No internal connection

detailed description

autoflow control

Auto-flow control is comprised of auto-$\overline{CTS}$ and auto-$\overline{RTS}$. With auto-$\overline{CTS}$, the $\overline{CTS}$ input must be active before the transmitter FIFO can emit data (see Figure 1). With auto-$\overline{RTS}$, $\overline{RTS}$ becomes active when the receiver needs more data and notifies the sending serial device (see Figure 1). When $\overline{RTS}$ is connected to $\overline{CTS}$, data transmission does not occur unless the receiver FIFO has space for the data; thus, overrun errors are eliminated using ACE1 and ACE2 from a TLC16C550C with the autoflow control enabled. If not, overrun errors occur when the transmit data rate exceeds the receiver FIFO read latency.

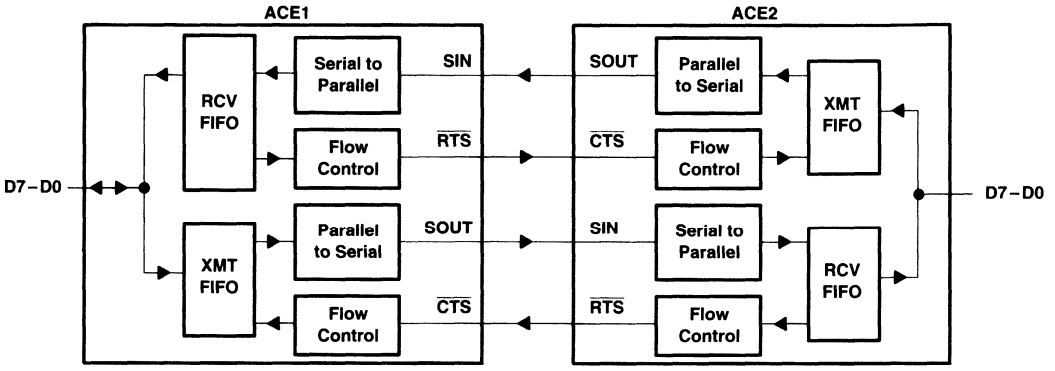


Figure 1. Autoflow Control (Auto-$\overline{RTS}$ and Auto-$\overline{CTS}$) Example

auto-$\overline{RTS}$ (see Figure 1)

Auto-$\overline{RTS}$ data flow control originates in the receiver timing and control block (see functional block diagram) and is linked to the programmed receiver FIFO trigger level. When the receiver FIFO level reaches a trigger level of 1, 4, or 8 (see Figure 3), $\overline{RTS}$ is deasserted. With trigger levels of 1, 4, and 8, the sending ACE may send an additional byte after the trigger level is reached (assuming the sending ACE has another byte to send) because it may not recognize the deassertion of $\overline{RTS}$ until after it has begun sending the additional byte. $\overline{RTS}$ is automatically reasserted once the RCV FIFO is emptied by reading the receiver buffer register.

When the trigger level is 14 (see Figure 6), $\overline{RTS}$ is deasserted after the first data bit of the 16th character is present on the SIN line. $\overline{RTS}$ is reasserted when the RCV FIFO has at least one available byte space.

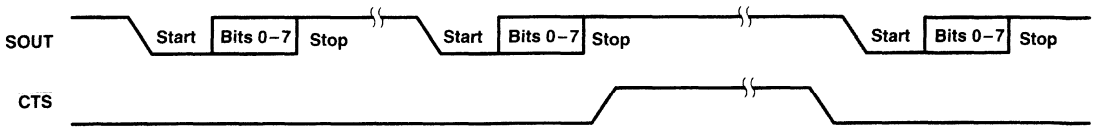
auto-$\overline{CTS}$ (see Figure 1)

The transmitter circuitry checks $\overline{CTS}$ before sending the next data byte. When $\overline{CTS}$ is active, it sends the next byte. To stop the transmitter from sending the following byte, $\overline{CTS}$ must be released before the middle of the last stop bit that is currently being sent (see Figure 2). The auto-$\overline{CTS}$ function reduces interrupts to the host system. When flow control is enabled, $\overline{CTS}$ level changes do not trigger host interrupts because the device automatically controls its own transmitter. Without auto-$\overline{CTS}$, the transmitter sends any data present in the transmit FIFO and a receiver overrun error may result.

enabling autoflow control and auto-$\overline{CTS}$

Auto-flow control is enabled by setting modem control register bits 5 (autoflow enable or AFE) and 1 (RTS) to 1. Auto-flow incorporates both auto-$\overline{RTS}$ and auto-$\overline{CTS}$. When only auto-$\overline{CTS}$ is desired, bit 1 in the modem control register should be cleared (this assumes that a control signal is driving $\overline{CTS}$).

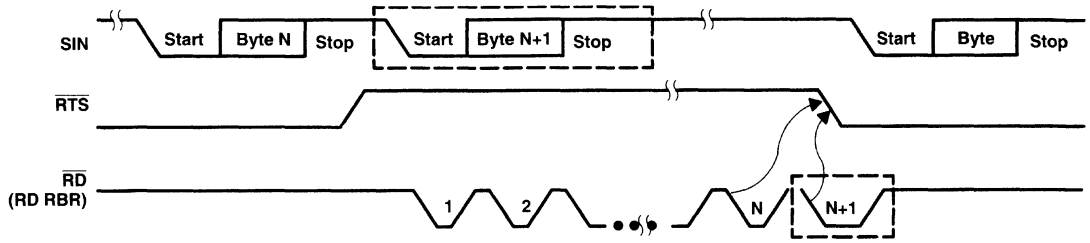
auto-$\overline{CTS}$ and auto-$\overline{RTS}$ functional timing



NOTES: A. When $\overline{CTS}$ is low, the transmitter keeps sending serial data out.
B. If $\overline{CTS}$ goes high before the middle of the last stop bit of the current byte, the transmitter finishes sending the current byte but it does not send the next byte.
C. When $\overline{CTS}$ goes from high to low, the transmitter begins sending data again.

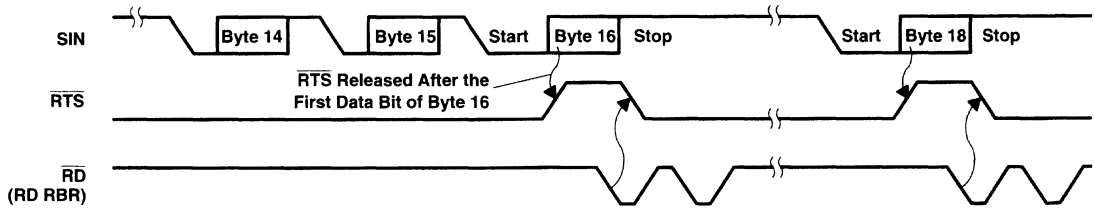
Figure 2. $\overline{CTS}$ Functional Timing Waveforms

The receiver FIFO trigger level can be set to 1, 4, 8, or 14 bytes. These are described in Figures 3 and 4.



NOTES: A. N = RCV FIFO trigger level (1, 4, or 8 bytes)
B. The two blocks in dashed lines cover the case where an additional byte is sent as described in the preceding auto-$\overline{RTS}$ section.

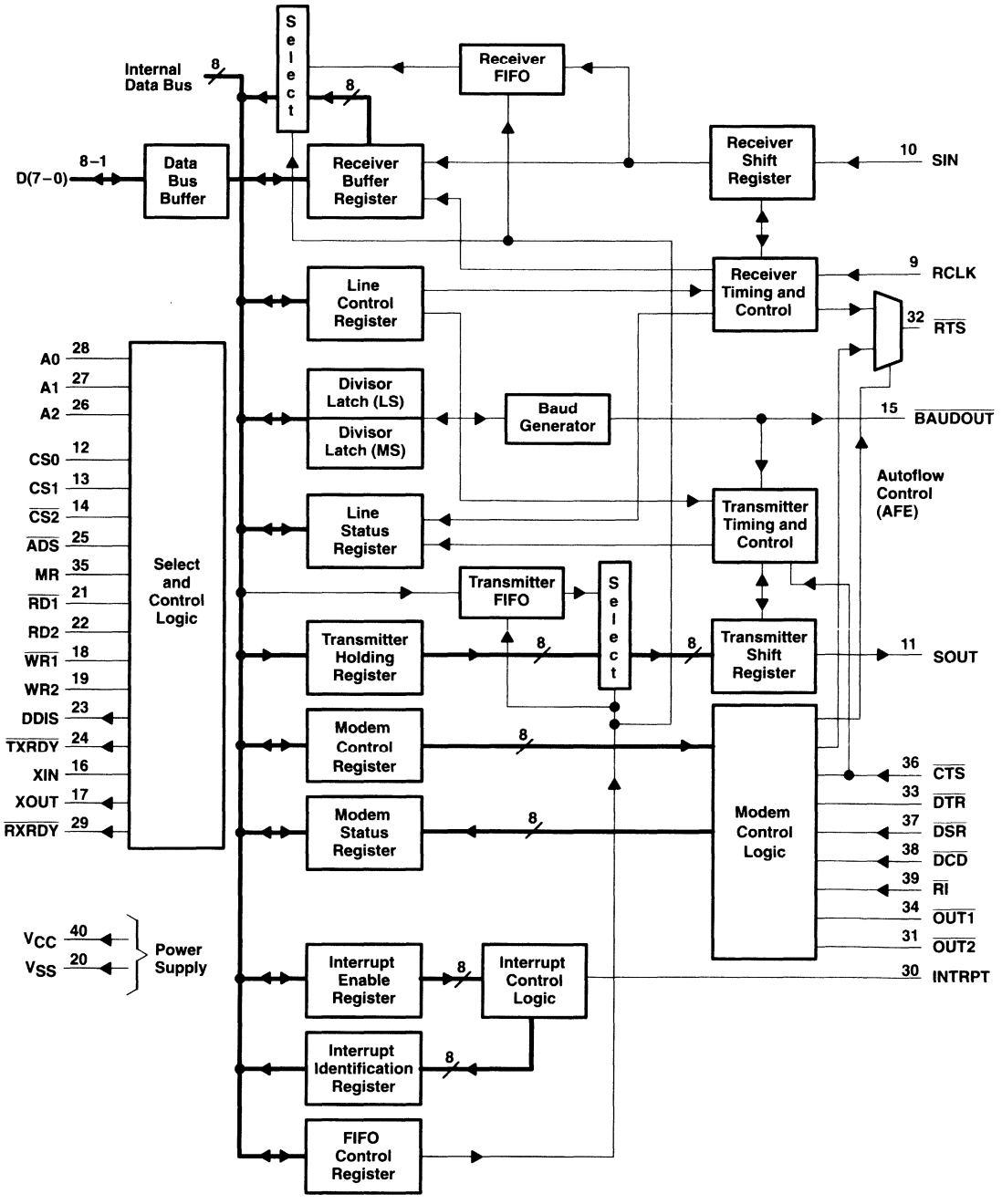
Figure 3. $\overline{RTS}$ Functional Timing Waveforms, RCV FIFO Trigger Level = 1,4, or 8 Bytes



NOTES: A. $\overline{RTS}$ is deasserted when the receiver receives the first data bit of the sixteenth byte. The receive FIFO is full after finishing the sixteenth byte.
B. $\overline{RTS}$ is asserted again when there is at least one byte of space available and no incoming byte is in processing or there is more than one byte of space available.
C. When the receive FIFO is full, the first receive buffer register read reasserts $\overline{RTS}$.

Figure 4. $\overline{RTS}$ Functional Timing Waveforms, RCV FIFO Trigger Level = 14 Bytes

functional block diagram



NOTE A: Terminal numbers shown are for the N package.

Terminal Functions

TERMINAL NAME	TERMINAL NO. N	TERMINAL NO. FN	TERMINAL NO. PT	I/O	DESCRIPTION
A0 A1 A2	28 27 26	31 30 29	28 27 26	I	Register select. A0–A2 are used during read and write operations to select the ACE register to read from or write to. Refer to Table 1 for register addresses and refer to $\overline{ADS}$ description.
$\overline{ADS}$	25	28	24	I	Address strobe. When $\overline{ADS}$ is active (low), A0, A1, and A2 and CS0, CS1, and $\overline{CS2}$ drive the internal select logic directly; when $\overline{ADS}$ is high, the register select and chip select signals are held at the logic levels they were in when the low-to-high transition of $\overline{ADS}$ occurred.
$\overline{BAUDOUT}$	15	17	12	O	Baud out. $\overline{BAUDOUT}$ is a 16× clock signal for the transmitter section of the ACE. The clock rate is established by the reference oscillator frequency divided by a divisor specified by the baud generator divisor latches. $\overline{BAUDOUT}$ may also be used for the receiver section by tying this output to RCLK.
CS0 CS1 $\overline{CS2}$	12 13 14	14 15 16	9 10 11	I	Chip select. When CS0 and CS1 are high and $\overline{CS2}$ is low, these three inputs select the ACE. When any of these inputs are inactive, the ACE remains inactive (refer to $\overline{ADS}$ description).
$\overline{CTS}$	36	40	38	I	Clear to send. $\overline{CTS}$ is a modem status signal. Its condition can be checked by reading bit 4 (CTS) of the modem status register. Bit 0 (ΔCTS) of the modem status register indicates that $\overline{CTS}$ has changed states since the last read from the modem status register. If the modem status interrupt is enabled when $\overline{CTS}$ changes levels and the auto-$\overline{CTS}$ mode is not enabled, an interrupt is generated. $\overline{CTS}$ is also used in the auto-$\overline{CTS}$ mode to control the transmitter.
D0 D1 D2 D3 D4 D5 D6 D7	1 2 3 4 5 6 7 8	2 3 4 5 6 7 8 9	43 44 45 46 47 2 3 4	I/O	Data bus. Eight data lines with 3-state outputs provide a bidirectional path for data, control, and status information between the ACE and the CPU.
$\overline{DCD}$	38	42	40	I	Data carrier detect. $\overline{DCD}$ is a modem status signal. Its condition can be checked by reading bit 7 (DCD) of the modem status register. Bit 3 (ΔDCD) of the modem status register indicates that $\overline{DCD}$ has changed states since the last read from the modem status register. If the modem status interrupt is enabled when $\overline{DCD}$ changes levels, an interrupt is generated.
DDIS	23	26	22	O	Driver disable. $\overline{DDIS}$ is active (high) when the CPU is not reading data. When active, $\overline{DDIS}$ can disable an external transceiver.
$\overline{DSR}$	37	41	39	I	Data set ready. $\overline{DSR}$ is a modem status signal. Its condition can be checked by reading bit 5 (DSR) of the modem status register. Bit 1 (ΔDSR) of the modem status register indicates $\overline{DSR}$ has changed levels since the last read from the modem status register. If the modem status interrupt is enabled when $\overline{DSR}$ changes levels, an interrupt is generated.
$\overline{DTR}$	33	37	33	O	Data terminal ready. When active (low), $\overline{DTR}$ informs a modem or data set that the ACE is ready to establish communication. $\overline{DTR}$ is placed in the active level by setting the DTR bit of the modem control register. $\overline{DTR}$ is placed in the inactive level either as a result of a master reset, during loop mode operation, or clearing the DTR bit.
INTRPT	30	33	30	O	Interrupt. When active (high), INTRPT informs the CPU that the ACE has an interrupt to be serviced. Four conditions that cause an interrupt to be issued are: a receiver error, received data that is available or timed out (FIFO mode only), an empty transmitter holding register, or an enabled modem status interrupt. INTRPT is reset (deactivated) either when the interrupt is serviced or as a result of a master reset.
MR	35	39	35	I	Master reset. When active (high), MR clears most ACE registers and sets the levels of various output signals (refer to Table 2).

Terminal Functions (Continued)

TERMINAL NAME	NO. N	NO. FN	NO. PT	I/O	DESCRIPTION
$\overline{OUT1}$ $\overline{OUT2}$	34 31	38 35	34 31	O	Outputs 1 and 2. These are user-designated output terminals that are set to the active (low) level by setting respective modem control register (MCR) bits (OUT1 and OUT2). $\overline{OUT1}$ and $\overline{OUT2}$ are set to inactive the (high) level as a result of master reset, during loop mode operations, or by clearing bit 2 (OUT1) or bit 3 (OUT2) of the MCR.
RCLK	9	10	5	I	Receiver clock. RCLK is the 16× baud rate clock for the receiver section of the ACE.
$\overline{RD1}$ RD2	21 22	24 25	19 20	I	Read inputs. When either $\overline{RD1}$ or RD2 is active (low or high respectively) while the ACE is selected, the CPU is allowed to read status information or data from a selected ACE register. Only one of these inputs is required for the transfer of data during a read operation; the other input should be tied to its inactive level (i.e., RD2 tied low or $\overline{RD1}$ tied high).
$\overline{RI}$	39	43	41	I	Ring indicator. $\overline{RI}$ is a modem status signal. Its condition can be checked by reading bit 6 (RI) of the modem status register. Bit 2 (TERI) of the modem status register indicates that $\overline{RI}$ has transitioned from a low to a high level since the last read from the modem status register. If the modem status interrupt is enabled when this transition occurs, an interrupt is generated.
$\overline{RTS}$	32	36	32	O	Request to send. When active, $\overline{RTS}$ informs the modem or data set that the ACE is ready to receive data. $\overline{RTS}$ is set to the active level by setting the RTS modem control register bit and is set to the inactive (high) level either as a result of a master reset or during loop mode operations or by clearing bit 1 (RTS) of the MCR. In the auto-$\overline{RTS}$ mode, $\overline{RTS}$ is set to the inactive level by the receiver threshold control logic.
$\overline{RXRDY}$	29	32	29	O	Receiver ready. Receiver direct memory access (DMA) signalling is available with $\overline{RXRDY}$. When operating in the FIFO mode, one of two types of DMA signalling can be selected using the FIFO control register bit 3 (FCR3). When operating in the TL16C450 mode, only DMA mode 0 is allowed. Mode 0 supports single-transfer DMA in which a transfer is made between CPU bus cycles. Mode 1 supports multitransfer DMA in which multiple transfers are made continuously until the receiver FIFO has been emptied. In DMA mode 0 (FCR0 = 0 or FCR0 = 1, FCR3 = 0), when there is at least one character in the receiver FIFO or receiver holding register, $\overline{RXRDY}$ is active (low). When $\overline{RXRDY}$ has been active but there are no characters in the FIFO or holding register, $\overline{RXRDY}$ goes inactive (high). In DMA mode 1 (FCR0 = 1, FCR3 = 1), when the trigger level or the time-out has been reached, $\overline{RXRDY}$ goes active (low); when it has been active but there are no more characters in the FIFO or holding register, it goes inactive (high).
SIN	10	11	7	I	Serial data input. SIN is serial data input from a connected communications device
SOUT	11	13	8	O	Serial data output. SOUT is composite serial data output to a connected communication device. SOUT is set to the marking (high) level as a result of master reset.
$\overline{TXRDY}$	24	27	23	O	Transmitter ready. Transmitter DMA signalling is available with $\overline{TXRDY}$. When operating in the FIFO mode, one of two types of DMA signalling can be selected using FCR3. When operating in the TL16C450 mode, only DMA mode 0 is allowed. Mode 0 supports single-transfer DMA in which a transfer is made between CPU bus cycles. Mode 1 supports multitransfer DMA in which multiple transfers are made continuously until the transmit FIFO has been filled.
V_{CC}	40	44	42		5-V supply voltage
V_{SS}	20	22	18		Supply common
$\overline{WR1}$ WR2	18 19	20 21	16 17	I	Write inputs. When either $\overline{WR1}$ or WR2 is active (low or high respectively) and while the ACE is selected, the CPU is allowed to write control words or data into a selected ACE register. Only one of these inputs is required to transfer data during a write operation; the other input should be tied to its inactive level (i.e., WR2 tied low or $\overline{WR1}$ tied high).
XIN XOUT	16 17	18 19	14 15	I/O	External clock. XIN and XOUT connect the ACE to the main timing reference (clock or crystal).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Input voltage range at any input, V_I ..... −0.5 V to 7 V
Output voltage range, V_O ..... −0.5 V to 7 V
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Case temperature for 10 seconds, T_C: FN package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N or PT package ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2		V_{CC}	V
Low-level input voltage, V_{IL}	−0.5		0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{OH}§	High-level output voltage	I_{OH} = −1 mA	2.4			V
V_{OL}§	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
I_I	Input current	V_{CC} = 5.25 V, V_{SS} = 0, V_I = 0 to 5.25 V, All other terminals floating			10	μA
I_{OZ}	High-impedance-state output current	V_{CC} = 5.25 V, V_{SS} = 0, V_O = 0 to 5.25 V, Chip selected in write mode or chip deselect			±20	μA
I_{CC}	Supply current	V_{CC} = 5.25 V, T_A = 25°C, SIN, $\overline{DSR}$, $\overline{DCD}$, $\overline{CTS}$, and $\overline{RI}$ at 2 V, All other inputs at 0.8 V, XTAL1 at 4 MHz, No load on outputs, Baud rate = 50 kbit/s			10	mA
$C_{i(CLK)}$	Clock input capacitance	V_{CC} = 0, V_{SS} = 0, f = 1 MHz, T_A = 25°C, All other terminals grounded		15	20	pF
$C_{o(CLK)}$	Clock output capacitance			20	30	pF
C_i	Input capacitance			6	10	pF
C_o	Output capacitance			10	20	pF

‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.
§ These parameters apply for all outputs except XOUT.

system timing requirements over recommended ranges of supply voltage and operating free-air temperature

		ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{cR}	Cycle time, read ($t_{w7} + t_{d8} + t_{d9}$)	RC			87		ns
t_{cW}	Cycle time, write ($t_{w6} + t_{d5} + t_{d6}$)	WC			87		ns
t_{w1}	Pulse duration, clock high	t_{XH}	5	f = 16 MHz Max	25		ns
t_{w2}	Pulse duration, clock low	t_{XL}	5	f = 16 MHz Max	25		ns
t_{w5}	Pulse duration, $\overline{ADS}$ low	t_{ADS}	6, 7		9		ns
t_{w6}	Pulse duration, $\overline{WR}$	t_{WR}	6		40		ns
t_{w7}	Pulse duration, $\overline{RD}$	t_{RD}	7		40		ns
t_{w8}	Pulse duration, MR	t_{MR}			1		µs
t_{su1}	Setup time, address valid before $\overline{ADS}\uparrow$	t_{AS}	6, 7		8		ns
t_{su2}	Setup time, CS valid before $\overline{ADS}\uparrow$	t_{CS}	6, 7		8		ns
t_{su3}	Setup time, data valid before $\overline{WR1}\downarrow$ or WR2$\uparrow$	t_{DS}	6		15		ns
t_{su4}	Setup time, $\overline{CTS}\uparrow$ before midpoint of stop bit		17			10	ns
t_{h1}	Hold time, address low after $\overline{ADS}\uparrow$	t_{AH}	6, 7		0		ns
t_{h2}	Hold time, CS valid after $\overline{ADS}\uparrow$	t_{CH}	6, 7		0		ns
t_{h3}	Hold time, CS valid after $\overline{WR1}\uparrow$ or WR2$\downarrow$	t_{WCS}	6		10		ns
t_{h4}	Hold time, address valid after $\overline{WR1}\uparrow$ or WR2$\downarrow$	t_{WA}	6		10		ns
t_{h5}	Hold time, data valid after $\overline{WR1}\uparrow$ or WR2$\downarrow$	t_{DH}	6		5		ns
t_{h6}	Hold time, chip select valid after $\overline{RD1}\uparrow$ or RD2$\downarrow$	t_{RCS}	7		10		ns
t_{h7}	Hold time, address valid after $\overline{RD1}\uparrow$ or RD2$\downarrow$	t_{RA}	7		20		ns
t_{d4}†	Delay time, CS valid before $\overline{WR1}\downarrow$ or WR2$\uparrow$	t_{CSW}	6		7		ns
t_{d5}†	Delay time, address valid before $\overline{WR1}\downarrow$ or WR2$\uparrow$	t_{AW}	6		7		ns
t_{d6}†	Delay time, write cycle, WR1$\uparrow$ or WR2$\downarrow$ to $\overline{ADS}\downarrow$	t_{WC}	6		40		ns
t_{d7}†	Delay time, CS valid to $\overline{RD1}\downarrow$ or RD2$\uparrow$	t_{CSR}	7		7		ns
t_{d8}†	Delay time, address valid to $\overline{RD1}\downarrow$ or RD2$\uparrow$	t_{AR}	7		7		ns
t_{d9}	Delay time, read cycle, $\overline{RD1}\uparrow$ or RD2$\downarrow$ to $\overline{ADS}\downarrow$	tRC	7		40		ns
t_{d10}	Delay time, $\overline{RD1}\downarrow$ or RD2$\uparrow$ to data valid	t_{RVD}	7	C_L = 75 pF	45		ns
t_{d11}	Delay time, $\overline{RD1}\uparrow$ or RD2$\downarrow$ to floating data	t_{HZ}	7	C_L = 75 pF	20		ns

† Only applies when $\overline{ADS}$ is low

system switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 2)

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$t_{dis(R)}$	Disable time, $\overline{RD1}\downarrow\uparrow$ or RD2$\uparrow\downarrow$ to DDIS$\uparrow\downarrow$	t_{RDD}	7	C_L = 75 pF	20		ns

NOTE 2: Charge and discharge times are determined by V_{OL}, V_{OH}, and external loading.

baud generator switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 75 pF

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{w3}	Pulse duration, $\overline{BAUDOUT}$ low	t_{LW}	5	f = 16 MHz, CLK ÷ 2	50		ns
t_{w4}	Pulse duration, $\overline{BAUDOUT}$ high	t_{HW}	5	f = 16 MHz, CLK ÷ 2	50		ns
t_{d1}	Delay time, XIN$\uparrow$ to $\overline{BAUDOUT}\uparrow$	t_{BLD}	5			45	ns
t_{d2}	Delay time, XIN$\uparrow\downarrow$ to $\overline{BAUDOUT}\downarrow$	t_{BHD}	5			45	ns

receiver switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 3)

	PARAMETER	ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d12}	Delay time, RCLK to sample	t_{SCD}	8			10	ns
t_{d13}	Delay time, stop to set INTRPT or read RBR to LSI interrupt or stop to $\overline{RXRDY}\downarrow$	t_{SINT}	8, 9, 10, 11, 12			1	RCLK cycle
t_{d14}	Delay time, read RBR/LSR to reset INTRPT	t_{RINT}	8, 9, 10, 11, 12	C_L = 75 pF		70	ns

NOTE 3: In the FIFO mode, the read cycle (RC) = 425 ns (min) between reads of the receive FIFO and the status registers (interrupt identification register or line status register).

transmitter switching characteristics over recommended ranges of supply voltage and operating free-air temperature

	PARAMETER	ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d15}	Delay time, initial write to transmit start	t_{IRS}	13		8	24	baudout cycles
t_{d16}	Delay time, start to INTRPT	t_{STI}	13		8	10	baudout cycles
t_{d17}	Delay time, $\overline{WR}$ (WR THR) to reset INTRPT	t_{HR}	13	C_L = 75 pF		50	ns
t_{d18}	Delay time, initial write to INTRPT (THRE†)	t_{SI}	13		16	34	baudout cycles
t_{d19}	Delay time, read IIR† to reset INTRPT (THRE†)	t_{IR}	13	C_L = 75 pF		35	ns
t_{d20}	Delay time, write to $\overline{TXRDY}$ inactive	t_{WXI}	14,15	C_L = 75 pF		35	ns
t_{d21}	Delay time, start to $\overline{TXRDY}$ active	t_{SXA}	14,15	C_L = 75 pF		9	baudout cycles

† THRE = transmitter holding register empty; IIR = interrupt identification register.

modem control switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 75 pF

	PARAMETER	ALT. SYMBOL	FIGURE	MIN	MAX	UNIT
t_{d22}	Delay time, WR MCR to output	t_{MDO}	16		50	ns
t_{d23}	Delay time, modem interrupt to set INTRPT	t_{SIM}	16		35	ns
t_{d24}	Delay time, RD MSR to reset INTRPT	t_{RIM}	16		40	ns
t_{d25}	Delay time, $\overline{CTS}$ low to SOUT$\downarrow$		17		24	baudout cycles
t_{d26}	Delay time, RCV threshold byte to $\overline{RTS}\uparrow$		18		2	baudout cycles
t_{d27}	Delay time, read of last byte in receive FIFO to $\overline{RTS}\downarrow$		18		2	baudout cycles
t_{d28}	Delay time, first data bit of 16th character to $\overline{RTS}\uparrow$		19		2	baudout cycles
t_{d29}	Delay time, $\overline{RBRRD}$ low to $\overline{RTS}\downarrow$		19		2	baudout cycles

PARAMETER MEASUREMENT INFORMATION

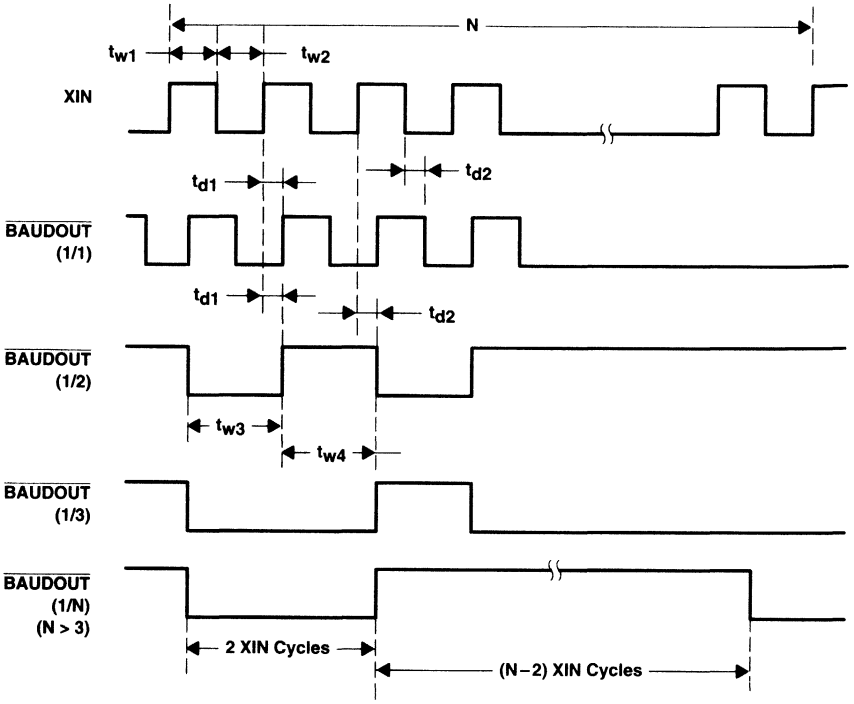
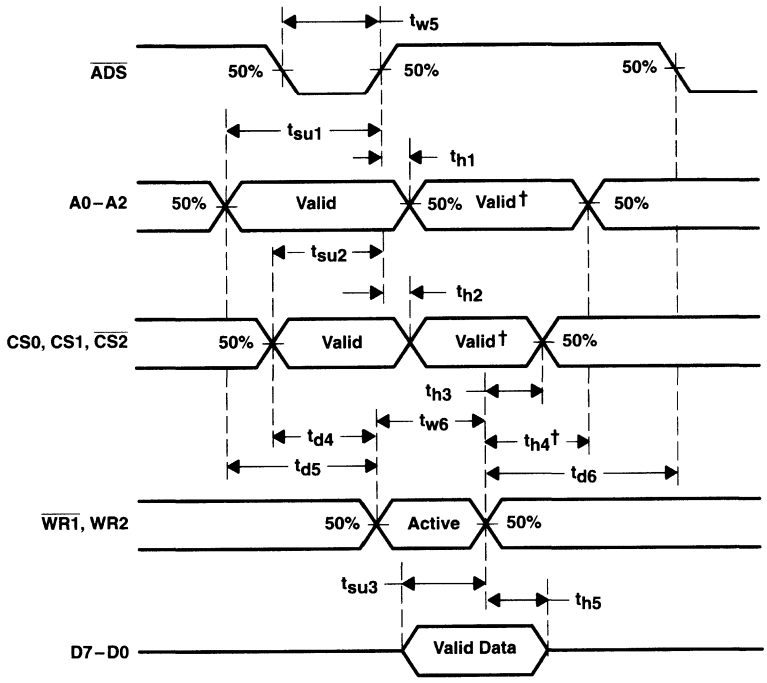


Figure 5. Baud Generator Timing Waveforms

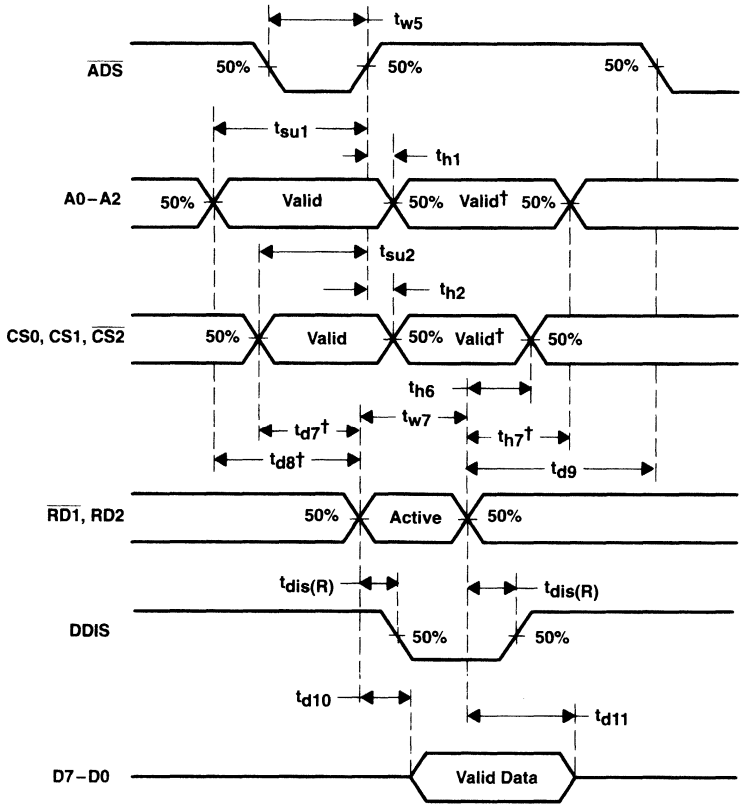
PARAMETER MEASUREMENT INFORMATION



† Applicable only when $\overline{ADS}$ is low

Figure 6. Write Cycle Timing Waveforms

PARAMETER MEASUREMENT INFORMATION



† Applicable only when $\overline{ADS}$ is low

Figure 7. Read Cycle Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

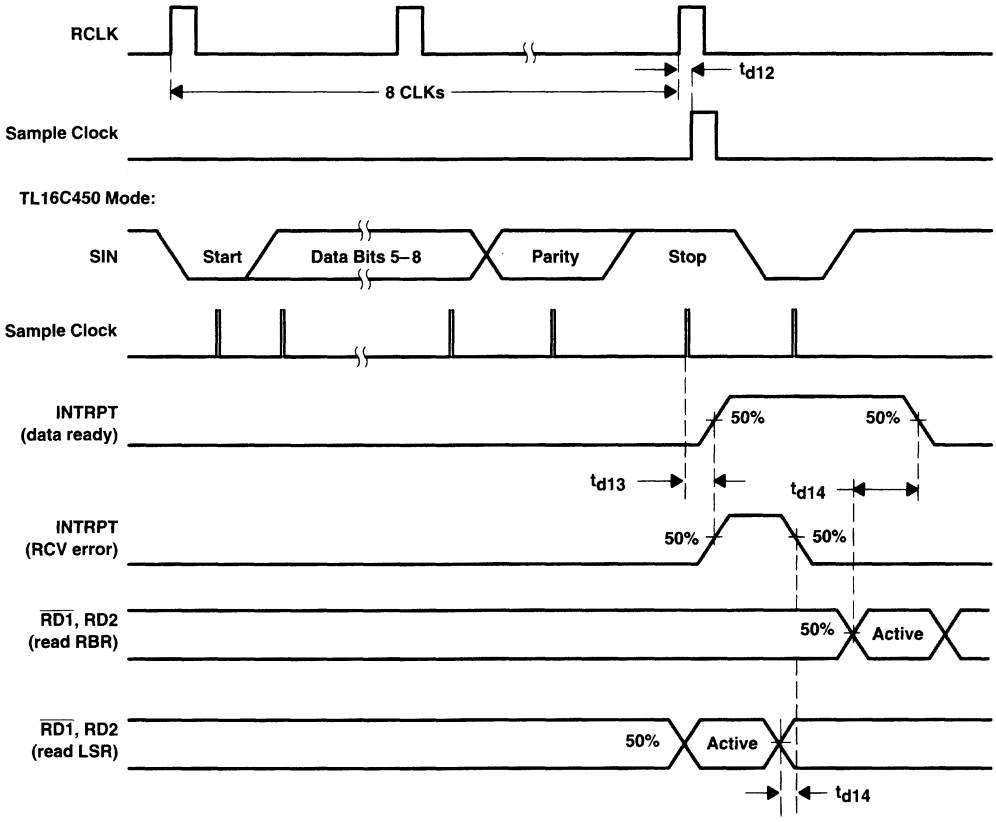
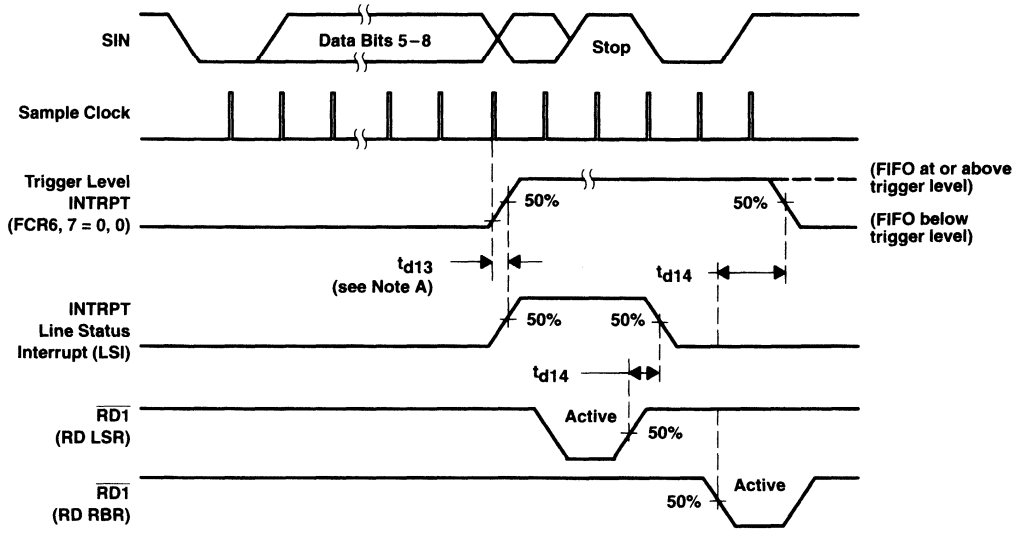


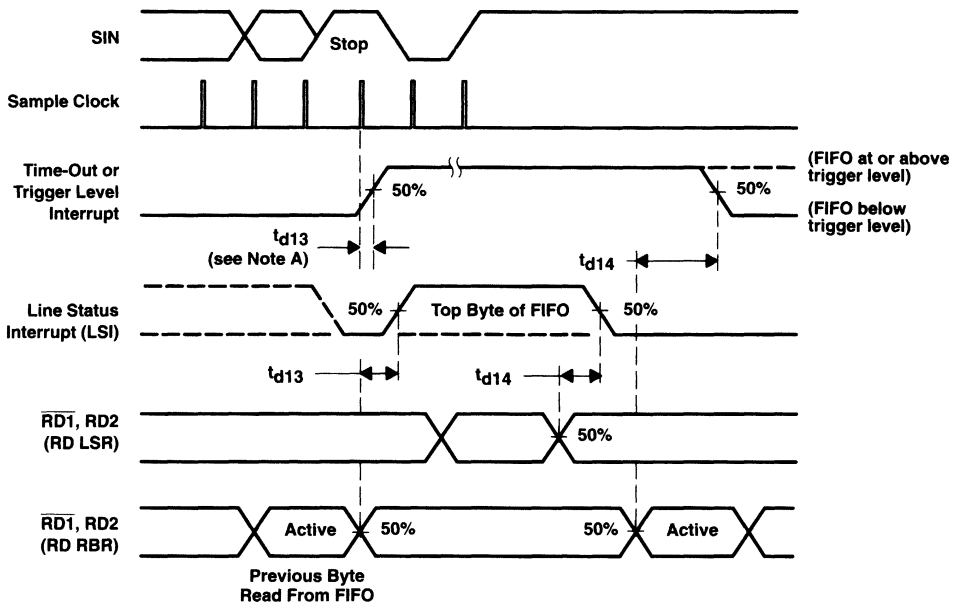
Figure 8. Receiver Timing Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: For a time-out interrupt, t_{d13} = 9 RCLKs.

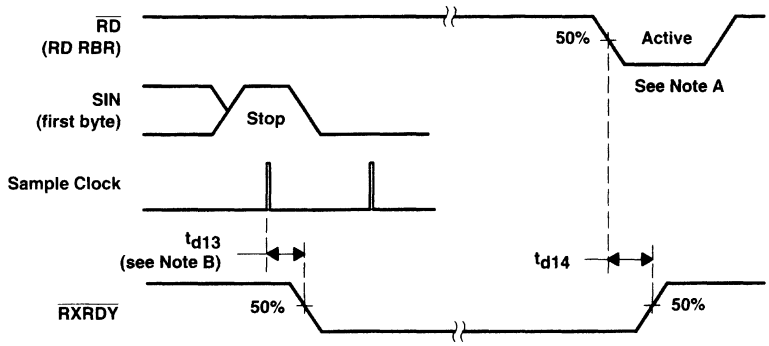
Figure 9. Receive FIFO First Byte (Sets DR Bit) Waveforms



NOTE A: For a time-out interrupt, t_{d13} = 9 RCLKs.

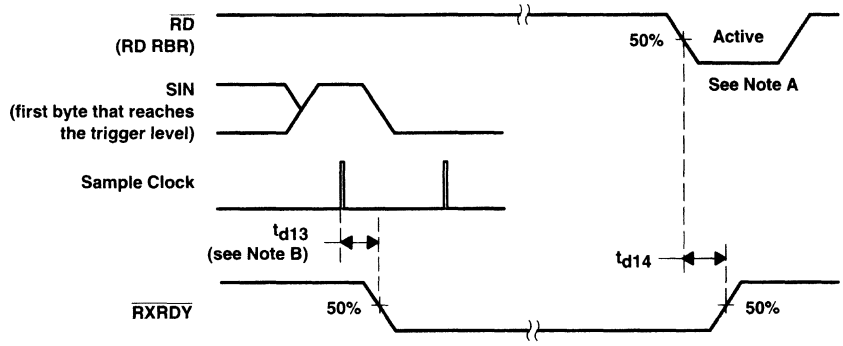
Figure 10. Receive FIFO Bytes Other Than the First Byte (DR Internal Bit Already Set) Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: This is the reading of the last byte in the FIFO.

Figure 11. Receiver Ready ($\overline{RXRDY}$) Waveforms, FCR0 = 0 or FCR0 = 1 and FCR3 = 0 (Mode 0)



NOTES: A. This is the reading of the last byte in the FIFO.
B. For a time-out interrupt, t_{d13} = 9 RCLKs.

Figure 12. Receiver Ready ($\overline{RXRDY}$) Waveforms, FCR0 = 1 or FCR3 = 1 (Mode 1)

PARAMETER MEASUREMENT INFORMATION

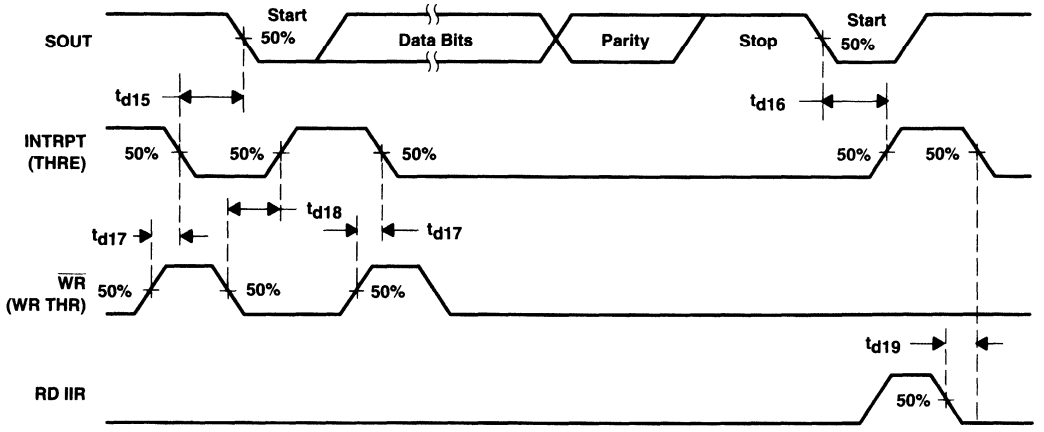


Figure 13. Transmitter Timing Waveforms

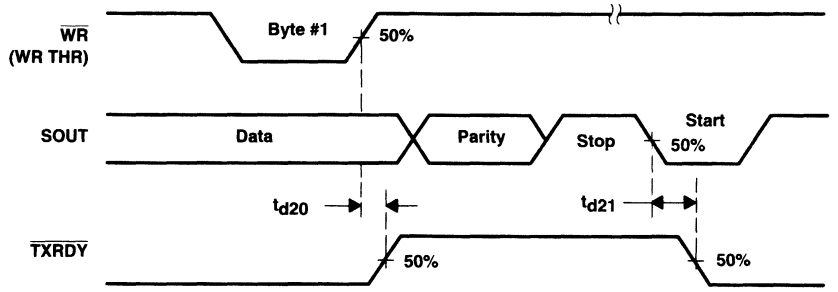


Figure 14. Transmitter Ready ($\overline{\text{TXRDY}}$) Waveforms, FCR0 = 0 or FCR0 = 1 and FCR3 = 0 (Mode 0)

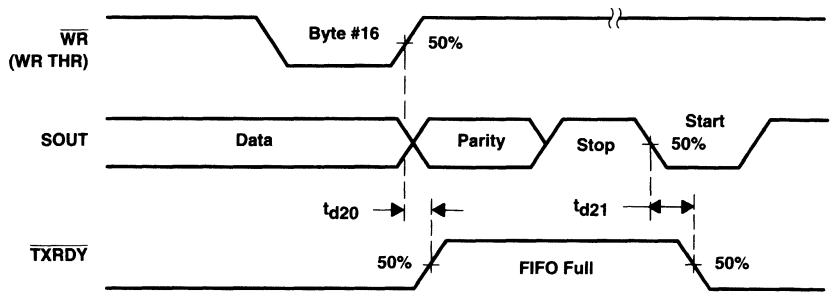


Figure 15. Transmitter Ready ($\overline{\text{TXRDY}}$) Waveforms, FCR0 = 1 and FCR3 = 1 (Mode 1)

PARAMETER MEASUREMENT INFORMATION

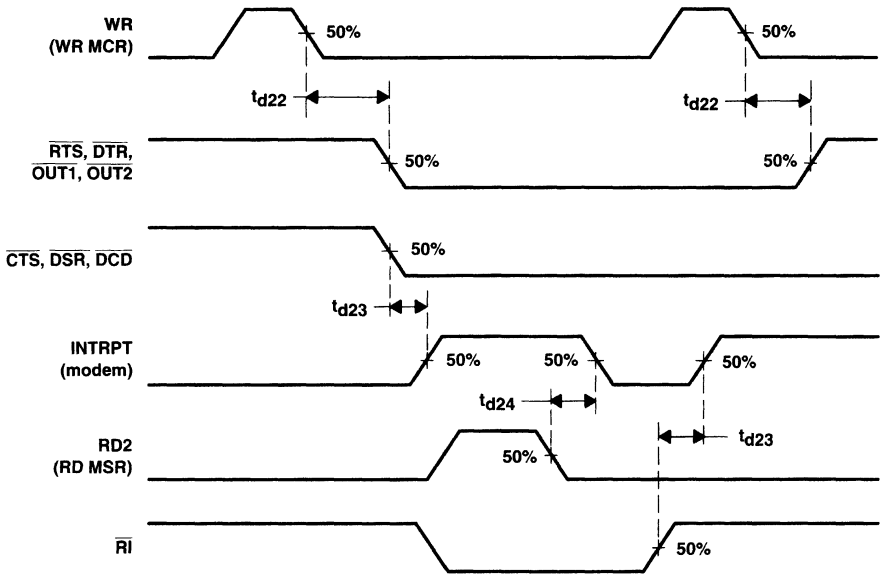


Figure 16. Modem Control Timing Waveforms

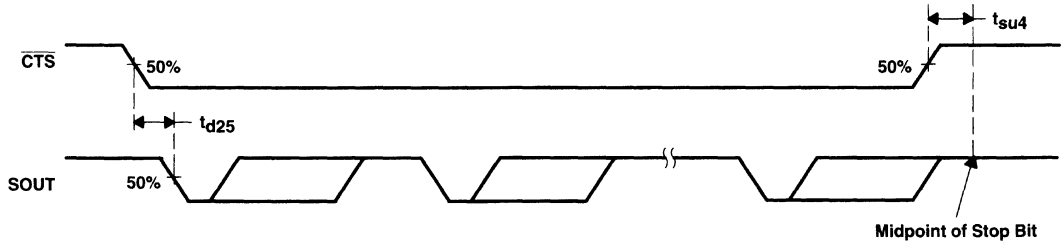


Figure 17. CTS and SOUT Autoflow Control Timing (Start and Stop) Waveforms

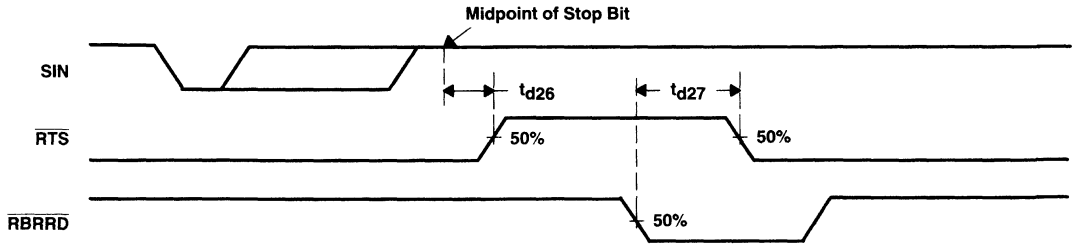


Figure 18. Auto-RTS Timing for RCV Threshold of 1, 4, or 8 Waveforms

PARAMETER MEASUREMENT INFORMATION

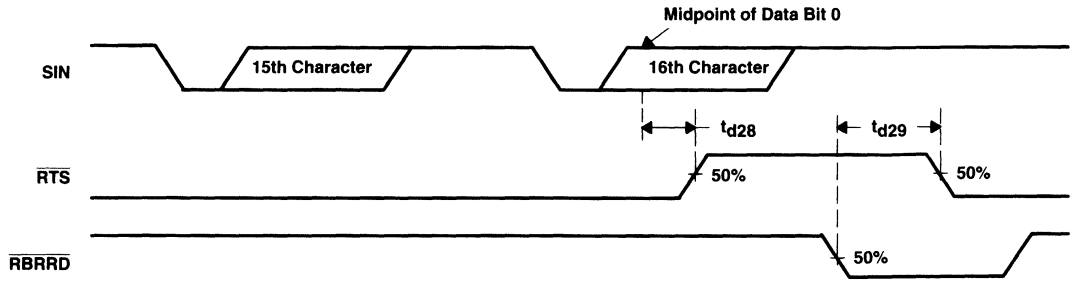


Figure 19. Auto-RTS Timing for RCV Threshold of 14 Waveforms

APPLICATION INFORMATION

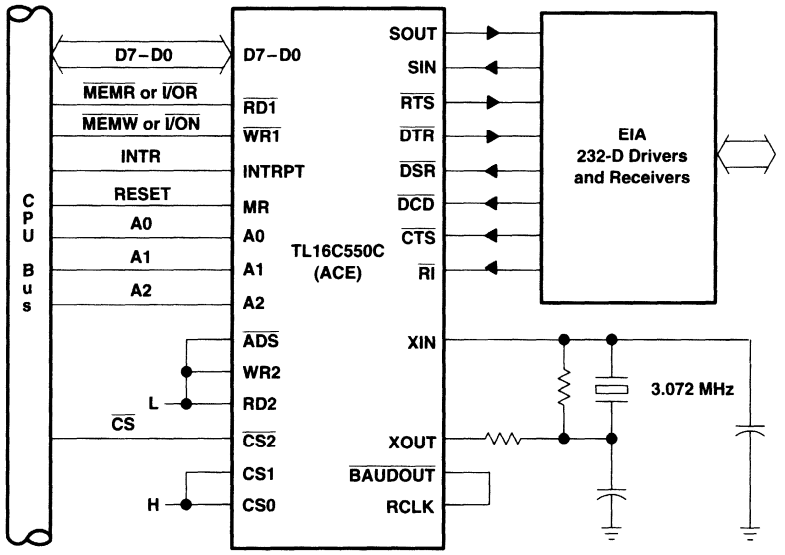


Figure 20. Basic TL16C550C Configuration

APPLICATION INFORMATION

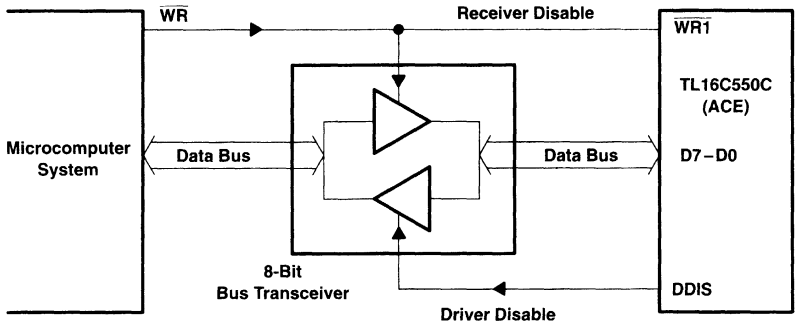
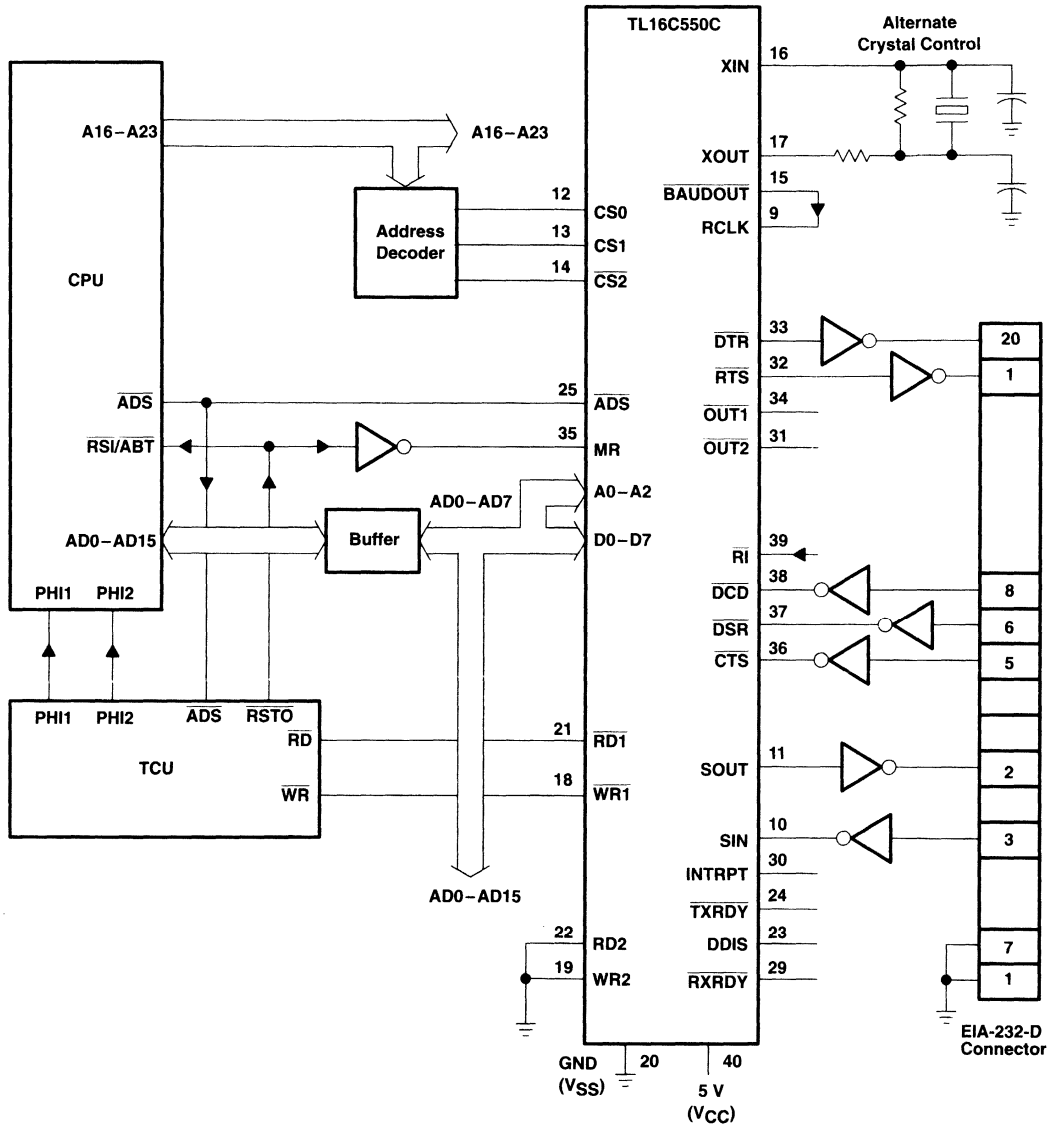


Figure 21. Typical Interface for a High Capacity Data Bus

APPLICATION INFORMATION



NOTE A: Terminal numbers shown are for the N package.

Figure 22. Typical TL16C550C Connection to a CPU

PRINCIPLES OF OPERATION

Table 1. Register Selection

DLAB†	A2	A1	A0	REGISTER
0	L	L	L	Receiver buffer (read), transmitter holding register (write)
0	L	L	H	Interrupt enable register
X	L	H	L	Interrupt identification register (read only)
X	L	H	L	FIFO control register (write)
X	L	H	H	Line control register
X	H	L	L	Modem control register
X	H	L	H	Line status register
X	H	H	L	Modem status register
X	H	H	H	Scratch register
1	L	L	L	Divisor latch (LSB)
1	L	L	H	Divisor latch (MSB)

† The divisor latch access bit (DLAB) is the most significant bit of the line control register. The DLAB signal is controlled by writing to this bit location (see Table 4).

Table 2. ACE Reset Functions

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	Master Reset	All bits cleared (0–3 forced and 4–7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is set, bits 1, 2, 3, 6, and 7 are cleared, and bits 4–5 are permanently cleared
FIFO Control Register	Master Reset	All bits cleared
Line Control Register	Master Reset	All bits cleared
Modem Control Register	Master Reset	All bits cleared (6–7 permanent)
Line Status Register	Master Reset	Bits 5 and 6 are set; all other bits are cleared
Modem Status Register	Master Reset	Bits 0–3 are cleared; bits 4–7 are input signals
SOUT	Master Reset	High
INTRPT (receiver error flag)	Read LSR/MR	Low
INTRPT (received data available)	Read RBR/MR	Low
INTRPT (transmitter holding register empty)	Read IR/Write THR/MR	Low
INTRPT (modem status changes)	Read MSR/MR	Low
$\overline{OUT2}$	Master Reset	High
$\overline{RTS}$	Master Reset	High
$\overline{DTR}$	Master Reset	High
$\overline{OUT1}$	Master Reset	High
Scratch Register	Master Reset	No effect
Divisor Latch (LSB and MSB) Registers	Master Reset	No effect
Receiver Buffer Register	Master Reset	No effect
Transmitter Holding Register	Master Reset	No effect
RCVR FIFO	MR/FCR1–FCR0/ΔFCR0	All bits cleared
XMIT FIFO	MR/FCR2–FCR0/ΔFCR0	All bits cleared

PRINCIPLES OF OPERATION

accessible registers

The system programmer, using the CPU, has access to and control over any of the ACE registers that are summarized in Table 2. These registers control ACE operations, receive data, and transmit data. Descriptions of these registers follow Table 3.

Table 3. Summary of Accessible Registers

BIT NO.	REGISTER ADDRESS											
	0 DLAB = 0	0 DLAB = 0	1 DLAB = 0	2	2	3	4	5	6	7	0 DLAB = 1	1 DLAB = 1
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident. Register (Read Only)	FIFO Control Register (Write Only)	Line Control Register	Modem Control Register	Line Status Register	Modem Status Register	Scratch Register	Divisor Latch (LSB)	Latch (MSB)
	RBR	THR	IER	IIR	FCR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Data Bit 0†	Data Bit 0	Enable Received Data Available Interrupt (ERBI)	0 if Interrupt Pending	FIFO Enable	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (ΔCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit 1	Receiver FIFO Reset	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (ΔDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit 2	Transmitter FIFO Reset	Number of Stop Bits (STB)	OUT1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable Modem Status Interrupt (EDSSI)	Interrupt ID Bit 3 (see Note 4)	DMA Mode Select	Parity Enable (PEN)	OUT2	Framing Error (FE)	Delta Data Carrier Detect (ΔDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity	Autoflow Control Enable (AFE)	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	FIFOs Enabled (see Note 4)	Receiver Trigger (LSB)	Break Control	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	FIFOs Enabled (see Note 4)	Receiver Trigger (MSB)	Divisor Latch Access Bit (DLAB)	0	Error in RCVR FIFO (see Note 4)	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

† Bit 0 is the least significant bit. It is the first bit serially transmitted or received.
NOTE 4: These bits are always 0 in the TL16C450 mode.

PRINCIPLES OF OPERATION

FIFO control register (FCR)

The FCR is a write-only register at the same location as the IIR, which is a read-only register. The FCR enables and clears the FIFOs, sets the receiver FIFO trigger level, and selects the type of DMA signalling.

- Bit 0: This bit, when set, enables the transmitter and receiver FIFOs. Bit 0 must be set when other FCR bits are written to or they are not programmed. Changing this bit clears the FIFOs.
- Bit 1: This bit, when set, clears all bytes in the receiver FIFO and clears its counter. The shift register is not cleared. The one that is written to this bit position is self clearing.
- Bit 2: This bit, when set, clears all bytes in the transmit FIFO and clears its counter. The shift register is not cleared. The one that is written to this bit position is self clearing.
- Bit 3: When FCR0 is set, setting FCR3 causes $\overline{\text{RXRDY}}$ and $\overline{\text{TXRDY}}$ to change from level 0 to level 1.
- Bits 4 and 5: These two bits are reserved for future use.
- Bits 6 and 7: These two bits set the trigger level for the receiver FIFO interrupt (see Table 5).

Table 4. Receiver FIFO Trigger Level

BIT 7	BIT 6	RECEIVER FIFO TRIGGER LEVEL (BYTES)
0	0	01
0	1	04
1	0	08
1	1	14

FIFO interrupt mode operation

When the receiver FIFO and receiver interrupts are enabled (FCR0 = 1, IER0 = 1, IER2 = 1), a receiver interrupt occurs as follows:

1. The received data available interrupt is issued to the microprocessor when the FIFO has reached its programmed trigger level. It is cleared when the FIFO drops below its programmed trigger level.
2. The IIR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt, it is cleared when the FIFO drops below the trigger level.
3. The receiver line status interrupt (IIR = 06) has higher priority than the received data available (IIR = 04) interrupt.
4. The data ready bit (LSR0) is set when a character is transferred from the shift register to the receiver FIFO. It is cleared when the FIFO is empty.

PRINCIPLES OF OPERATION

FIFO interrupt mode operation (continued)

When the receiver FIFO and receiver interrupts are enabled:

1. FIFO time-out interrupt occurs if the following conditions exist:
   a. At least one character is in the FIFO.
   b. The most recent serial character was received more than four continuous character times ago (if two stop bits are programmed, the second one is included in this time delay).
   c. The most recent microprocessor read of the FIFO occurred more than four continuous character times ago. This causes a maximum character received to interrupt an issued delay of 160 ms at 300 baud with a 12-bit character.
2. Character times are calculated by using the RCLK input for a clock signal (makes the delay proportional to the baud rate).
3. When a time-out interrupt has occurred, it is cleared and the timer is cleared when the microprocessor reads one character from the receiver FIFO.
4. When a time-out interrupt has not occurred, the time-out timer is cleared after a new character is received or after the microprocessor reads the receiver FIFO.

When the transmitter FIFO and THRE interrupt are enabled (FCR0 = 1, IER1 = 1), transmit interrupts occur as follows:

1. The transmitter holding register interrupt [IIR (3–0) = 2] occurs when the transmit FIFO is empty. It is cleared [IIR (3–0) = 1] when the THR is written to (1 to 16 characters may be written to the transmit FIFO while servicing this interrupt) or the IIR is read.
2. The transmitter FIFO empty indicator (LSR5 (THRE) = 1) is delayed one character time minus the last stop bit time when there have not been at least two bytes in the transmitter FIFO at the same time since the last time that THRE = 1. The first transmitter interrupt after changing FCR0 is immediate if it is enabled.

Character time-out and receiver FIFO trigger level interrupts have the same priority as the current received data available interrupt; transmit FIFO empty has the same priority as the current THRE interrupt.

FIFO polled mode operation

With FCR0 = 1 (transmitter and receiver FIFOs enabled), clearing IER0, IER1, IER2, IER3, or all four to 0 puts the ACE in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately, either one or both can be in the polled mode of operation.

In this mode, the user program checks receiver and transmitter status using the LSR. As stated previously:

- LSR0 is set as long as there is one byte in the receiver FIFO.
- LSR1 – LSR4 specify which error(s) have occurred. Character error status is handled the same way as when in the interrupt mode; the IIR is not affected since IER2 = 0.
- LSR5 indicates when the THR is empty.
- LSR6 indicates that both the THR and TSR are empty.
- LSR7 indicates whether there are any errors in the receiver FIFO.

There is no trigger level reached or time-out condition indicated in the FIFO polled mode. However, the receiver and transmitter FIFOs are still fully capable of holding characters.

PRINCIPLES OF OPERATION

interrupt enable register (IER)

The IER enables each of the five types of interrupts (refer to Table 4) and enables INTRPT in response to an interrupt generation. The IER can also disable the interrupt system by clearing bits 0 through 3. The contents of this register are summarized in Table 3 and are described in the following bullets.

- Bit 0: When set, this bit enables the received data available interrupt.
- Bit 1: When set, this bit enables the THRE interrupt.
- Bit 2: When set, this bit enables the receiver line status interrupt.
- Bit 3: When set, this bit enables the modem status interrupt.
- Bits 4 through 7: These bits are not used (always cleared).

interrupt identification register (IIR)

The ACE has an on-chip interrupt generation and prioritization capability that permits a flexible interface with most popular microprocessors.

The ACE provides four prioritized levels of interrupts:

- Priority 1 – Receiver line status (highest priority)
- Priority 2 – Receiver data ready or receiver character time-out
- Priority 3 – Transmitter holding register empty
- Priority 4 – Modem status (lowest priority)

When an interrupt is generated, the IIR indicates that an interrupt is pending and encodes the type of interrupt in its three least significant bits (bits 0, 1, and 2). The contents of this register are summarized in Table 2 and described in Table 4. Detail on each bit is as follows:

- Bit 0: This bit is used either in a hardwire prioritized or polled interrupt system. When bit 0 is cleared, an interrupt is pending If bit 0 is set, no interrupt is pending.
- Bits 1 and 2: These two bits identify the highest priority interrupt pending as indicated in Table 3
- Bit 3: This bit is always cleared in TL16C450 mode. In FIFO mode, bit 3 is set with bit 2 to indicate that a time-out interrupt is pending.
- Bits 4 and 5: These two bits are not used (always cleared).
- Bits 6 and 7: These bits are always cleared in TL16C450 mode. They are set when bit 0 of the FIFO control register is set.

PRINCIPLES OF OPERATION

interrupt identification register (IIR) (continued)

Table 5. Interrupt Control Functions

INTERRUPT IDENTIFICATION REGISTER				PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET METHOD
BIT 3	BIT 2	BIT 1	BIT 0				
0	0	0	1	None	None	None	None
0	1	1	0	1	Receiver line status	Overrun error, parity error, framing error, or break interrupt	Read the line status register
0	1	0	0	2	Received data available	Receiver data available in the TL16C450 mode or trigger level reached in the FIFO mode	Read the receiver buffer register
1	1	0	0	2	Character time-out indication	No characters have been removed from or input to the receiver FIFO during the last four character times, and there is at least one character in it during this time	Read the receiver buffer register
0	0	1	0	3	Transmitter holding register empty	Transmitter holding register empty	Read the interrupt identification register (if source of interrupt) or writing into the transmitter holding register
0	0	0	0	4	Modem status	Clear to send, data set ready, ring indicator, or data carrier detect	Read the modem status register

line control register (LCR)

The system programmer controls the format of the asynchronous data communication exchange through the LCR. In addition, the programmer is able to retrieve, inspect, and modify the contents of the LCR; this eliminates the need for separate storage of the line characteristics in system memory. The contents of this register are summarized in Table 3 and described in the following bulleted list.

- Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. These bits are encoded as shown in Table 6.

Table 6. Serial Character Word Length

BIT 1	BIT 0	WORD LENGTH
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

- Bit 2: This bit specifies either one, one and one-half, or two stop bits in each transmitted character. When bit 2 is cleared, one stop bit is generated in the data. When bit 2 is set, the number of stop bits generated is dependent on the word length selected with bits 0 and 1. The receiver clocks only the first stop bit regardless of the number of stop bits selected. The number of stop bits generated in relation to word length and bit 2 are shown in Table 7.

PRINCIPLES OF OPERATION

line control register (LCR) (continued)

Table 7. Number of Stop Bits Generated

BIT 2	WORD LENGTH SELECTED BY BITS 1 AND 2	NUMBER OF STOP BITS GENERATED
0	Any word length	1
1	5 bits	1 1/2
1	6 bits	2
1	7 bits	2
1	8 bits	2

- Bit 3: This bit is the parity enable bit. When bit 3 is set, a parity bit is generated in transmitted data between the last data word bit and the first stop bit. In received data, if bit 3 is set, parity is checked. When bit 3 is cleared, no parity is generated or checked.
- Bit 4: This bit is the even parity select bit. When parity is enabled (bit 3 is set) and bit 4 is set even parity (an even number of logic 1s in the data and parity bits) is selected. When parity is enabled and bit 4 is cleared, odd parity (an odd number of logic 1s) is selected.
- Bit 5: This bit is the stick parity bit. When bits 3, 4, and 5 are set, the parity bit is transmitted and checked as cleared. When bits 3 and 5 are set and bit 4 is cleared, the parity bit is transmitted and checked as set. If bit 5 is cleared, stick parity is disabled.
- Bit 6: This bit is the break control bit. Bit 6 is set to force a break condition; i.e., a condition where SOUT is forced to the spacing (cleared) state. When bit 6 is cleared, the break condition is disabled and has no affect on the transmitter logic; it only effects SOUT.
- Bit 7: This bit is the divisor latch access bit (DLAB). Bit 7 must be set to access the divisor latches of the baud generator during a read or write. Bit 7 must be cleared during a read or write to access the receiver buffer, the THR, or the IER.

line status register (LSR)†

The LSR provides information to the CPU concerning the status of data transfers. The contents of this register are summarized in Table 3 and described in the following bulleted list.

- Bit 0: This bit is the data ready (DR) indicator for the receiver. DR is set whenever a complete incoming character has been received and transferred into the RBR or the FIFO. DR is cleared by reading all of the data in the RBR or the FIFO.
- Bit 1‡: This bit is the overrun error (OE) indicator. When OE is set, it indicates that before the character in the RBR was read, it was overwritten by the next character transferred into the register. OE is cleared every time the CPU reads the contents of the LSR. If the FIFO mode data continues to fill the FIFO beyond the trigger level, an overrun error occurs only after the FIFO is full and the next character has been completely received in the shift register. An overrun error is indicated to the CPU as soon as it happens. The character in the shift register is overwritten, but it is not transferred to the FIFO.

† The line status register is intended for read operations only; writing to this register is not recommended outside of a factory testing environment.
‡ Bits 1 through 4 are the error conditions that produce a receiver line status interrupt.

PRINCIPLES OF OPERATION

line status register (LSR) (continued)†

- Bit 2‡: This bit is the parity error (PE) indicator. When PE is set, it indicates that the parity of the received data character does not match the parity selected in the LCR (bit 4). PE is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO.
- Bit 3‡: This bit is the framing error (FE) indicator. When FE is set, it indicates that the received character did not have a valid (set) stop bit. FE is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. The ACE tries to resynchronize after a framing error. To accomplish this, it is assumed that the framing error is due to the next start bit. The ACE samples this start bit twice and then accepts the input data.
- Bit 4‡: This bit is the break interrupt (BI) indicator. When BI is set, it indicates that the received data input was held low for longer than a full-word transmission time. A full-word transmission time is defined as the total time to transmit the start, data, parity, and stop bits. BI is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. When a break occurs, only one 0 character is loaded into the FIFO. The next character transfer is enabled after SIN goes to the marking state for at least two RCLK samples and then receives the next valid start bit.
- Bit 5: This bit is the THRE indicator. THRE is set when the THR is empty, indicating that the ACE is ready to accept a new character. If the THRE interrupt is enabled when THRE is set, an interrupt is generated. THRE is set when the contents of the THR are transferred to the TSR. THRE is cleared concurrent with the loading of the THR by the CPU. In the FIFO mode, THRE is set when the transmit FIFO is empty; it is cleared when at least one byte is written to the transmit FIFO.
- Bit 6: This bit is the transmitter empty (TEMT) indicator. TEMT bit is set when the THR and the TSR are both empty. When either the THR or the TSR contains a data character, TEMT is cleared. In the FIFO mode, TEMT is set when the transmitter FIFO and shift register are both empty.
- Bit 7: In the TL16C550C mode, this bit is always cleared. In the TL16C450 mode, this bit is always cleared. In the FIFO mode, LSR7 is set when there is at least one parity, framing, or break error in the FIFO. It is cleared when the microprocessor reads the LSR and there are no subsequent errors in the FIFO.

modem control register (MCR)

The MCR is an 8-bit register that controls an interface with a modem, data set, or peripheral device that is emulating a modem. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bit 0: This bit (DTR) controls the $\overline{\text{DTR}}$ output.
- Bit 1: This bit (RTS) controls the $\overline{\text{RTS}}$ output.
- Bit 2: This bit (OUT1) controls $\overline{\text{OUT1}}$, a user-designated output signal.
- Bit 3: This bit (OUT2) controls $\overline{\text{OUT2}}$, a user-designated output signal.

When any of bits 0 through 3 are set, the associated output is forced low. When any of these bits are cleared, the associated output is forced high.

† The line status register is intended for read operations only; writing to this register is not recommended outside of a factory testing environment.
‡ Bits 1 through 4 are the error conditions that produce a receiver line status interrupt.

PRINCIPLES OF OPERATION

modem control register (MCR) (continued)

- Bit 4: This bit (LOOP) provides a local loop back feature for diagnostic testing of the ACE. When LOOP is set, the following occurs:
  - The transmitter SOUT is set high.
  - The receiver SIN is disconnected.
  - The output of the TSR is looped back into the receiver shift register input.
  - The four modem control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$) are disconnected.
  - The four modem control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT1}$, and $\overline{OUT2}$) are internally connected to the four modem control inputs.
  - The four modem control outputs are forced to the inactive (high) levels.
- Bit 5: This bit (AFE) is the autoflow control enable. When set, the autoflow control as described in the detailed description is enabled.

  In the diagnostic mode, data that is transmitted is immediately received. This allows the processor to verify the transmit and receive data paths to the ACE. The receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational, but the modem control interrupt's sources are now the lower four bits of the MCR instead of the four modem control inputs. All interrupts are still controlled by the IER.

  The ACE flow can be configured by programming bits 1 and 5 of the MCR as shown in Table 8.

Table 8. ACE Flow Configuration

MCR BIT 5 (AFE)	MCR BIT 1 (RTS)	ACE FLOW CONFIGURATION
1	1	Auto-$\overline{RTS}$ and auto-$\overline{CTS}$ enabled (autoflow control enabled)
1	0	Auto-$\overline{CTS}$ only enabled
0	X	Auto-$\overline{RTS}$ and auto-$\overline{CTS}$ disabled

modem status register (MSR)

The MSR is an 8-bit register that provides information about the current state of the control lines from the modem, data set, or peripheral device to the CPU. Additionally, four bits of this register provide change information; when a control input from the modem changes state, the appropriate bit is set. All four bits are cleared when the CPU reads the MSR. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bit 0: This bit is the change in clear-to-send (ΔCTS) indicator. ΔCTS indicates that the $\overline{CTS}$ input has changed state since the last time it was read by the CPU. When ΔCTS is set (autoflow control is not enabled and the modem status interrupt is enabled), a modem status interrupt is generated. When autoflow control is enabled (ΔCTS is cleared), no interrupt is generated.
- Bit 1: This bit is the change in data set ready (ΔDSR) indicator. ΔDSR indicates that the $\overline{DSR}$ input has changed state since the last time it was read by the CPU. When ΔDSR is set and the modem status interrupt is enabled, a modem status interrupt is generated.
- Bit 2: This bit is the trailing edge of the ring indicator (TERI) detector. TERI indicates that the $\overline{RI}$ input to the chip has changed from a low to a high level. When TERI is set and the modem status interrupt is enabled, a modem status interrupt is generated.

PRINCIPLES OF OPERATION

modem status register (MSR) (continued)

- Bit 3: This bit is the change in data carrier detect (ΔDCD) indicator. ΔDCD indicates that the $\overline{DCD}$ input to the chip has changed state since the last time it was read by the CPU. When ΔDCD is set and the modem status interrupt is enabled, a modem status interrupt is generated.
- Bit 4: This bit is the complement of the clear-to-send ($\overline{CTS}$) input. When the ACE is in the diagnostic test mode (LOOP [MCR4] = 1), this bit is equal to the MCR bit 1 (RTS).
- Bit 5: This bit is the complement of the data set ready ($\overline{DSR}$) input. When the ACE is in the diagnostic test mode (LOOP [MCR4] = 1), this bit is equal to the MCR bit 0 (DTR).
- Bit 6: This bit is the complement of the ring indicator ($\overline{RI}$) input. When the ACE is in the diagnostic test mode (LOOP [MCR4] = 1), this bit is equal to the MCR bit 2 (OUT1).
- Bit 7: This bit is the complement of the data carrier detect ($\overline{DCD}$) input. When the ACE is in the diagnostic test mode (LOOP [MCR4] = 1), this bit is equal to the MCR bit 3 (OUT2).

programmable baud generator

The ACE contains a programmable baud generator that takes a clock input in the range between dc and 16 MHz and divides it by a divisor in the range between 1 and (2^{16}–1). The output frequency of the baud generator is sixteen times (16×) the baud rate. The formula for the divisor is:

divisor = XIN frequency input ÷ (desired baud rate × 16)

Two 8-bit registers, called divisor latches, store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization of the ACE in order to ensure desired operation of the baud generator. When either of the divisor latches is loaded, a 16-bit baud counter is also loaded to prevent long counts on initial load.

Tables 9 and 10 illustrate the use of the baud generator with crystal frequencies of 1.8432 MHz and 3.072 MHz respectively. For baud rates of 38.4 kbits/s and below, the error obtained is very small. The accuracy of the selected baud rate is dependent on the selected crystal frequency (refer to Figure 23 for examples of typical clock circuits).

PRINCIPLES OF OPERATION

programmable baud generator (continued)

Table 9. Baud Rates Using a 1.8432-MHz Crystal

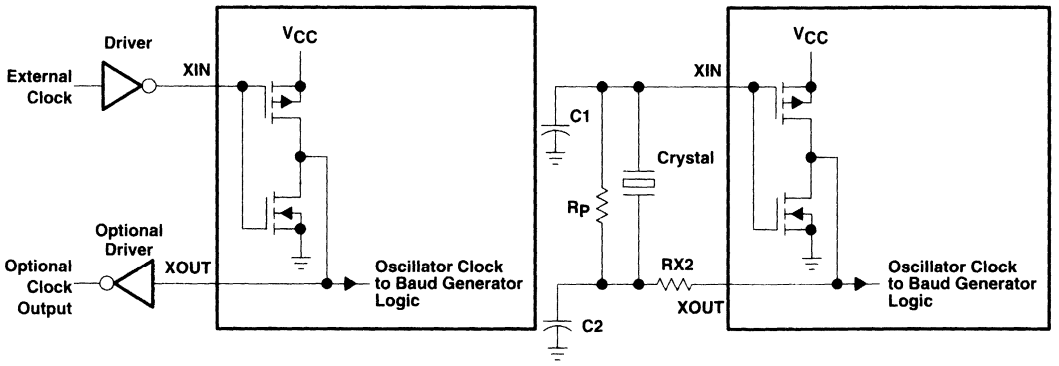
DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 × CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
1800	64	
2000	58	0.69
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19200	6	
38400	3	
56000	2	2.86

Table 10. Baud Rates Using a 3.072-MHz Crystal

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 × CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	
75	2560	
110	1745	0.026
134.5	1428	0.034
150	1280	
300	640	
600	320	
1200	160	
1800	107	0.312
2000	96	
2400	80	
3600	53	0.628
4800	40	
7200	27	1.23
9600	20	
19200	10	
38400	5	

PRINCIPLES OF OPERATION

programmable baud generator (continued)



TYPICAL CRYSTAL OSCILLATOR NETWORK

CRYSTAL	Rp	RX2	C1	C2
3.072 MHz	1 MΩ	1.5 kΩ	10–30 pF	40–60 pF
1.8432 MHz	1 MΩ	1.5 kΩ	10–30 pF	40–60 pF

Figure 23. Typical Clock Circuits

receiver buffer register (RBR)

The ACE receiver section consists of a receiver shift register (RSR) and a RBR. The RBR is actually a 16-byte FIFO. Timing is supplied by the 16× receiver clock (RCLK). Receiver section control is a function of the ACE line control register.

The ACE RSR receives serial data from SIN. The RSR then concatenates the data and moves it into the RBR FIFO. In the TL16C450 mode, when a character is placed in the RBR and the received data available interrupt is enabled (IER0 = 1), an interrupt is generated. This interrupt is cleared when the data is read out of the RBR. In the FIFO mode, the interrupts are generated based on the control setup in the FIFO control register.

scratch register

The scratch register is an 8-bit register that is intended for the programmer's use as a scratchpad in the sense that it temporarily holds the programmer's data without affecting any other ACE operation.

transmitter holding register (THR)

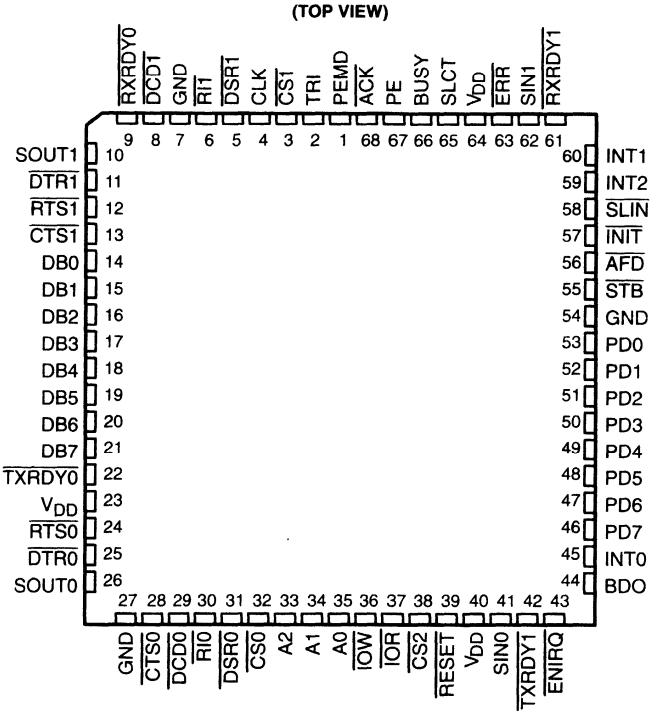
The ACE transmitter section consists of a THR and a transmitter shift register (TSR). The THR is actually a 16-byte FIFO. Timing is supplied by $\overline{\text{BAUDOUT}}$. Transmitter section control is a function of the ACE line control register.

The ACE THR receives data off the internal data bus and when the shift register is idle, moves it into the TSR. The TSR serializes the data and outputs it at SOUT. In the TL16C450 mode, if the THR is empty and the transmitter holding register empty (THRE) interrupt is enabled (IER1 = 1), an interrupt is generated. This interrupt is cleared when a character is loaded into the register. In the FIFO mode, the interrupts are generated based on the control setup in the FIFO control register.

- **IBM PC/AT™ Compatible**
- **Two TL16C550 ACEs**
- **Enhanced Bidirectional Printer Port**
- **16-Byte FIFOs Reduce CPU Interrupts**
- **Independent Control of Transmit, Receive, Line Status, and Data Set Interrupts on Each Channel**
- **Individual Modem Control Signals for Each Channel**
- **Programmable Serial Interface Characteristics for Each Channel:**
  - **5-, 6-, 7-, or 8-bit Characters**
  - **Even-, Odd-, or No-Parity Bit Generation and Detection**
  - **1-, 1 1/2-, or 2-Stop Bit Generation**
- **3-State TTL Drive for the Data and Control Bus on Each Channel**
- **Hardware and Software Compatible With TL16C452**

description

FN PACKAGE
(TOP VIEW)



description

The TL16C552 is an enhanced dual channel version of the popular TL16C550 asynchronous communications element (ACE). The device serves two serial input/output interfaces simultaneously in microcomputer or microprocessor-based systems. Each channel performs serial-to-parallel conversion on data characters

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description (continued)

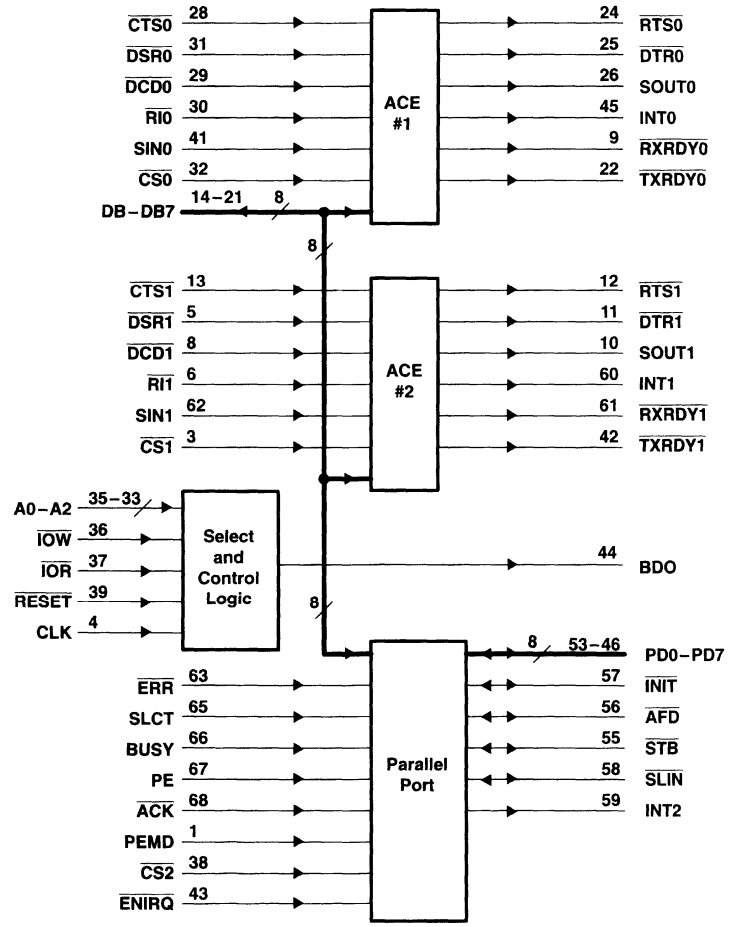
received from peripheral devices or modems and parallel-to-serial conversion on data characters transmitted by the CPU. The complete status of each channel of the dual ACE can be read at any time during functional operation by the CPU. The information obtained includes the type and condition of the transfer operations being performed and the error conditions.

In addition to its dual communications interface capabilities, the TL16C552 provides the user with a fully bidirectional parallel data port that fully supports the parallel Centronics-type printer. The parallel port and the two serial ports provide IBM PC/AT-compatible computers with a single device to serve the three system ports.

A programmable baud rate generator is included that can divide the timing reference clock input by a divisor between 1 and ($2^{16} - 1$).

The TL16C552 is housed in a 68-pin plastic leaded chip carrier.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{ACK}$	68	I	Line printer acknowledge. $\overline{ACK}$ goes low to indicate a successful data transfer has taken place. It generates a printer port interrupt during its positive transition.
$\overline{AFD}$	56	I/O	Line printer autofeed. $\overline{AFD}$ is an open-drain line that provides the printer with an active-low signal when continuous form paper is to be autofed to the printer. This terminal has an internal pullup resistor to V_{DD} of approximately 10 kΩ.
A0, A1, A2	35, 34, 33	I	Address lines A0–A2. A0, A1, and A2 select the internal registers during CPU bus operations. See Table 2 for the decode of the serial channels and Table 13 for the decode of the parallel printer port.
BDO	44	O	Bus buffer output. BDO is an active-high output that is asserted when either serial channel or the parallel port is read. This output can control the system bus driver (74LS245).
BUSY	66	I	Line printer busy. BUSY is an input line from the printer that goes high when the printer is not ready to accept data.
CLK	4	I	Clock input. CLK is an external clock input to the baud rate divisor of each ACE.
$\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$	32, 3, 38	I	Chip selects. $\overline{CS0}$, $\overline{CS1}$, and $\overline{CS2}$ act as an enable for the write and read signals for the serial channels 1 ($\overline{CS0}$) and 2 ($\overline{CS1}$). $\overline{CS2}$ enables the signals to the printer port.
$\overline{CTS0}$, $\overline{CTS1}$	28, 13	I	Clear to send inputs. The logical state of $\overline{CTS0}$ or $\overline{CTS1}$ is reflected in the CTS bit of the modem status register (CTS is bit 4 of the modem status register, written MSR4) of each ACE. A change of state in either $\overline{CTS}$ terminal, since the previous reading of the associated modem status register, causes the setting of delta clear to send (ΔCTS) bit (MSR0) of each modem status register.
DB0 – DB7	14 – 21	I/O	Data bits DB0 – DB7. The data bus provides eight 3-state I/O lines for the transfer of data, control, and status information between the TL16C552 and the CPU. These lines are normally in a high-impedance state except during read operations. D0 is the least significant bit (LSB) and is the first serial data bit to be received or transmitted.
$\overline{DCD0}$, $\overline{DCD1}$	29, 8	I	Data carrier detect. $\overline{DCD}$ is a modem input. Its condition can be tested by the CPU by reading the MSR7 (DCD) bit of the modem status registers. The MSR3 (delta data carrier detect or ΔDCD) bit of the modem status register indicates whether the $\overline{DCD}$ input has changed states since the previous reading of the modem status register. $\overline{DCD}$ has no affect on the receiver.
$\overline{DSR0}$, $\overline{DSR1}$	31, 5	I	Data set ready inputs. The logical state of $\overline{DSR0}$ and $\overline{DSR1}$ is reflected in MSR5 of its associated modem status register. The MSR1 (delta data set ready or ΔDSR) bit indicates whether the associated DSR terminal has changed states since the previous reading of the modem status register.
$\overline{DTR0}$, $\overline{DTR1}$	25, 11	O	Data terminal ready lines. $\overline{DTR0}$ and $\overline{DTR1}$ can be asserted low by setting modem control register bit 0 (MCR0) of its associated ACE. This signal is asserted high by clearing the DTR bit (MCR0) or whenever a reset occurs. When active (low), the DTR terminal indicates that its ACE is ready to receive data.
$\overline{ENIRQ}$	43	I	Parallel port interrupt source mode selection. When $\overline{ENIRQ}$ is low, the PC/AT mode of interrupts is enabled. In this mode, the INT2 output is internally connected to the $\overline{ACK}$ input. When the $\overline{ENIRQ}$ input is tied high, the INT2 output is internally tied to the $\overline{PRINT}$ signal in the line printer status register. INT2 is latched high on rising edge of $\overline{ACK}$.
$\overline{ERR}$	63	I	Line printer error. $\overline{ERR}$ is an input line from the printer. The printer reports an error by holding this line low during the error condition.
GND	7, 27, 54		Ground (0 V). All terminals must be tied to ground for proper operation.
$\overline{INIT}$	57	I/O	Line printer initialize. $\overline{INIT}$ is an open-drain line that provides the printer with an active-low signal, which allows the printer initialization routine to be started. This terminal has an internal pullup resistor to V_{DD} of approximately 10 kΩ.
$\overline{IOR}$	37	I	Input/output read strobe. $\overline{IOR}$ is an active-low input that enables the selected channel to output data to the data bus (DB0–DB7). The data output depends upon the register selected by the address inputs A0, A1, A2, and chip select. Chip select 0 ($\overline{CS0}$) selects ACE #1, chip select 1 ($\overline{CS1}$) selects ACE #2, and chip select 2 ($\overline{CS2}$) selects the printer port.
$\overline{IOW}$	36	I	Input/output write strobe. $\overline{IOW}$ is an active-low input causing data from the data bus to be input to either ACE or to the parallel port. The destination depends upon the register selected by the address inputs A0, A1, A2, and chip selects $\overline{CS0}$, $\overline{CS1}$, and $\overline{CS2}$.

Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
INT0, INT1	45, 60	O	Serial channel interrupts. INT0 and INT1 are 3-state serial channel interrupt outputs (enabled by bit 3 of the MCR) that go active (high) when one of the following interrupts has an active (high) condition and is enabled by the interrupt enable register of its associated channel: receiver error flag, received data available, transmitter holding register empty, and modem status. The interrupt is cleared upon appropriate service. When reset, the interrupt output is in the high-impedance state.
INT2	59	O	Printer port interrupt. INT2 is an active-high, 3-state output generated by the positive transition of $\overline{ACK}$. It is enabled by bit 4 of the write control register. Upon a reset, the interrupt output is in the high-impedance state. Its mode is also controlled by $\overline{ENIRQ}$.
PD0–PD7	53–46	I/O	Parallel data bits (0–7). These eight lines (PD0–PD7) provide a byte wide input or output port to the system.
PE	67	I	Printer paper empty. PE is an input line from the printer that goes high when the printer runs out of paper.
PEMD	1	I	Printer enhancement mode. When low, PEMD enables the write data register to the PD0–PD7 lines. A high on this signal allows direction control of the PD0–PD7 port by the DIR bit in the control register. PEMD is usually tied low for the printer operation.
$\overline{RESET}$	39	I	Reset. When low, $\overline{RESET}$ forces the TL16C552 into an idle mode in which all serial data activities are suspended. The modem control register along with its associated outputs are cleared. The line status register is cleared except for the THRE and TEMT bits, which are set. All functions of the device remain in an idle state until programmed to resume serial data activities. This input has a hysteresis level of typically 400 mV.
$\overline{RTS0}$, $\overline{RTS1}$	24, 12	O	Request to send outputs. $\overline{RTSx}$ is asserted low by setting MCR1, bit 1 of its UARTs modem control register. Both $\overline{RTSx}$ terminals are set by $\overline{RESET}$. A low on the $\overline{RTSx}$ terminal indicates that its ACE has data ready to transmit. In half-duplex operations, $\overline{RTSx}$ controls the direction of the line.
$\overline{RXRDY0}$, $\overline{RXRDY1}$	9, 61	O	Receiver ready. $\overline{RXRDY0}$ and $\overline{RXRDY1}$ are receiver direct memory access (DMA) signaling terminals. One of two types of DMA signaling can be selected using FIFO control register bit 3 (FCR3) when operating in the FIFO mode. Only DMA mode 0 is allowed when operating in the TL16C450 mode. For signal transfer DMA (a transfer is made between CPU bus cycles), mode 0 is used. Multiple transfers that are made continuously until the receiver FIFO has been emptied are supported by mode 1. Mode 0. $\overline{RXRDYx}$ is active (low) when in the FIFO mode (FCR0=1, FCR3=0) or when in the TL16C450 mode (FCR0=0) and the receiver FIFO or receiver holding register contain at least one character. When there are no more characters in the receiver FIFO or receiver holding register, the $\overline{RXRDYx}$ terminal goes inactive (high). Mode 1. $\overline{RXRDYx}$ goes active (low) in the FIFO mode (FCR0=1) when FCR3=1 and the time-out or trigger levels have been reached. It goes inactive (high) when the FIFO or receiver holding register is empty.
$\overline{RI0}$, $\overline{RI1}$	30, 6	I	Ring indicator inputs. $\overline{RI0}$ and $\overline{RI1}$ are modem control inputs. Their condition is tested by reading MSR6 (RI) of each ACE. The modem status register outputs trailing edge of ring indicator (TERI or MSR2) that indicates whether either input has changed states from high to low since the previous reading of the modem status register.
SIN0, SIN1	41, 62	I	Serial data inputs. SIN0 and SIN1 are serial data inputs that move information from the communication line or modem to the TL16C552 receiver circuits. Mark (set) is a high state and a space (cleared) is low state. Data on the serial data inputs is disabled when operating in the loop mode.
SLCT	65	I	Printer selected. SLCT is an input line from the printer that goes high when the printer has been selected.
$\overline{SLIN}$	58	I/O	Line printer select. $\overline{SLIN}$ is an open-drain input that selects the printer when it is active (low). This terminal has an internal pullup resistor to V_{DD} of approximately 10 kΩ.
SOUT0, SOUT1	26, 10	O	Serial data outputs. SOUT0 and SOUT1 are the serial data outputs from the ACE transmitter circuitry. A mark is a high state and a space is a low state. Each SOUT is held in the mark condition when the transmitter is disabled, when $\overline{RESET}$ is true (low), when the transmitter register is empty, or when in the loop mode.

Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{STB}$	55	I/O	Printer strobe. $\overline{STB}$ is an open-drain line that provides communication between the TL16C552 and the printer. When it is active (low), it provides the printer with a signal to latch the data currently on the parallel port. This terminal has an internal pullup resistor to V_{DD} of approximately 10 kΩ.
TRI	2	I	3-state control. TRI controls the 3-state control of all I/O and output terminals. When TRI is asserted, all I/O and outputs become high impedance, allowing board level testers to drive the outputs without overdriving the internal buffers. This terminal is level sensitive, is a CMOS input, and is pulled down with an internal resistor that is approximately 5 kΩ.
$\overline{TXRDY0}$, $\overline{TXRDY1}$	22, 42	O	Transmitter ready. $\overline{TXRDY0}$ and $\overline{TXRDY1}$ are transmitter ready signals. Two types of DMA signaling are available. Either can be selected using FCR3 when operating in the FIFO mode. Only DMA mode 0 is allowed when operating in the TL16C450 mode. Single-transfer DMA (a transfer is made between CPU bus cycles) is supported by mode 0. Multiple transfers that are made continuously until the transmitter FIFO has been filled are supported by mode 1. Mode 0. When in the FIFO mode (FCR0=1, FCR3=0) or in the TL16C450 mode (FCR0=0) and there are no characters in the transmitter holding register or transmitter FIFO, $\overline{TXRDY}$ are active (low). Once $\overline{TXRDY}$ is activated (low), it goes inactive after the first character is loaded into the holding register of transmitter FIFO. Mode 1. $\overline{TXRDYx}$ goes active (low) if in the FIFO mode (FCR0=1) when FCR3=1 and there are no characters in the transmitter FIFO. When the transmitter FIFO is completely full, $\overline{TXRDYx}$ goes inactive (high).
V_{DD}	23, 40, 64		Power supply. V_{DD} is the power supply requirement is 5 V ±5%.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 1) ..... −0.5 V to V_{DD} + 0.3 V
Input voltage range, V_I ..... −0.5 V to 7 V
Output voltage range, V_O ..... −0.5 V to V_{DD} + 0.3 V
Continuous total power dissipation ..... 500 mW
Operating free-air temperature range, T_A ..... −10°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage levels are with respect to ground (V_{SS}).

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.75	5	5.25	V
Clock high-level input voltage, $V_{IH(CLK)}$	2		V_{DD}	V
Clock low-level input voltage, $V_{IL(CLK)}$	−0.5		0.8	V
High-level input voltage, V_{IH}	2		V_{DD}	V
Low-level input voltage, V_{IL}	−0.5		0.8	V
Clock frequency, f_{clock}			8	MHz
Operating free-air temperature range, T_A	0		70	°C

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −0.4 mA for DB0–DB7, I_{OH} = −2 mA for PD0–PD7, I_{OH} = −0.4 mA for $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$, and $\overline{SLIN}$ (see Note 2), I_{OH} = −0.4 mA for all other outputs	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA for DB0–DB7, I_{OL} = 12 mA for PD0–PD7, I_{OL} = 10 mA for $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$, and $\overline{SLIN}$ (see Note 2), I_{OL} = 2 mA for all other outputs		0.4	V
I_I	Input current	V_{DD} = 5.25 V, All other terminals are floating		±10	μA
$I_{I(CLK)}$	Clock input current	V_I = 0 to 5.25 V		±10	μA
I_{OZ}	High-impedance output current	V_{DD} = 5.25 V, V_O = 0 with chip deselected, or V_O = 5.25 V with chip and write mode selected		±20	μA
I_{DD}	Supply current	V_{DD} = 5.25 V, No loads on outputs, SIN0, SIN1, $\overline{DSR0}$, $\overline{DSR1}$, $\overline{DCD0}$, $\overline{DCD1}$, $\overline{CTS0}$, $\overline{CTS1}$, $\overline{RI0}$ and $\overline{RI1}$ at 2 V, Other inputs at 0.8 V, Baud rate generator f_{clock} = 8 MHz, Baud rate = 56 kbit/s		50	mA

NOTE 2: These four terminals contain an internal pullup resistor to V_{DD} of approximately 10 kΩ.

clock timing requirements over recommended ranges of operating free-air temperature and supply voltage

		MIN	MAX	UNIT
t_{w1}	Pulse duration, CLK high (external clock, 8 MHz max) (see Figure 1)	55		ns
t_{w2}	Pulse duration, CLK low (external clock, 8 MHz max) (see Figure 1)	55		ns
t_{w3}	Pulse duration, master ($\overline{RESET}$) low (see Figure 16)	1000		ns

read cycle timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 4)

		MIN	MAX	UNIT
t_{w4}	Pulse duration, $\overline{IOR}$ low	80		ns
t_{su1}	Setup time, chip select valid before $\overline{IOR}$ low (see Note 3)	15		ns
t_{su2}	Setup time, A2–A0 valid before $\overline{IOR}$ low (see Note 3)	15		ns
t_{h1}	Hold time, A2–A0 valid after $\overline{IOR}$ high (see Note 3)	20		ns
t_{h2}	Hold time, chip select valid after $\overline{IOR}$ high (see Note 3)	20		ns
t_{d1}	Delay time, $t_{su2} + t_{w4} + t_{d2}$ (see Note 4)	175		ns
t_{d2}	Delay time, $\overline{IOR}$ high to $\overline{IOR}$ or $\overline{IOW}$ low	80		ns

NOTES: 3. The internal address strobe is always active.
4. In the FIFO mode, t_{d1} = 425 ns (min) between reads of the receiver FIFO and the status registers (IIR and LSR).

write cycle timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 5)

		MIN	MAX	UNIT
t_{w5}	Pulse duration, $\overline{IOW}$ low	80		ns
t_{su4}	Setup time, chip select valid before $\overline{IOW}$ low (see Note 3)	15		ns
t_{su5}	Setup time, A2–A0 valid before $\overline{IOW}$ low (see Note 3)	15		ns
t_{su6}	Setup time, D0–D7 valid before $\overline{IOW}$ high	15		ns
t_{h3}	Hold time, A2–A0 valid after $\overline{IOW}$ high (see Note 3)	20		ns
t_{h4}	Hold time, chip select valid after $\overline{IOW}$ high (see Note 3)	20		ns
t_{h5}	Hold time, D0–D7 valid after $\overline{IOW}$ high	15		ns
t_{d3}	Delay time, $t_{su5} + t_{w5} + t_{d4}$	175		ns
t_{d4}	Delay time, $\overline{IOW}$ high to $\overline{IOW}$ or $\overline{IOR}$ low	80		ns

NOTE 3: The internal address strobe is always active.

read cycle switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figure 4)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{pd1}	Propagation delay time from $\overline{IOR}$ high to BDO high or from $\overline{IOR}$ low to BDO low	C_L = 100 pF, See Note 5		60	ns
t_{en}	Enable time from $\overline{IOR}$ low to D0–D7 valid	C_L = 100 pF, See Note 5		60	ns
t_{dis}	Disable time from $\overline{IOR}$ high to D0–D7 released	C_L = 100 pF, See Note 5	0	60	ns

NOTE 5: V_{OL} and V_{OH} (and the external loading) determine the charge and discharge time.

transmitter switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figures 6, 7, and 8)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{d5}	Delay time, interrupt THRE low to SOUT low at start		8	24	RCLK cycles
t_{d6}	Delay time, SOUT low at start to interrupt THRE high	See Note 6	8	8	RCLK cycles
t_{d7}	Delay time, $\overline{IOW}$ (WR THR) high to interrupt THRE high	See Note 6	16	32	RCLK cycles
t_{d8}	Delay time, SOUT low at start to $\overline{TXRDY}$ low	C_L = 100 pF		8	RCLK cycles
t_{pd2}	Propagation delay time from $\overline{IOW}$ (WR THR) low to interrupt THRE low	C_L = 100 pF		140	ns
t_{pd3}	Propagation delay time from $\overline{IOR}$ (RD IIR) high to interrupt THRE low	C_L = 100 pF		140	ns
t_{pd4}	Propagation delay time from $\overline{IOW}$ (WR THR) high to $\overline{TXRDY}$ high	C_L = 100 pF		195	ns

NOTE 6: When the transmitter interrupt delay is active, this delay si lengthened by one character time minus the last stop bit time.

receiver switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figures 9, 10, 11, 12 and 13)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{d9}	Delay time from stop to INT high	See Note 7		1	RCLK cycle
t_{pd5}	Propagation delay time from RCLK high to sample CLK high			100	ns
t_{pd6}	Propagation delay time from $\overline{IOR}$ (RD RBR/RD LSR) high to reset interrupt low	C_L = 100 pF		150	ns
t_{pd7}	Propagation delay time from $\overline{IOR}$ (RD RBR) low to $\overline{RXRDY}$ high			150	ns

NOTE 7: The receiver data available indication, the overrun error indication, the trigger level interrupts and the active $\overline{RXRDY}$ indication is delayed three RCLK cycles in the FIFO mode (FCR0 = 1). After the first byte has been received, status indicators (PE, FE, BI) is delayed three RCLK cycles. These indicators are updated immediately for any further bytes received after RD RBR goes active. There are eight RCLK cycle delays for trigger change level interrupts.

modem control switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figure 14)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{pd8}	Propagation delay time from $\overline{IOW}$ (WR MCR) high to $\overline{RTS}$ ($\overline{DTR}$) low/high	C_L = 100 pF		100	ns
t_{pd9}	Propagation delay time from modem input ($\overline{CTS}$, $\overline{DSR}$) low/high to interrupt high	C_L = 100 pF		170	ns
t_{pd10}	Propagation delay time from $\overline{IOR}$ (RD MSR) high to interrupt low	C_L = 100 pF		140	ns
t_{pd11}	Propagation delay time from $\overline{RI}$ high to interrupt high	C_L = 100 pF		170	ns

parallel port timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figure 15)

		MIN	MAX	UNIT
t_{su7}	Setup time, data valid before $\overline{STB}$ low	1		µs
t_{h6}	Hold time, data valid after $\overline{STB}$ high	1		µs
t_{w6}	Pulse duration, $\overline{STB}$ low	1	500	µs
t_{d10}	Delay time, BUSY high to $\overline{ACK}$ low	Defined by printer		
t_{d11}	Delay time, BUSY low to $\overline{ACK}$ low	Defined by printer		
t_{w6}	Pulse duration, $\overline{ACK}$ low	Defined by printer		
t_{w7}	Pulse duration, BUSY high	Defined by printer		
t_{d12}	Delay time, BUSY high after $\overline{STB}$ high	Defined by printer		

PARAMETER MEASUREMENT INFORMATION

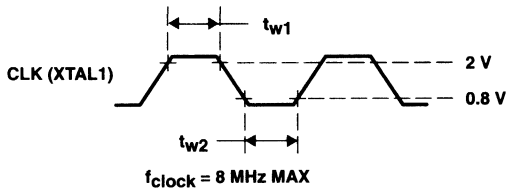
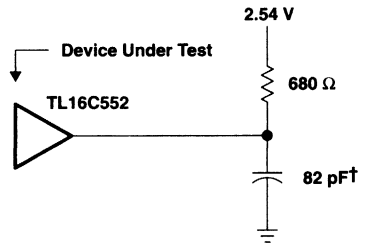


Figure 1. Clock Input (CLK) Voltage Waveform



†Includes scope and jig capacitance

Figure 2. Output Load Circuit

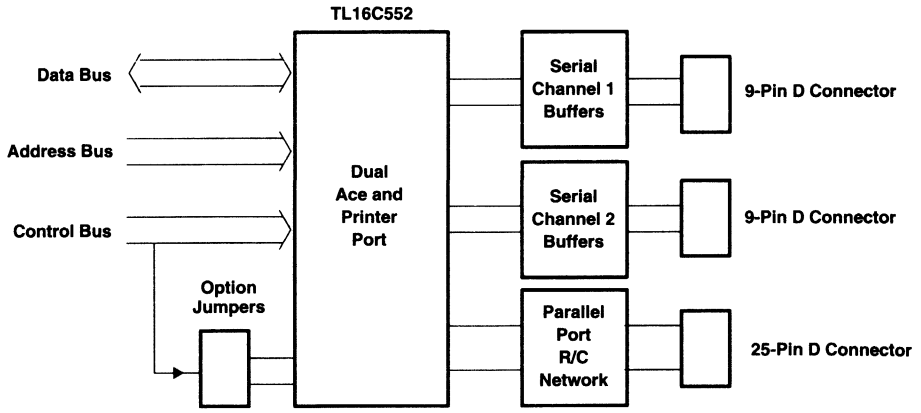


Figure 3. Basic Test Configuration

PARAMETER MEASUREMENT INFORMATION

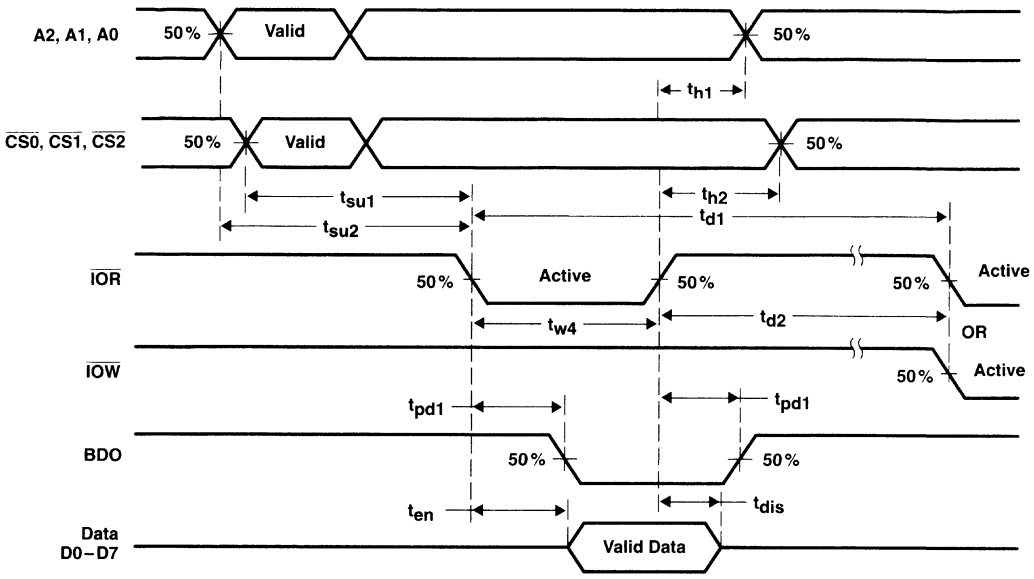


Figure 4. Read Cycle Timing Waveforms

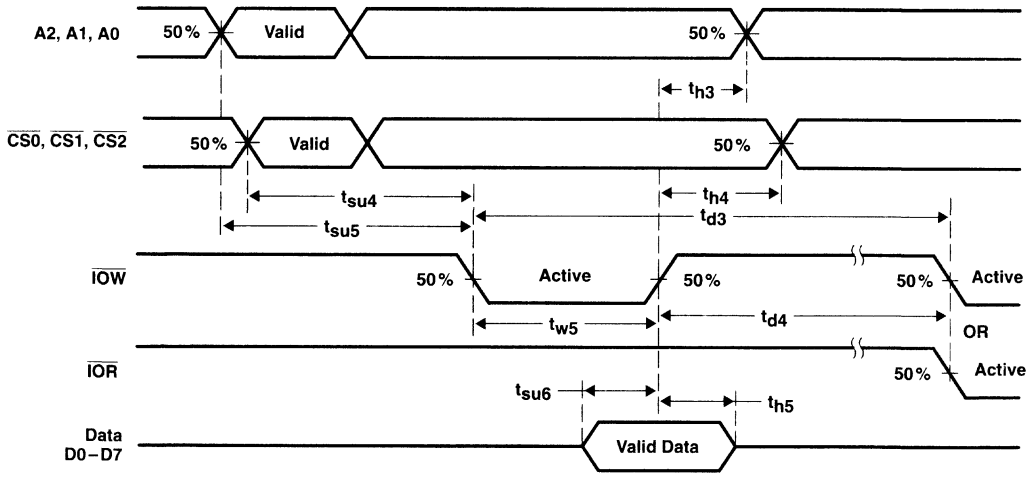


Figure 5. Write Cycle Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

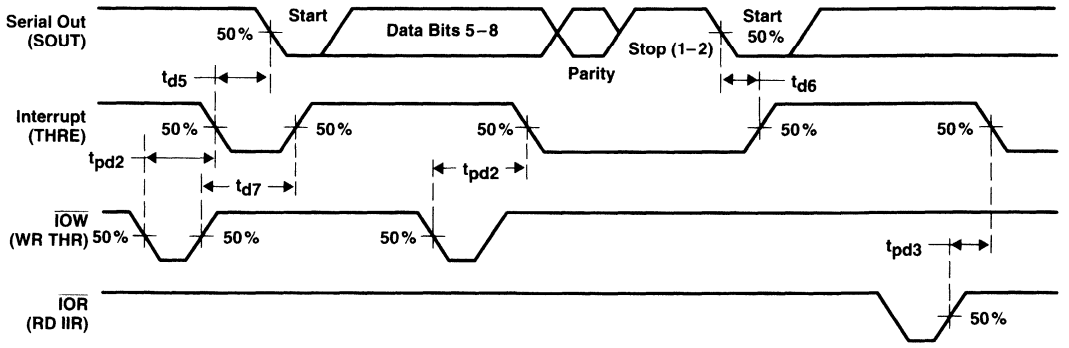


Figure 6. Transmitter Timing Waveforms

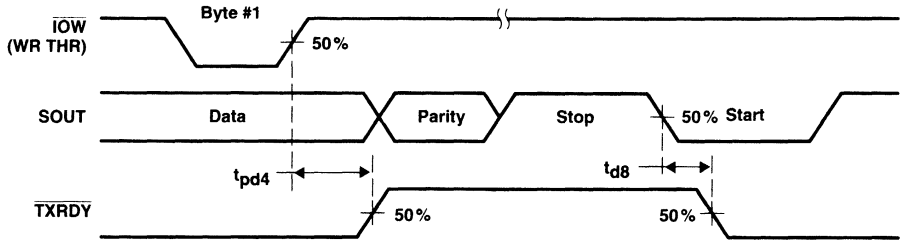


Figure 7. Transmitter Ready Mode 0 Timing Waveforms

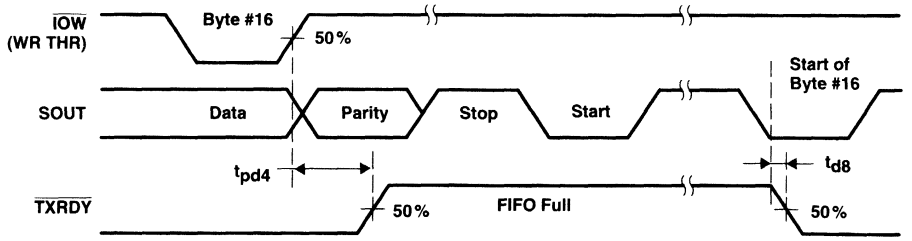


Figure 8. Transmitter Ready Mode 1 Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

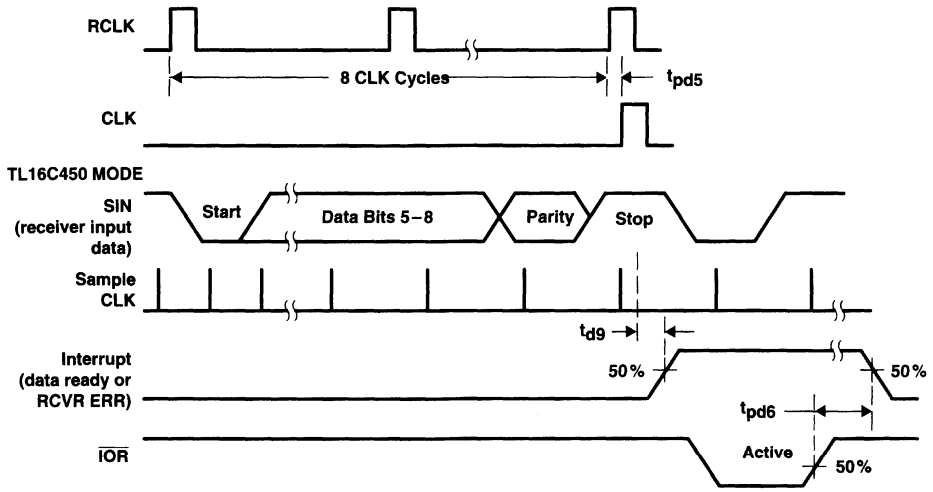


Figure 9. Receiver Timing Waveforms

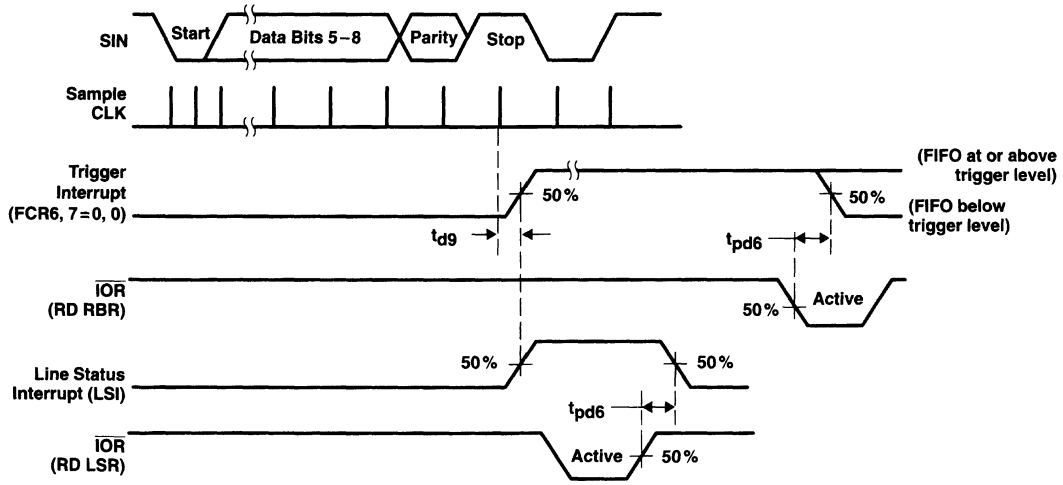


Figure 10. Receiver FIFO First Byte (Sets RDR) Waveforms

PARAMETER MEASUREMENT INFORMATION

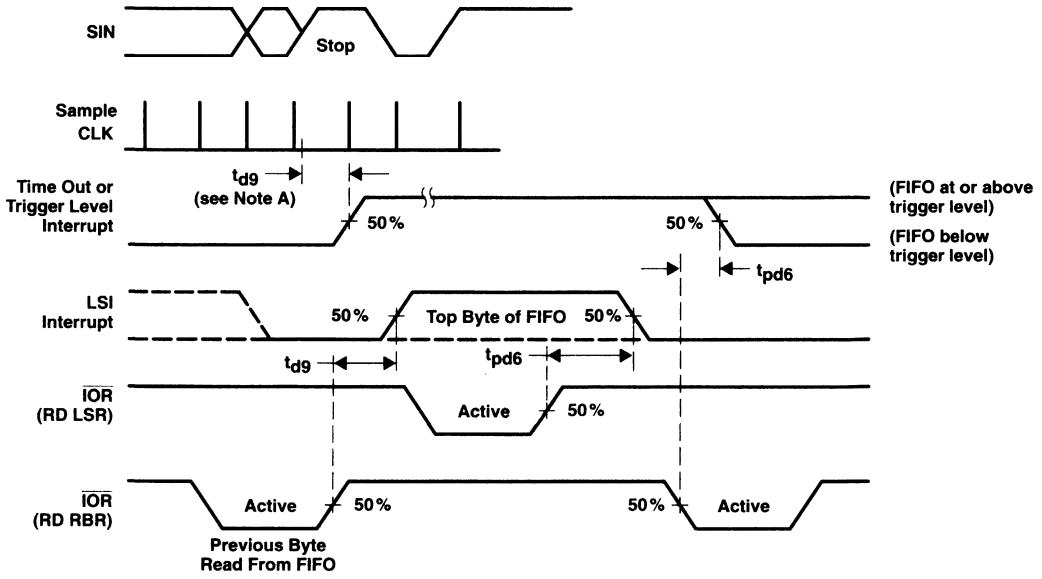


Figure 11. Receiver FIFO After First Byte (After RDR Set) Waveforms

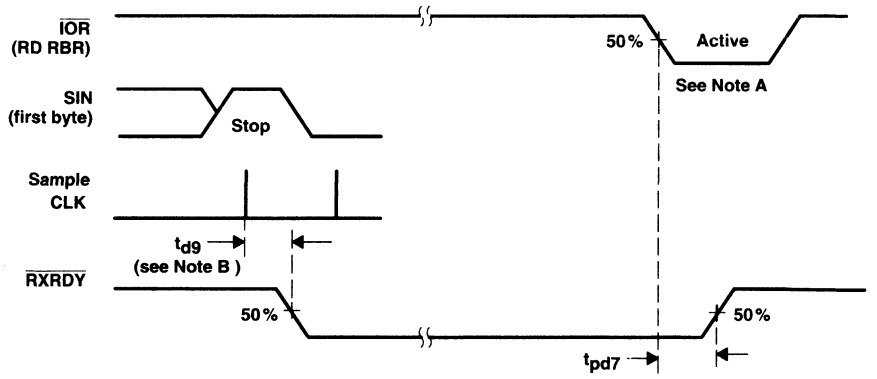
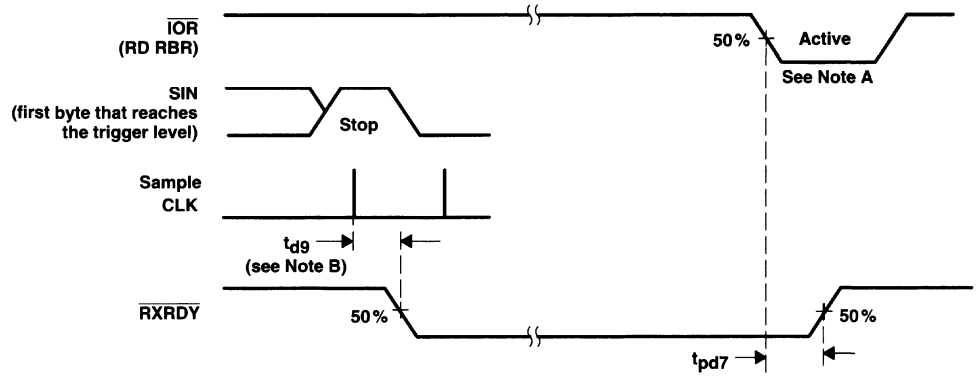


Figure 12. Receiver Ready Mode 0 Waveforms

NOTES: A. This is the reading of the last byte in the FIFO.
B. When FCR0=1, then t_{d9} = 3 RCLK cycles. For a time-out interrupt, t_{d9} = 8 RCLK cycles.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. This is the reading of the last byte in the FIFO.
B. When FCR0=1, then t_{d9} = 3 RCLK cycles. For a trigger change level interrupt, t_{d9} = 8 RCLK

Figure 13. Receiver Ready Mode 1 Waveforms

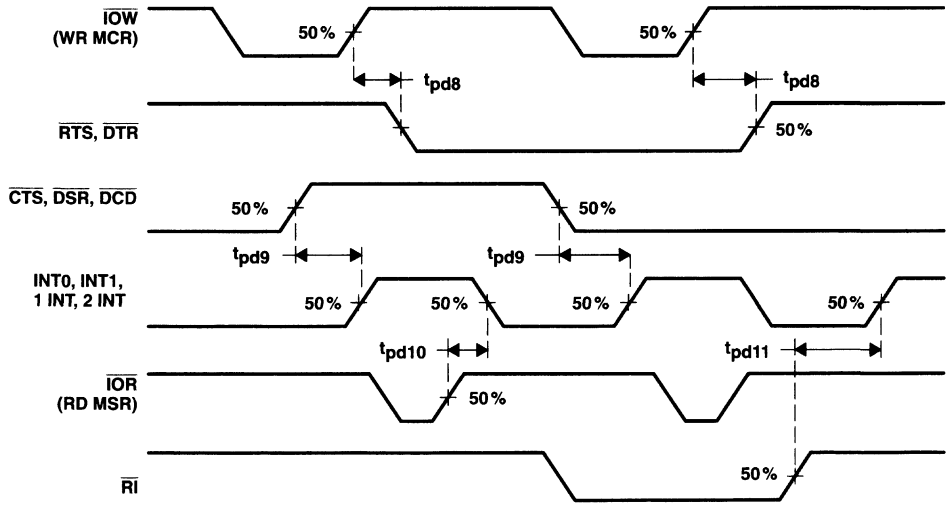


Figure 14. Modem Control Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

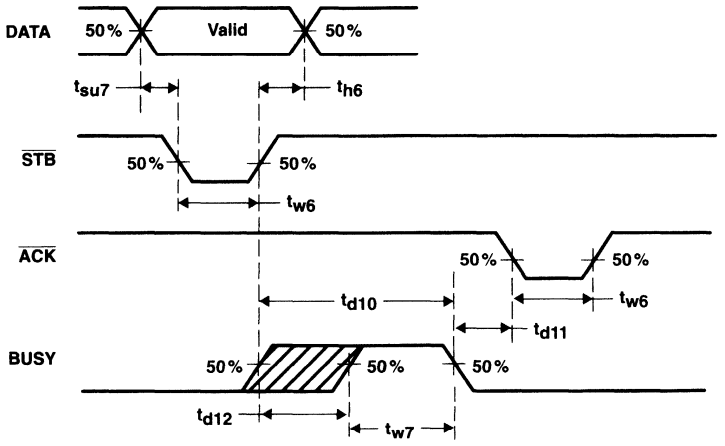


Figure 15. Parallel Port Timing Waveforms

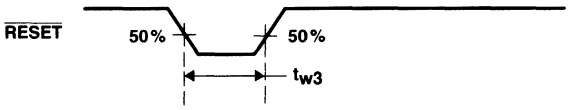


Figure 16. $\overline{\text{RESET}}$ Voltage Waveform

PRINCIPLES OF OPERATION

Three types of information are stored in the internal registers used in the ACE: control, status, and data. Mnemonic abbreviations are shown in the Table 1 for the registers.

Table 1. Internal Register Types With Mnemonics

CONTROL	MNEMONIC	STATUS	MNEMONIC	DATA	MNEMONIC
Line control register	LCR	Line status register	LSR	Receiver buffer register	RBR
FIFO control register	FCR	Modem status register	MSR	Transmitter holding register	THR
Modem control register	MCR				
Divisor latch LSB	DLL				
Divisor latch MSB	DLM				
Interrupt enable register	IER				

The address, read, and write inputs are used with the divisor latch access bit (DLAB) in the line control register (bit 7) to select the register to be written to or read from (see Table 2).

Table 2. Register Selection†‡

DLAB	A2	A1	A0	MNEMONIC	REGISTER
L	L	L	L	RBR	Receiver buffer register (read only)
L	L	L	L	THR	Transmitter holding register (write only)
L	L	L	H	IER	Interrupt enable register
X	L	H	L	IIR	Interrupt identification register (read only)
X	L	H	L	FCR	FIFO control register (write only)
X	L	H	H	LCR	Line control register
X	H	L	L	MCR	Modem control register
X	H	L	H	LSR	Line status register
X	H	H	L	MSR	Modem status register
X	H	H	H	SCR	Scratch register
H	L	L	L	DLL	Divisor latch (LSB)
H	L	L	H	DLM	Divisor latch (MSB)

† X = irrelevant, L = low level, H = high level
‡ The serial channel is accessed when either $\overline{CS0}$ or $\overline{CS1}$ is low.

Individual bits within the registers are referred to by the register mnemonic and the bit number in parenthesis. As an example, LCR7 refers to line control register bit 7.

The transmitter buffer register and receiver buffer register are data registers that hold from five to eight bits of data. If less than eight data bits are transmitted, data is right justified to the LSB. Bit 0 of a data word is always the first serial data bit received and transmitted. The ACE data registers are double buffered so that read and write operations may be performed when the ACE is performing the parallel-to-serial or serial-to-parallel conversion.

PRINCIPLES OF OPERATION

accessible registers

The system programmer, using the CPU, has access to and control over any of the ACE registers that are summarized in Table 2. These registers control ACE operations, receive data, and transmit data. Descriptions of these registers follow Table 3.

Table 3. Summary of Accessible Registers

ADDRESS	REGISTER MNEMONIC	REGISTER BIT NUMBER							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	RBR (read only)	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)
0	THR (write only)	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
0†	DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1†	DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
1	IER	0	0	0	0	(EDSSI) Enable modem status interrupt	(ERLSI) Enable receiver line status interrupt	(ETBEI) Enable transmitter holding register empty interrupt	(ERBFI) Enable received data available interrupt
2	FCR (write only)	Receiver Trigger (MSB)	Receiver Trigger (LSB)	Reserved	Reserved	DMA mode select	Tranmitter FIFO reset	Receiver FIFO reset	FIFO Enable
2	IIR (read only)	FIFOs Enabled‡	FIFOs Enabled‡	0	0	Interrupt ID Bit (2)‡	Interrupt ID Bit (1)	Interrupt ID Bit (0)	0 If interrupt pending
3	LCR	(DLAB) Divisor latch access bit	Set break	Stick parity	(EPS) Even parity select	(PEN) Parity enable	(STB) Number of stop bits	(WLSB1) Word length select bit 1	(WLSB0) Word length select bit 0
4	MCR	0	0	0	Loop	Enable external interrupt (INT0 or INT1)	OUT1 (an unused internal signal)	(RTS) Request to send	(DTR) Data terminal ready
5	LSR	Error in receiver FIFO‡	(TEMT) Transmitter empty	(THRE) Transmitter holding register empty	(BI) Break interrupt	(FE) Framing error	(PE) Parity error	(OE) Overrun error	(DR) Data ready
6	MSR	(DCD) Data carrier detect	(RI) Ring indicator	(DSR) Data set ready	(CTS) Clear to send	(ΔDCD) Delta data carrier detect	(TERI) Trailing edge ring indicator	(ΔDSR) Delta data set ready	(ΔCTS) Delta clear to send
7	SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

† DLAB = 1
‡ These bits are always 0 when FIFOs are disabled.

PRINCIPLES OF OPERATION

FIFO control register (FCR)

This write-only register is at the same location as the IIR. It enables and clears the FIFOs, sets the trigger level of the receiver FIFO, and selects the type of DMA signaling. The contents of FCR are described in Table 3 and the following bulleted list.

- Bit 0: FCR0 enables both the transmitter and receiver FIFOs. All bytes in both FIFOs can be reset by clearing FCR0. Data is cleared automatically from the FIFOs when changing from the FIFO mode to the TL16C450 mode and vice versa. Programming of other FCR bits is enabled by setting FCR0=1.
- Bit 1: FCR1=1 clears all bytes in the receiver FIFO and resets the counter. This does not clear the shift register.
- Bit 2: FCR2=1 clears all bytes in the transmitter FIFO and resets the counter. This does not clear the shift register.
- Bit 3: FCR3=1 changes the $\overline{\text{RXRDY}}$ and $\overline{\text{TXRDY}}$ terminals from mode 0 to mode 1 when FCR0=1.
- Bits 4 and 5: These two bits are reserved for future use.
- Bits 6 and 7: These two bits set the trigger level for the receiver FIFO interrupt as shown in Table 4.

Table 4. Receiver FIFO Trigger Level

BIT		RECEIVER FIFO TRIGGER LEVEL (BYTES)
7	6	
0	0	01
0	1	04
1	0	08
1	1	14

FIFO interrupt mode operation

The following receiver status occurs when the receiver FIFO and receiver interrupts are enabled:

1. LSR0 is set when a character is transferred from the shift register to the receiver FIFO. When the FIFO is empty, it is cleared.
2. IIR = 06 receiver line status interrupt has higher priority than the received data available interrupt IIR = 04.
3. Receive data available interrupt is issued to the CPU when the programmed trigger level is reached by the FIFO. As soon as the FIFO drops below its programmed trigger level, it is cleared.
4. IIR = 04 (receive data available indication) also occurs when the FIFO reaches its trigger level. It is cleared when the FIFO drops below the programmed trigger level.

The following receiver FIFO character time-out status occurs when receiver FIFO and receiver interrupts are enabled.

PRINCIPLES OF OPERATION

FIFO interrupt mode operation (continued)

1. A FIFO timeout interrupt occurs when the following conditions exist:
   a. Minimum of one character in FIFO
   b. Last received serial character was longer than four continuous previous character times ago (if two stop bits are programmed, the second one is included in the time delay).
   c. The last CPU read of the FIFO was more than four continuous character times earlier. At 300 baud and 12-bit characters, the FIFO time-out interrupt causes a latency of 160 ms maximum from received character to interrupt issued.
2. By using the RCLK input for a clock signal, the character times can be calculated. (The delay is proportional to the baud rate.)
3. The time-out timer is reset after the CPU reads the receiver FIFO or after a new character is received, when there has been no time-out interrupt.
4. A time-out interrupt is cleared and the timer is reset when the CPU reads a character from the receiver FIFO.

Transmitter interrupts occur as follows when the transmitter and transmitter FIFO interrupts are enabled (FCRO = 1, IER = 1).

1. When the transmitter FIFO is empty, the THR interrupt (IIR = 02) occurs. The interrupt is cleared as soon as the THR is written to or the IIR is read. One to sixteen characters can be written to the transmit FIFO when servicing this interrupt.
2. The transmitter FIFO empty indications are delayed one character time minus the last stop bit time whenever the following occurs:

   THRE = 1 and there has not been a minimum of two bytes at the same time in transmitter FIFO, since the last THRE = 1. The first transmitter interrupt after changing FCR0 is immediate, however, assuming it is enabled.

Receiver FIFO trigger level and character time-out interrupts have the same priority as the received data available interrupt. The THRE interrupt has the same priority as the transmitter FIFO empty interrupt.

FIFO polled mode operation

Clearing IER0, IER1, IER2, IER3, or all, with FCR0 = 1, puts the ACE into the FIFO polled mode. Receiver and transmitter are controlled separately. Therefore, either or both can be in the polled mode.

In the FIFO polled mode, there is no time-out condition indicated or trigger level reached. However, the receiver and transmitter FIFOs still have the capability of holding characters. The LSR must be read to determine the ACE status.

interrupt enable register (IER)

The IER independently enables the four serial channel interrupt sources that activate the interrupt (INT0 or INT1) output. All interrupts are disabled by clearing IER0 – IER3. Interrupts are enabled by setting the appropriate bits of the IER. Disabling the interrupt system inhibits the IIR and the active (high) interrupt output. All other system functions operate in their normal manner, including the setting of the LSR and MSR. The contents of the IER are described in Table 3 and in the following bulleted list.

- Bit 0: IER0, when set, enables the received data available interrupt and the time-out interrupts in the FIFO mode.

PRINCIPLES OF OPERATION

interrupt enable register (IER) (continued)

- Bit 1: IER1, when set, enables the THRE interrupt.
- Bit 2: IER2, when set, enables the receiver line status interrupt.
- Bit 3: IER3, when set, enables the modem status interrupt.
- Bits 4 – 7: IER4 – IER7 are always cleared.

interrupt identification register (IIR)

In order to minimize software overhead during data character transfers, the serial channel prioritizes interrupts into four levels. The four levels of interrupt conditions are shown in the following bulleted list:

- Priority 1 – Receiver line status (highest priority)
- Priority 2 – Receiver data ready or receiver character time out
- Priority 3 – Transmitter holding register empty
- Priority 4 – Modem status (lowest priority)

Information indicating that a prioritized interrupt is pending and the type of interrupt is stored in the IIR. The IIR indicates the highest priority interrupt pending. The contents of the IIR are indicated in Table 5.

Table 5. Interrupt Control Functions

FIFO MODE ONLY	INTERRUPT IDENTIFICATION REGISTER			INTERRUPT SET AND RESET FUNCTIONS			
BIT 3	BIT 2	BIT 1	BIT 0	PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET CONTROL
0	0	0	1	–	None	None	–
0	1	1	0	First	Receiver line status	OE, PE, FE, or BI	LSR read
0	1	0	0	Second	Received data available	Receiver data available or trigger level reached	RBR read until FIFO drops below the trigger level
1	1	0	0	Second	Character time-out indication	No characters have been removed from or input to the receiver FIFO during the last four character times and there is at least one character in it during this time.	RBR read
0	0	1	0	Third	THRE	THRE	IIR read if THRE is the interrupt source or THR write
0	0	0	0	Fourth	Modem status	$\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$, or $\overline{DCD}$	MSR read

- Bit 0: IIR0 indicates whether an interrupt is pending. When IIR0 is cleared, an interrupt is pending.
- Bits 1 and 2: IIR1 and IIR2 identify the highest priority interrupt pending as indicated in Table 5.
- Bit 3: IIR3 is always cleared when in the TL16C450 mode. This bit is set along with bit 2 when in the FIFO mode and a trigger change level interrupt is pending.
- Bits 4 and 5: IIR4 and IIR5 are always cleared.
- Bits 6 and 7: IIR6 and IIR7 are set when FCR0=1.

PRINCIPLES OF OPERATION

line control register (LCR)

The format of the data character is controlled by the LCR. The LCR may be read. Its contents are described in the following bulleted list and shown in Figure 17.

- Bits 0 and 1: LCR0 and LCR1 are the word length select bits. The number of bits in each serial character is programmed as shown in Figure 17.
- Bit 2: LCR2 is the stop bit select bit. LCR2 specifies the number of stop bits in each transmitted character as shown in Figure 17. The receiver always checks for one stop bit.
- Bit 3: LCR3 is the parity enable bit 3. When LCR3 is high, a parity bit between the last data word bit and stop bit is generated and checked.
- Bit 4: LCR4 is the even parity select bit 4. When enabled, setting this bit selects even parity.
- Bit 5: LCR5 is the stick parity bit 5. When parity is enabled (LCR3=1), LCR5=1 causes the transmission and reception of a parity bit to be in the opposite state from the value of LCR4. This forces parity to a known state and allows the receiver to check the parity bit in a known state.
- Bit 6: LCR6 is the break control bit 6. When LCR6 is set, the serial output (SOUT1 and SOUT0) is forced to the spacing state (low). The break control bit acts only on the serial output and does not affect the transmitter logic. When the following sequence is used, no invalid characters are transmitted because of the break:

  Step 1. Load a zero byte in response to the transmitter holding register empty (THRE) status indication.

  Step 2. Set the break in response to the next THRE status indication.

  Step 3. Wait for the transmitter to be idle when transmitter empty status signal is set high (TEMT=1). Then clear the break when the normal transmission has to be restored.

- Bit 7: LCR7 is the divisor latch access bit (DLAB) bit 7. Bit 7 must be set to access the divisor latches DLL and DLM of the baud rate generator during a read or write operation. LCR7 must be cleared to access the receiver buffer register, the transmitter holding register or the interrupt enable register.

PRINCIPLES OF OPERATION

line control register (LCR) (continued)

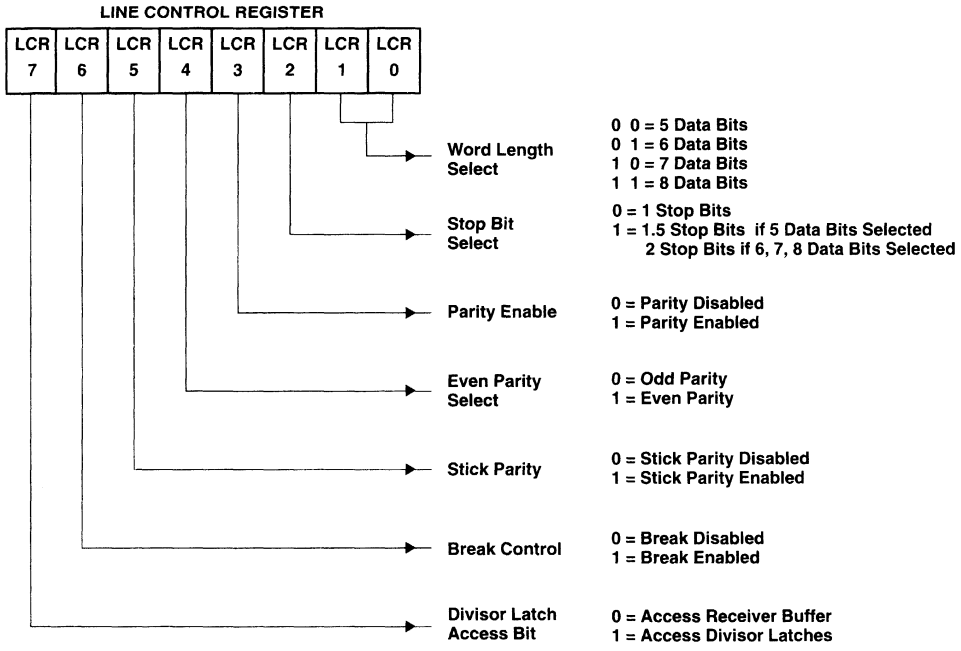


Figure 17. Line Control Register Contents

line printer port (LPT)

The line printer port contains the functionality of the port included in the TL16C452, but offers a hardware programmable extended mode controlled by the printer enhancement mode (PEMD) terminal. This enhancement is the addition of a direction control bit, and an interrupt status bit.

register 0 line printer data register (LPD)

The LPD port is either output only or bidirectional, depending on the state of the extended mode terminal and data direction control bits.

- Compatibility mode (PEMD is low). Reads to the LPD register return the last data that was written to the port. Write operations immediately output data to the PD0–PD7 terminals.
- Extended mode (PEMD is high). Read operations return either the data last written to the LPT data register when the direction bit is cleared to write, or the data that is present on PD0–PD7 when the direction is set to read. Writes to the LPD register latch data into the output register, but only drive the LPT port when the direction bit is cleared to write.

PRINCIPLES OF OPERATION

line printer port (LPT) (continued)

Table 6 summarizes the possible combinations of extended mode and the direction control bit. In either case, the bits of the LPD register are defined as follows:

Table 6. Extended Mode and Direction Control Bit Combinations

PEMD	DIR	PD0–PD7 FUNCTION
L	X	PC/AT mode – output
H	0	PS/2™ mode – output
H	1	PS/2™ mode – input

register 1 read line printer status register

The line printer status (LPS) register is a read-only register that contains interrupt and printer status of the LPT connector terminals. In Table 7 (in the default column), are the values of each bit after reset in the case of the printer being disconnected from the port.

Table 7. LPS Register Bit Description

BIT	DESCRIPTION	DEFAULT
0	Reserved	1
1	Reserved	1
2	$\overline{\text{PRINT}}$	1
3	$\overline{\text{ERR}}$	†
4	SLCT	†
5	PE	†
6	$\overline{\text{ACK}}$	†
7	$\overline{\text{BSY}}$	†

† Outputs are dependent upon device inputs.

- Bits 0 and 1: These bits are reserved and are always set.
- Bit 2: This bit is the printer interrupt ($\overline{\text{PRINT}}$, active low) status bit. When cleared indicates that the printer has acknowledged the previous transfer with an ACK handshake (bit 4 of the control register is set). The bit is cleared on the active to inactive transition of the $\overline{\text{ACK}}$ signal. This bit is set after a read of the status port.
- Bit 3: This bit is the error ($\overline{\text{ERR}}$, active low) status bit corresponds to $\overline{\text{ERR}}$ input.
- Bit 4: This bit is the select (SLCT) status bit corresponds to SLCT input.
- Bit 5: This bit is the paper empty (PE) status bit corresponds to PE input.
- Bit 6: This bit is the acknowledge ($\overline{\text{ACK}}$, active low) status bit corresponds to $\overline{\text{ACK}}$ input.
- Bit 7: This bit is the busy ($\overline{\text{BSY}}$, active low) status bit corresponds to BUSY input (active high).

register 2 line printer control (LPC) register

The LPC register is read/write port that controls the PD0–PD7 direction and drive the printer control lines. Write operations set or clear these bits, while read operations return the state of the last write operation to this register. The bits in this register are described in Table 8.

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PRINCIPLES OF OPERATION

line printer port (LPT) (continued)

Table 8. LPC Register Bit Description

BIT	DESCRIPTION
0	STB
1	AFD
2	$\overline{\text{INIT}}$
3	SLIN
4	INT2 EN
5	DIR
6	Reserved (0)
7	Reserved (0)

- Bit 0: This bit is the printer strobe (STB) control bit. When this bit is set, the $\overline{\text{STB}}$ signal is asserted on the LPT interface. When STB is cleared, the signal is negated.
- Bit 1: This bit is the auto feed (AFD) control bit. When this bit is set, the $\overline{\text{AFD}}$ signal is asserted on the LPT interface. When AFD is cleared, the signal is negated.
- Bit 2: This bit is the initialize printer ($\overline{\text{INIT}}$) control bit. When this bit is set, the $\overline{\text{INIT}}$ signal is negated. When $\overline{\text{INIT}}$ is cleared, the $\overline{\text{INIT}}$ signal is asserted on the LPT interface.
- Bit 3: This bit is the select input (SLIN) control bit. When this bit is set, the SLCT signal is asserted on the LPT interface. when SLIN is cleared, the signal is negated.
- Bit 4: This bit is the interrupt request enable (INT2 EN) control bit. When set, this bit enables interrupts from the LPT port whenever the $\overline{\text{ACK}}$ signal is released. When cleared, INT2 EN disables interrupts and places INT2 signal in 3-state.
- Bit 5: This bit is the direction (DIR) control bit (only used when PEMD is high). When this bit is set, the output buffers in the LPD port are disabled allowing data driven from external sources to be read from the LPD port. When DIR is cleared, the LPD port is in output mode.

line status register (LSR)

The LSR is a single register that provides status indications. The LSR is shown in Table 9 and is described in the following bulleted list.

Table 9. Line Status Register Bits

LSR BITS	1	0
LSR0 data ready (DR)	Ready	Not ready
LSR1 overrun error (OE)	Error	No error
LSR2 parity error (PE)	Error	No error
LSR3 framing error (FE)	Error	No error
LSR4 break interrupt (BI)	Break	No break
LSR5 THRE	Empty	Not empty
LSR6 transmitter empty (TEMT)	Empty	Not empty
LSR7 receiver FIFO error	Error in FIFO	No error in FIFO

† LSR is intended only for factory test. It should be considered as read only by applications software.

PRINCIPLES OF OPERATION

line status register (LSR) (continued)

- Bit 0: LSR0 is the data ready (DR) bit. DR is set high when an incoming character has been received and transferred into the receiver buffer register or the FIFO. LSR0 is cleared by a CPU read of the data in the receiver buffer register or the FIFO.
- Bit 1: SR1 is the overrun error (OE) bit. OE indicates that data in the receiver buffer register was not read by the CPU before the next character was transferred into the receiver buffer register overwriting the previous character. The OE indicator is cleared whenever the CPU reads the contents of the LSR. An OE occurs in the FIFO mode after the FIFO is full and the next character is completely received. The OE is detected by the CPU on the first LSR read after the overrun happens. The character in the shift register is not transferred to the FIFO but it is overwritten.
- Bit 2: LSR2 is the parity error (PE) bit. PE indicates that the received data character does not have the correct parity as selected by LCR3 and LCR4. The PE bit is set upon detection of a parity error and is cleared when the CPU reads the contents of the LSR. In the FIFO mode, the parity error is associated with a particular character in the FIFO. LSR2 reflects the error when the character is at the top of the FIFO.
- Bit 3: LSR3 is the framing error (FE) bit. FE indicates that the received character did not have a valid stop bit. LSR3 is set when the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE indicator is cleared when the CPU reads the contents of the LSR. In the FIFO mode, the framing error is associated with a particular character in the FIFO. LSR3 reflects the error when the character is at the top of the FIFO.
- Bit 4: LSR4 is the break interrupt (BI) bit. BI is set when the received data input is held in the spacing (cleared) state for longer than a full word transmission time (start bit + data bits + parity + stop bits). The BI indicator is cleared when the CPU reads the contents of the LSR. In the FIFO mode, this is associated with a particular character in the FIFO. LSR2 reflects the BI when the break character is at the top of the FIFO. The error is detected by the CPU when its associated character is at the top of the FIFO during the first LSR read. Only one zero character is loaded into the FIFO when BI occurs.

LSR1 – LSR4 are the error conditions that produce a receiver line status interrupt (priority 1 interrupt in the interrupt identification register) when any of the conditions are detected. This interrupt is enabled by setting IER2=1 in the interrupt enable register.

- Bit 5: LSR5 is the THRE bit. THRE indicates that the ACE is ready to accept a new character for transmission. The THRE bit is set when a character is transferred from the transmitter holding register (THR) into the transmitter shift register (TSR). LSR5 is cleared by the loading of the transmitter holding register by the CPU. LSR5 is not reset by a CPU read of the LSR. In the FIFO mode when the transmitter FIFO is empty, this bit is set. It is cleared when one byte is written to the transmitter FIFO. When the THRE interrupt is enabled by IER1, THRE causes a priority 3 interrupt in the IIR. When THRE is the interrupt source indicated in IIR, INTRPT is cleared by a read of the IIR.
- Bit 6: LSR6 is the transmitter empty (TEMT) bit. TEMT is set when the THR and the TSR are both empty. LSR6 is cleared when a character is loaded into the THR and remains low until the character is transferred out of SOUT. TEMT is not cleared by a CPU read of the LSR. In the FIFO mode, when both the transmitter FIFO and shift register are empty, this bit is set.
- Bit 7: LSR7 is the receiver FIFO error bit. The LSR7 bit is always cleared in the TL16C450 mode. In FIFO mode, it is set when at least one of the following data errors is in the FIFO: PE, FE, or BI indication. It is cleared when the CPU reads the LSR if there are no subsequent errors in the FIFO.

PRINCIPLES OF OPERATION

master reset

After power up, the ACE $\overline{\text{RESET}}$ input should be held low for one microsecond to reset the ACE circuits to an idle mode until initialization. A low on $\overline{\text{RESET}}$ causes the following:

1. It initializes the transmitter and receiver clock counters.
2. It clears the LSR, except for TEMT and THRE, which are set. The MCR is also cleared. All of the discrete lines, memory elements, and miscellaneous logic associated with these register bits are also cleared or turned off. The LCR, divisor latches, RBR, and transmitter buffer register are not effected.

Following the removal of the reset condition ($\overline{\text{RESET}}$ high), the ACE remains in the idle mode until programmed.

A hardware reset of the ACE sets the THRE and TEMT status bit in the LSR. When interrupts are subsequently enabled, an interrupt occurs due to THRE. A summary of the affect of a reset on the ACE is given in Table 10.

Table 10. $\overline{\text{RESET}}$ Affects On Registers and Signals

REGISTER/SIGNAL	RESET CONTROL	RESET
Interrupt enable register	Reset	All bits cleared (0–3 forced and 4–7 permanent)
Interrupt identification register	Reset	Bit 0 is set, bits 1, 2, 3, 6, and 7 cleared Bits 4–5 are permanently cleared
Line control register	Reset	All bits cleared
Modem control register	Reset	All bits cleared
FIFO control register	Reset	All bits cleared
Line status register	Reset	All bits cleared, except bits 5 and 6 are set
Modem status register	Reset	Bits 0–3 cleared, bits 4–7 input signal
SOUT	Reset	High
Interrupt (receiver errs)	Read LSR/Reset	Cleared
Interrupt (receiver data ready)	Read RBR/Reset	Cleared
Interrupt (THRE)	Read IIR/Write THR/Reset	Cleared
Interrupt (modem status changes)	Read MSR/Reset	Cleared
$\overline{\text{OUT2}}$	Reset	High
$\overline{\text{RTS}}$	Reset	High
$\overline{\text{DTR}}$	Reset	High
$\overline{\text{OUT1}}$	Reset	High

PRINCIPLES OF OPERATION

modem control register (MCR)

The MCR controls the interface with the modem or data set as described in Figure 18. The MCR can be written to and read from. The $\overline{RTS}$ and $\overline{DTR}$ outputs are directly controlled by their control bits in this register. A high input asserts a low (true) at the output terminals. MCR bits 0, 1, 2, 3, and 4 are shown as follows:

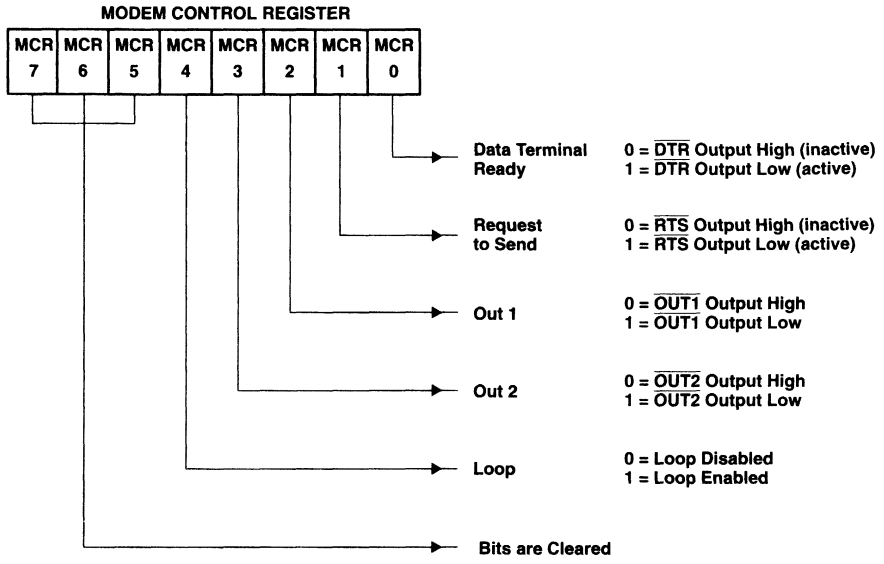


Figure 18. Modem Control Register Contents

- Bit 0: When MCR0 is set, the $\overline{DTR}$ output is forced low. When MCR0 is cleared, the $\overline{DTR}$ output is forced high. The $\overline{DTR}$ output of the serial channel can be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.
- Bit 1: When MCR1 is set, the $\overline{RTS}$ output is forced low. When MCR1 is cleared, the $\overline{RTS}$ output is forced high. The $\overline{RTS}$ output of the serial channel can be input into an inverting line driver to obtain the proper polarity input at the modem or data set.
- Bit 2: When MCR2 is set, $\overline{OUT1}$ is forced low.
- Bit 3: When MCR3 is set, the $\overline{OUT2}$ output is forced low.
- Bit 4: MCR4 provides a local loopback feature for diagnostic testing of the channel. When MCR4 is set, serial output (SOUT) is set to the marking (high) state, and the SIN is disconnected. The output of the TSR is looped back into the receiver shift register input. The four modem control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$) are disconnected. The modem control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OIUT1}$, and $\overline{OUT2}$) are internally connected to the four modem control inputs. The modem control output terminals are forced to their inactive state (high) on the TL16C552. In the diagnostic mode, data transmitted is immediately received. This allows the processor to verify the transmit and receive data paths of the selected serial channel. Interrupt control is fully operational. However, interrupts are generated by controlling the lower four MCR bits internally. Interrupts are not generated by activity on the external terminals represented by those four bits.
- Bits 5 – 7: These three bits(MCR5 – MCR7) are permanently cleared.

PRINCIPLES OF OPERATION

modem status register (MSR)

The MSR provides the CPU with status of the modem input lines from the modem or peripheral devices. The MSR allows the CPU to read the serial channel modem signal inputs by accessing the data bus interface of the ACE in addition to the current status of four bits of the MSR that indicate whether the modem inputs have changed since the last reading of the MSR. The delta status bits are set when a control input from the modem changes state and cleared when the CPU reads the MSR.

The modem input lines are $\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$, and $\overline{DCD}$. MSR4 – MSR7 are status indications of these lines. A status bit = 1 indicates the input is a low. A status bit = 0 indicates the input is high. When the modem status interrupt in the interrupt enable register is enabled (IER3), an interrupt is generated whenever MSR0 – MSR3 is set. The MSR is a priority 4 interrupt. The contents of the MSR are described in Table 11.

Table 11. Modem Status Register Bits

MSR BIT	MNEMONIC	DESCRIPTION
MSR0	ΔCTS	Delta clear to send
MSR1	ΔDSR	Delta data set ready
MSR2	TERI	Trailing edge of ring indicator
MSR3	ΔDCD	Delta data carrier detect
MSR4	$\overline{CTS}$	Clear to send
MSR5	$\overline{DSR}$	Data set ready
MSR6	$\overline{RI}$	Ring indicator
MSR7	$\overline{DCD}$	Data carrier detect

- Bit 0: MSR0 is the delta clear to send (ΔCTS) bit. ΔCTS displays that the $\overline{CTS}$ input to the serial channel has changed state since it was last read by the CPU.
- Bit 1: MSR1 is the delta data set ready (ΔDSR) bit. ΔDSR indicates that the $\overline{DSR}$ input to the serial channel has changed state since the last time it was read by the CPU.
- Bit 2: MSR2 is the trailing edge of ring indicator (TERI) bit. TERI indicates that the $\overline{RI}$ input to the serial channel has changed states from low to high since the last time it was read by the CPU. High-to-low transitions on RI do not activate TERI.
- Bit 3: MSR3 is the delta data carrier detect (ΔDCD) bit. ΔDCD indicates that the $\overline{DCD}$ input to the serial channel has changed state since the last time it was read by the CPU.
- Bit 4: MSR4 is the clear to send (CTS) bit. CTS is the complement of the $\overline{CTS}$ input from the modem indicating to the serial channel that the modem is ready to receive data from SOUT. When the serial channel is in the loop mode ((MCR4 = 1), MSR4 reflects the value of RTS in the MCR.
- Bit 5: MSR5 is the data set ready (DSR) bit. DSR is the complement of the $\overline{DSR}$ input from the modem to the serial channel that indicates that the modem is ready to provide received data to the serial channel receiver circuitry. When the channel is in the loop mode (MCR4=1), MSR5 reflects the value of DTR in the MCR.
- Bit 6: MSR6 is the ring indicator (RI) bit. RI is the complement of the $\overline{RI}$ input. When the channel is in the loop mode (MCR4=1), MSR6 reflects the value of $\overline{OUT1}$ in the MCR.
- Bit 7: MSR7 is the data carrier detect (DCD) bit. DCD indicates the status of the data carrier detect ($\overline{DCD}$) input. When the channel is in the loop mode (MCR4=1), MSR7 reflects the value of OUT2 in the MCR.

PRINCIPLES OF OPERATION

modem status register (MSR) (continued)

Reading the MSR register clears the delta modem status indications but has no affect on the other status bits. For LSR and MSR, the setting of status bits is inhibited during status register read operations. When a status condition is generated during a read $\overline{IOR}$ operation, the status bit is not set until the trailing edge of the read. If a status bit is set during a read operation, and the same status condition occurs, that status bit is cleared at the trailing edge of the read instead of being set again. In the loop back mode, when modem status interrupts are enabled, the $\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$ and $\overline{DCD}$ input terminals are ignored. However, a modem status interrupt can still be generated by writing to MCR3 – MCR0. Applications software should not write to the MSR.

parallel port registers

The TL16C552 parallel port can interface to the device to a Centronics-style printer interface. When chip select 2 ($\overline{CS2}$) is low, the parallel port is selected. Table 12 shows the registers associated with this parallel port. The read or write function of the register is controlled by the state of the read ($\overline{IOR}$) and write ($\overline{IOW}$) terminal as shown. The read data register allows the microprocessor to read the information on the parallel bus.

The read status register allows the microprocessor to read the status of the printer in the six most significant bits. The status bits are printer busy $\overline{BSY}$, acknowledge ($\overline{ACK}$) which is a handshake function, paper empty (PE), printer selected ($\overline{SLCT}$), error ($\overline{ERR}$) and printer interrupt ($\overline{PRINT}$). The read control register allows the state of the control lines to be read. The write control register sets the state of the control lines. They are direction (DIR), interrupt enable (INT2 EN), select in ($\overline{SLIN}$), initialize the printer ($\overline{INIT}$), autofeed the paper ($\overline{AFD}$), and strobe ($\overline{STB}$), which informs the printer of the presence of a valid byte on the parallel bus. The write data register allows the microprocessor to write a byte to the parallel bus. The parallel port is completely compatible with the parallel port implementation used in the IBM™ serial parallel adaptor.

Table 12. Parallel Port Registers

REGISTER	REGISTER BITS							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Read Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Read Status	$\overline{BSY}$	$\overline{ACK}$	PE	SLCT	$\overline{ERR}$	$\overline{PRINT}$	1	1
Read Control	0	0	DIR	INT2 EN	SLIN	$\overline{INIT}$	AFD	STB
Write Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Write Control	0	0	DIR	INT2 EN	SLIN	$\overline{INIT}$	AFD	STB

Table 13. Parallel Port Register Select

CONTROL TERMINALS					REGISTER SELECTED
$\overline{IOR}$	$\overline{IOW}$	$\overline{CS2}$	A1	A0	
L	H	L	L	L	Read data
L	H	L	L	H	Read status
L	H	L	H	L	Read control
L	H	L	H	H	Invalid
H	L	L	L	L	Write data
H	L	L	L	H	Invalid
H	L	L	H	L	Write control
H	L	L	H	H	Invalid

PRINCIPLES OF OPERATION

programmable baud generator

The ACE serial channel contains a programmable baud rate generator that divides the clock (dc to 8 MHz) by any divisor from 1 to ($2^{16}-1$). The output frequency of the baud rate generator is 16× the data rate (divisor # = clock ÷ (baud rate × 16)) referred to in this document as RCLK. Two 8-bit divisor latch registers store the divisor in a 16-bit binary format. These divisor latch registers must be loaded during initialization. Upon loading either of the divisor latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load. The baud rate generator can use any of three different popular frequencies to provide standard baud rates. These frequencies are 1.8432 MHz, 3.072 MHz, and 8 MHz. With these frequencies, standard bit rates from 50- to 512-kbits/s are available. Tables 14, 15, and 16 illustrate the divisors needed to obtain standard rates using these three frequencies.

Table 14. Baud Rates Using a 1.8432-MHz Crystal

BAUD RATE DESIRED	DIVISOR (N) USED TO GENERATE 16 X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	–
75	1536	–
110	1047	0.026
134.5	857	0.058
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.690
2400	48	–
3600	32	–
4800	24	–
7200	16	–
9600	12	–
19200	6	–
38400	3	–
56000	2	2.860

Table 15. Baud Rates Using a 3.072-MHz Crystal

BAUD RATE DESIRED	DIVISOR (N) USED TO GENERATE 16 X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	–
75	2560	–
110	1745	0.026
134.5	1428	0.034
150	1280	–
300	640	–
600	320	–
1200	160	–
1800	107	0.312
2000	96	–
2400	80	–
3600	53	0.628
4800	40	–
7200	27	1.230
9600	20	–
19200	10	–
38400	5	–

PRINCIPLES OF OPERATION

programmable baud generator (continued)

Table 16. Baud Rates Using a 8.192-MHz Crystal

BAUD RATE DESIRED	DIVISOR (N) USED TO GENERATE 16 X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	1000	–
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	3333	0.010
300	1667	0.020
600	833	0.040
1200	417	0.080
1800	277	0.080
2000	250	–
2400	208	0.160
3600	139	0.080
4800	104	0.160
7200	69	0.644
9600	52	0.160
19200	26	0.160
38400	13	0.160
56000	9	0.790
128000	4	2.344
256000	2	2.344
512000	1	2.400

programming

The serial channel of the ACE is programmed by the control registers: LCR, IER, DLL, DLM, MCR, and FCR. These control words define the character length, number of stop bits, parity, baud rate, and modem interface.

While the control registers can be written in any order, the IER should be written last because it controls the interrupt enables. Once the serial channel is programmed and operational, these registers can be updated any time the ACE serial channel is not transmitting or receiving data.

receiver

Serial asynchronous data is input into the SIN terminal. The ACE continually searches for a high-to-low transition
from the idle state. When the transition is detected, a counter is cleared, and counts the 16× clock to 7 1/2, which is the center of the start bit. The start bit is valid when the SIN is still low. Verifying the start bits prevents the receiver from assembling a false data character due to a low-going noise spike on the SIN input.

The LCR determines the number of data bits in a character [LCR0, LCR1]. When parity is used LCR3 and the polarity of parity LCR4 are needed. Status for the receiver is provided in the LSR. When a full character is received, including parity and stop bits, the data received indication in LSR0 is set. The CPU reads the RBR, which clears LSR0. If the character is not read prior to a new character transfer from the RSR to the RBR, the OE status indication is set in LSR1. When there is a PE, the PE bit is set in LSR2. If a stop bit is not detected, a FE indication is set in LSR3.

When the data into SIN is a symmetrical square wave, the center of the data cells occurs within ±3.125% of the actual center, providing an error margin of 46.875%. The start bit can begin as much as one 16× clock cycle prior to being detected.

PRINCIPLES OF OPERATION

scratchpad register

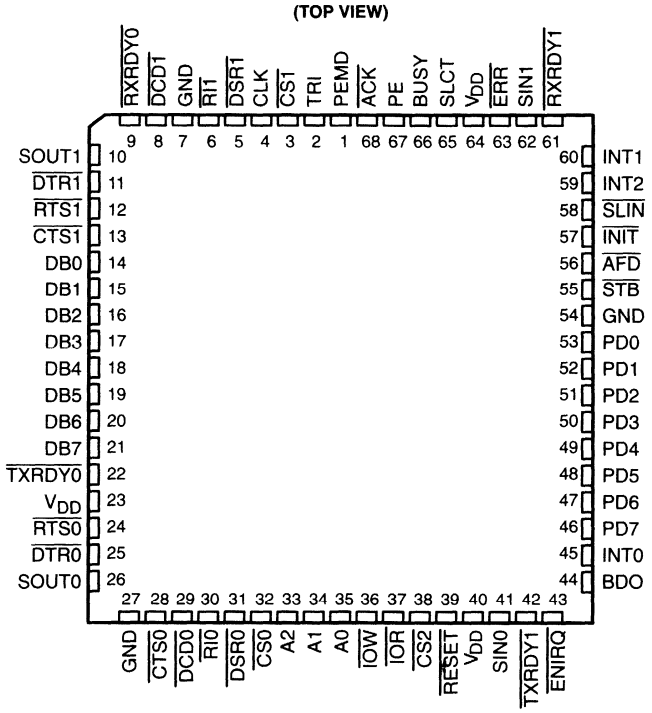
The scratch register is an 8-bit read/write register that has no affect on either channel in the ACE. It is intended to be used by the programmer to temporarily hold data.

TL16C552A
DUAL ASYNCHRONOUS COMMUNICATIONS ELEMENT WITH FIFO

SLLS176B – FEBRUARY 1994 – REVISED MARCH 1996

- **IBM PC/AT™ Compatible**
- **Two TL16C550 ACEs**
- **Enhanced Bidirectional Printer Port**
- **16-Byte FIFOs Reduce CPU Interrupts**
- **Up to 16-MHz Clock Rate for up to 1-Mbaud Operation**
- **Independent Control of Transmit, Receive, Line Status, and Data Set Interrupts on Each Channel**
- **Individual Modem Control Signals for Each Channel**
- **Programmable Serial Interface Characteristics for Each Channel:**
  - **5-, 6-, 7-, or 8-Bit Characters**
  - **Even-, Odd-, or No-Parity-Bit Generation and Detection**
  - **1-, 1 1/2-, or 2-Stop Bit Generation**
- **3-State Outputs Provide TTL Drive for the Data and Control Bus on Each Channel**
- **Hardware and Software Compatible With TL16C452**

FN PACKAGE
(TOP VIEW)



description

The TL16C552A is an enhanced dual channel version of the popular TL16C550B asynchronous communications element (ACE). The device serves two serial input/output interfaces simultaneously in microcomputer or microprocessor-based systems. Each channel performs serial-to-parallel conversion on data characters received from peripheral devices or modems and parallel-to-serial conversion on data characters

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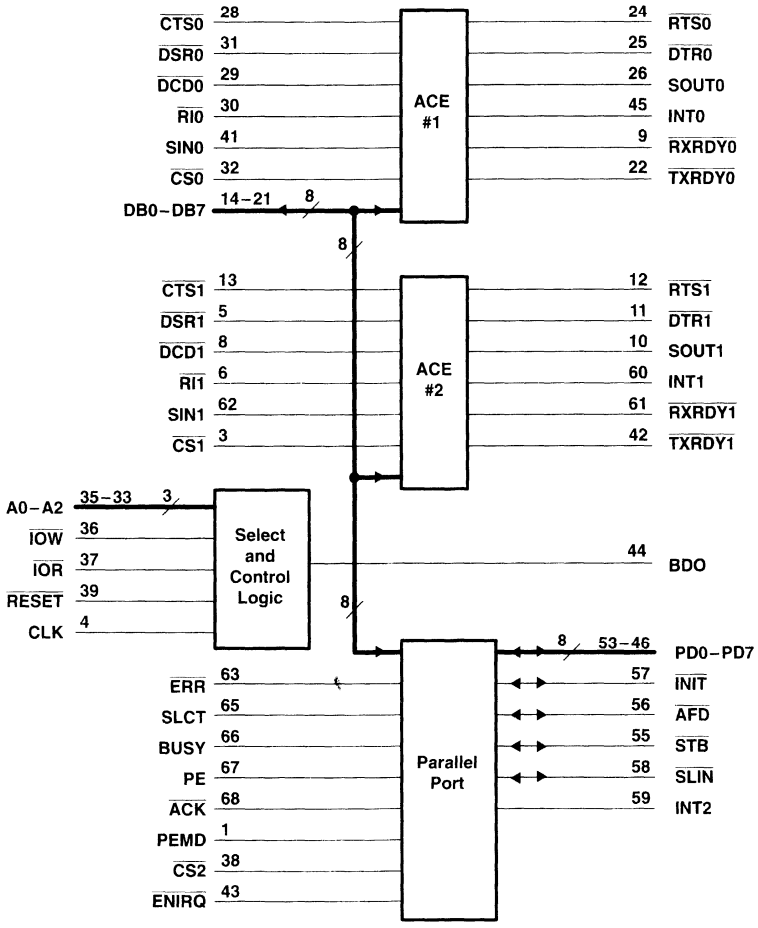
description (continued)

transmitted by the CPU. The complete status of each channel of the dual ACE can be read at any time during functional operation by the CPU. The information obtained includes the type and condition of the transfer operations being performed and the error conditions.

In addition to its dual communications interface capabilities, the TL16C552A provides the user with a bidirectional parallel data port that fully supports the parallel Centronics-type printer interface. The parallel port and the two serial ports provide IBM PC/AT-compatible computers with a single device to serve the three system ports. A programmable baud rate generator is included that can divide the timing reference clock input by a divisor between 1 and ($2^{16} - 1$).

The TL16C552A is available in a 68-pin plastic leaded chip-carrier (FN) package.

functional block diagram



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Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{ACK}$	68	I	Line printer acknowledge. $\overline{ACK}$ goes low to indicate a successful data transfer has taken place. $\overline{ACK}$ generates a printer port interrupt during its positive transition.
$\overline{AFD}$	56	I/O	Line printer autofeed. $\overline{AFD}$ is an open-drain line that provides the printer with an active-low signal when continuous form paper is to be autofed to the printer. $\overline{AFD}$ has an internal pullup resistor to V_{DD} of approximately 10 kΩ.
A0, A1, A2	35, 34, 33	I	Address. The address lines A0–A2 select the internal registers during CPU bus operations. See Table 2 for the decode of the serial channels and Table 13 for the decode of the parallel printer port.
BDO	44	O	Bus buffer. BDO is an active-high output that is asserted when either serial channel or the parallel port is read. BDO controls the system bus driver (74LS245).
BUSY	66	I	Line printer busy. BUSY is an input line from the printer that goes high when the printer is not ready to accept data.
CLK	4	I	Clock. CLK is the external clock input to the baud rate divisor of each ACE.
$\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$	32, 3, 38	I	Chip select. Each input acts as an enable for the write and read signals for serial channels 1 ($\overline{CS0}$) and 2 ($\overline{CS1}$). $\overline{CS2}$ enables the signals to the printer port.
$\overline{CTS0}$, $\overline{CTS1}$	28, 13	I	Clear to send. The logical state of each $\overline{CTSx}$ terminal is reflected in the CTS bit of the modem status register (CTS is bit 4 of the modem status register, written MSR4) of each ACE. A change of state in either $\overline{CTSx}$ terminal, since the previous reading of the associated modem status register, causes the setting of ΔCTS (MSR0) of each modem status register.
DB0 – DB7	14 – 21	I/O	Data bits DB0 – DB7. The data bus provides eight I/O lines with 3-state outputs for the transfer of data, control, and status information between the TL16C552A and the CPU. These lines are normally in the high-impedance state except during read operations. DB0 is the least significant bit (LSB) and is the first serial data bit to be received or transmitted.
$\overline{DCD0}$, $\overline{DCD1}$	29, 8	I	Data carrier detect. $\overline{DCDx}$ is a modem input. Its condition can be tested by the CPU by reading MSR7 (DCD) of the modem status registers. MSR3 (ΔDCD) of the modem status register indicates whether the $\overline{DCD}$ input has changed since the previous reading of the modem status register. $\overline{DCDx}$ has no affect on the receiver.
$\overline{DSR0}$, $\overline{DSR1}$	31, 5	I	Data set ready. The logical state of the $\overline{DSRx}$ terminals is reflected in MSR5 of its associated modem status register. ΔDSR (MSR1) indicates whether the associated $\overline{DSRx}$ terminal has changed state since the previous reading of the modem status register.
$\overline{DTR0}$, $\overline{DTR1}$	25, 11	O	Data terminal ready. Each $\overline{DTRx}$ output can be asserted low by setting MCR0, modem control register bit 0 of its associated ACE. $\overline{DTRx}$ is asserted high by clearing the DTR bit (MCR0) or whenever a reset occurs. When active (low), $\overline{DTRx}$ indicates that its ACE is ready to receive data.
$\overline{ENIRQ}$	43	I	Parallel port interrupt source mode selection. When $\overline{ENIRQ}$ is low, the AT mode of interrupts is enabled. In AT mode, the INT2 output is internally connected to the $\overline{ACK}$ input. When the $\overline{ENIRQ}$ output is tied high, the PS-2 mode of interrupt is enabled and the INT2 output is internally tied to the inverse of the $\overline{PRINT}$ bit in the printer status register. INT2 is latched high on the rising edge of $\overline{ACK}$. INT2 is held until the status register is read, which then resets the $\overline{PRINT}$ status bit and INT2.
$\overline{ERR}$	63	I	Line printer error. $\overline{ERR}$ is an input line from the printer. The printer reports an error by holding $\overline{ERR}$ low during the error condition.
GND	7, 27, 54		Ground (0 V). All terminals must be tied to GND for proper operation.
$\overline{INIT}$	57	I/O	Line printer initialize. $\overline{INIT}$ is an open-drain line that provides the printer with an active-low signal that allows the printer initialization routine to be started. $\overline{INIT}$ has an internal pullup resistor to V_{DD} of approximately 10 kΩ.
INT0, INT1	45, 60	O	External serial channel interrupt. Each serial channel interrupt 3-state output (enabled by bit 3 of the MCR) goes active (high) when one of the following interrupts has an active (high) condition and is enabled by the interrupt enable register of its associated channel: receiver error flag, received data available, transmitter holding register empty, and modem status. The interrupt is cleared on appropriate service. Upon reset, the interrupt output is in the high-impedance state.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
INT2	59	O	Printer port interrupt. INT2 is an active-high, 3-state output generated by the positive transition of $\overline{ACK}$. INT2 is enabled by bit 4 of the write control register. Upon reset, INT2 is in the high-impedance state. Its mode is also controlled by $\overline{ENIRQ}$.
$\overline{IOR}$	37	I	Input/output read strobe. $\overline{IOR}$ is an active-low input that enables the selected channel to output data to the data bus (DB0–DB7). The data output depends on the register selected by the address inputs A0, A1, A2, and chip select. Chip select 0 ($\overline{CS0}$) selects ACE #1, chip select 1 ($\overline{CS1}$) selects ACE #2, and chip select 2 ($\overline{CS2}$) selects the printer port.
$\overline{IOW}$	36	I	Input/output write strobe. $\overline{IOW}$ is an active-low input causing data from the data bus to be input to either ACE or to the parallel port. The destination depends on the register selected by the address inputs A0, A1, A2, and chip selects $\overline{CS0}$, $\overline{CS1}$, and $\overline{CS2}$.
PD0–PD7	53–46	I/O	Parallel data bits (0–7). PD0–PD7 provide a byte wide input or output port to the system.
PE	67	I	Line printer paper empty. PE is an input line from the printer that goes high when the printer runs out of paper.
PEMD	1	I	Printer enhancement mode. When low, PEMD enables the write data register to the PD0–PD7 lines. A high on this signal allows direction control of the PD0–PD7 port by the DIR bit in the control register. PEMD is usually tied low for the printer operation.
$\overline{RESET}$	39	I	Reset. When low, $\overline{RESET}$ forces the TL16C552A into an idle mode in which all serial data activities are suspended. The modem control register along with its associated outputs are cleared. The line status register is cleared except for the THRE and TEMT bits, which are set. All functions of the device remain in an idle state until programmed to resume serial data activities. $\overline{RESET}$ has a hysteresis level of typically 400 mV.
$\overline{RTS0}$, $\overline{RTS1}$	24, 12	O	Request to send. The $\overline{RTS}$ outputs are set low by setting the MCR1 of its UARTs modem control register. Both $\overline{RTS}$ terminals are asserted high by $\overline{RESET}$. A low on $\overline{RTS}$ indicates that its ACE has data ready to transmit. In half duplex operations, $\overline{RTS}$ controls the direction of the line.
$\overline{RXRDY0}$, $\overline{RXRDY1}$	9, 61	O	Receiver ready. Receiver direct memory access (DMA) signaling is also available through this output. One of two types of DMA signaling can be selected using FCR3 when operating in the FIFO mode. Only DMA mode 0 is allowed when operating in the TL16C450 mode. For signal transfer DMA (a transfer is made between CPU bus cycles), mode 0 is used. Multiple transfers that are made continuously until the receiver FIFO has been emptied are supported by mode 1. Mode 0. $\overline{RXRDY}$ is active (low) when in the FIFO mode (FCR0 = 1, FCR3 = 0) or when in the TL16C450 mode (FCR0 = 0) and the receiver FIFO or receiver holding register contain at least one character. When there are no more characters in the FIFO or holding register, $\overline{RXRDY}$ goes inactive (high). Mode 1. $\overline{RXRDY}$ goes active (low) in the FIFO mode (FCR0 = 1) when FCR3 = 1 and the time-out or trigger levels have been reached. $\overline{RXRDY}$ goes inactive (high) when the FIFO or holding register is empty.
$\overline{RI0}$, $\overline{RI1}$	30, 6	I	Ring indicator. The $\overline{RI}$ signal is a modem control input. Its condition is tested by reading MSR6 (RI) of each ACE. The modem status register output TERI (MSR2) indicates whether $\overline{RI}$ has changed from high to low since the previous reading of the modem status register.
SIN0, SIN1	41, 62	I	Serial data. SIN0 and SIN1 move information from the communication line or modem to the TL16C552A receiver circuits. A mark (set) is high and a space (cleared) is low. Data on serial data inputs is disabled when operating in the loop mode.
SLCT	65	I	Line printer select. SLCT is an input line from the line printer that goes high when the line printer is selected.
$\overline{SLIN}$	58	I/O	Line printer select. $\overline{SLIN}$ is an open-drain I/O that selects the printer when active (low). $\overline{SLIN}$ has an internal pullup resistor to V_{DD} of approximately 10 kΩ.
SOUT0, SOUT1	26, 10	O	Serial data outputs. These lines are the serial data outputs from the ACE transmitter circuitry. A mark is a set bit (high) and a space is a cleared bit 0 (low). Each SOUT is held in the mark condition when the transmitter is disabled ($\overline{RESET}$ is asserted low) the transmitter register is empty, or when in the loop mode.
$\overline{STB}$	55	I/O	Line printer strobe. $\overline{STB}$ is an open-drain line that provides communication between the TL16C552A and the printer. When $\overline{STB}$ is active (low), it provides the printer with a signal to latch the data currently on the parallel port. $\overline{STB}$ has an internal pullup resistor to V_{DD} of approximately 10 kΩ.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
TRI	2	I	3-state output control input. TRI controls the 3-state control of all I/O and output terminals. When TRI is asserted, all I/O and outputs are in the high-impedance state allowing board level testers to drive the outputs without overdriving internal buffers. This CMOS input is level sensitive and is pulled down with an internal resistor that is approximately 5 kΩ.
$\overline{\text{TXRDY0}}$ $\overline{\text{TXRDY1}}$	22 42	O	Transmitter ready. Two types of DMA signaling are available. Either can be selected using FCR3 when operating in the FIFO mode. Only DMA mode 0 is allowed when operating in the TL16C450 mode. Single-transfer DMA (a transfer is made between CPU bus cycles) is supported by mode 0. Multiple transfers that are made continuously until the transmitter FIFO has been filled are supported by mode 1. Mode 0. When in the FIFO mode (FCR0 = 1, FCR3 = 0) or in the TL16C450 mode (FCR0 = 0) and there are no characters in the transmitter holding register or transmitter FIFO, $\overline{\text{TXRDYx}}$ is active (low). Once $\overline{\text{TXRDYx}}$ is activated (low), it goes inactive after the first character is loaded into the holding register of the transmitter FIFO. Mode 1. $\overline{\text{TXRDYx}}$ goes active (low) when in the FIFO mode (FCR0 = 1) when FCR3 = 1 and there are no characters in the transmitter FIFO. When the transmitter FIFO is completely full, $\overline{\text{TXRDYx}}$ goes inactive (high).
V_{DD}	23, 40, 64		Power supply. The V_{DD} requirement is 5 V ±5%.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 1) ..... −0.5 V to V_{DD} + 0.3 V
Input voltage range, V_I ..... −0.5 V to 7 V
Output voltage range, V_O ..... −0.5 V to V_{DD} + 0.3 V
Continuous total power dissipation at (or below) 70°C ..... 500 mW
Operating free-air temperature range, T_A ..... −10°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage levels are with respect to GND.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.75	5	5.25	V
Clock high-level input voltage, $V_{IH(CLK)}$	2		V_{DD}	V
Clock low-level input voltage, $V_{IL(CLK)}$	−0.5		0.8	V
High-level input voltage, V_{IH}	2		V_{DD}	V
Low-level input voltage, V_{IL}	−0.5		0.8	V
Clock frequency, f_{clock}			16	MHz
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −0.4 mA for DB0–DB7, I_{OH} = −2 mA for PD0–PD7, I_{OH} = −0.4 mA for $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$, and $\overline{SLIN}$ (see Note 2), I_{OH} = −0.4 mA for all other outputs	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA for DB0–DB7, I_{OL} = 12 mA for PD0–PD7, I_{OL} = 10 mA for $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$, and $\overline{SLIN}$ (see Note 2), I_{OL} = 2 mA for all other outputs		0.4	V
I_I	Input current	V_{DD} = 5.25 V, All other terminals are floating		±10	µA
$I_{I(CLK)}$	Clock input current	V_I = 0 to 5.25 V		±10	µA
I_{OZ}	High-impedance output current	V_{DD} = 5.25 V, V_O = 0 with chip deselected, or V_O = 5.25 V with chip and write mode selected		±20	µA
I_{DD}	Supply current	V_{DD} = 5.25 V, No loads on outputs, SIN0, SIN1, $\overline{DSR0}$, $\overline{DSR1}$, $\overline{DCD0}$, $\overline{DCD1}$, $\overline{CTS0}$, $\overline{CTS1}$, $\overline{RI0}$ and $\overline{RI1}$ at 2 V, Other inputs at 0.8 V, Baud rate generator f_{clock} = 8 MHz, Baud rate = 56 kbit/s		50	mA

NOTE 2: These four terminals contain an internal pullup resistor to V_{DD} of approximately 10 kΩ.

clock timing requirements over recommended ranges of operating free-air temperature and supply voltage

		MIN	MAX	UNIT
t_{w1}	Pulse duration, CLK ↑ (external clock) (see Figure 1)	31		ns
t_{w2}	Pulse duration, CLK ↓ (external clock) (see Figure 1)	31		ns
t_{w3}	Pulse duration, master reset (see Figure 18)	1000		ns

read-cycle timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 4)

		MIN	MAX	UNIT
t_{w4}	Pulse duration, $\overline{IOR}$ ↓	80		ns
t_{su1}	Setup time, $\overline{CSx}$ valid before $\overline{IOR}$ ↓ (see Note 3)	15		ns
t_{su2}	Setup time, A2–A0 valid before $\overline{IOR}$ ↓ (see Note 3)	15		ns
t_{h1}	Hold time, A2–A0 valid after $\overline{IOR}$ ↑ (see Note 3)	20		ns
t_{h2}	Hold time, chip $\overline{CSx}$ after $\overline{IOR}$ ↑ (see Note 3)	20		ns
t_{d1}	Delay time, $t_{su2} + t_{w4} + t_{d2}$ (see Note 4)	175		ns
t_{d2}	Delay time, $\overline{IOR}$ ↑ to $\overline{IOR}$ ↓ or $\overline{IOW}$ ↓	80		ns

NOTES: 3. The internal address strobe is always active.
4. In the FIFO mode, t_{d1} = 425 ns (min) between reads of the receiver FIFO and the status registers (interrupt identification register and line status register).

write cycle timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 5)

		MIN	MAX	UNIT
t_{w5}	Pulse duration, $\overline{IOW}$ low	80		ns
t_{su4}	Setup time, $\overline{CSx}$ valid before $\overline{IOW}$ ↓ (see Note 3)	15		ns
t_{su5}	Setup time, A2–A0 valid before $\overline{IOW}$ ↓ (see Note 3)	15		ns
t_{su6}	Setup time, DB0–DB7 valid before $\overline{IOW}$ ↑	15		ns
t_{h3}	Hold time, A2–A0 valid after $\overline{IOW}$ ↑ (see Note 3)	20		ns
t_{h4}	Hold time, $\overline{CSx}$ valid after $\overline{IOW}$ ↑ (see Note 3)	20		ns
t_{h5}	Hold time, DB0–DB7 valid after $\overline{IOW}$ ↑	15		ns
t_{d3}	Delay time, $t_{su5} + t_{w5} + t_{d4}$	175		ns
t_{d4}	Delay time, $\overline{IOW}$ ↑ to $\overline{IOW}$ or $\overline{IOR}$ ↓	80		ns

NOTE 3: The internal address strobe is always active.

read cycle switching characteristics over recommended ranges of operating free-air temperature and supply voltage, C_L = 100 pF (see Note 5 and Figure 4)

	PARAMETER	MIN	MAX	UNIT
t_{pd1}	Propagation delay time from $\overline{IOR}$ ↓ to BDO ↑ or from $\overline{IOR}$ ↑ to BDO ↓		60	ns
t_{en}	Enable time from $\overline{IOR}$ ↓ to DB0–DB7 valid		60	ns
t_{dis}	Disable time from $\overline{IOR}$ ↑ to DB0–DB7 released	0	60	ns

NOTE 5: V_{OL} and V_{OH} (and the external loading) determine the charge and discharge time.

transmitter switching characteristics over recommended ranges of operating free-air temperature and supply voltage

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{d5}	Delay time, interrupt THRE† ↓ to SOUT ↓ at start	See Figure 6	8	24	RCLK cycles
t_{d6}	Delay time, SOUT ↓ at start to interrupt THRE ↑	See Note 6 and Figure 6	8	9	RCLK cycles
t_{d7}	Delay time, $\overline{IOW}$ (WR THR) ↑ to interrupt THRE ↑	See Note 6 and Figure 6	16	32	RCLK cycles
t_{d8}	Delay time, SOUT ↓ at start to $\overline{TXRDY}$ ↓	C_L = 100 pF, See Figures 7 and 8		8	RCLK cycles
t_{pd2}	Propagation delay time from $\overline{IOW}$ (WR THR) ↓ to interrupt THRE ↓	C_L = 100 pF, See Figure 6		140	ns
t_{pd4}	Propagation delay time from $\overline{IOR}$ (RD IIR) ↑ to interrupt THRE ↓	C_L = 100 pF, See Figure 6		140	ns
t_{pd5}	Propagation delay time from $\overline{IOW}$ (WR THR) ↑ to $\overline{TXRDY}$ ↑	C_L = 100 pF, See Figures 7 and 8		195	ns

† The acronym THRE is for transmitter holding register empty.
NOTE 6: If the transmitter interrupt delay is active, this delay is lengthened by one character time minus the last stop bit time.

receiver switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figures 9 through 13)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{d9}	Delay time from stop to INT ↑	See Note 7		1	RCLK cycle
t_{pd6}	Propagation delay time from RCLK ↑ to sample CLK ↑			100	ns
t_{pd7}	Propagation delay time from $\overline{IOR}$ (RD RBR/RD LSR) ↓ to reset interrupt ↓	C_L = 100 pF		150	ns
t_{pd8}	Propagation delay time from $\overline{IOR}$ (RD RBR) ↓ to $\overline{RXRDY}$ ↑			150	ns

NOTE 7: The receiver data available indicator, the overrun error indicator, the trigger level interrupts, and the active $\overline{RXRDY}$ indicator are delayed three RCLK cycles in the FIFO mode (FCR0 = 1). After the first byte has been received, status indicators (PE, FE, BI) are delayed three RCLK cycles. These indicators are updated immediately for any further bytes received after RD RBR goes active. There are eight RCLK cycle delays for trigger change level interrupts.

modem control switching characteristics over recommended ranges of operating free-air temperature and supply voltage, C_L = 100 pF (see Figure 14)

	PARAMETER	MIN	MAX	UNIT
t_{pd9}	Propagation delay time from $\overline{IOW}$ (WR MCR) ↑ to $\overline{RTS}$ ($\overline{DTR}$) ↓↑		100	ns
t_{pd10}	Propagation delay time from modem input ($\overline{CTS}$, $\overline{DSR}$) ↓↑ to interrupt ↑		170	ns
t_{pd11}	Propagation delay time from $\overline{IOR}$ (RD MSR) ↑ to interrupt ↓		140	ns
t_{pd12}	Propagation delay time from $\overline{RI}$ ↑ to interrupt ↑		170	ns

parallel port timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 15, 16, and 17)

		MIN	MAX	UNIT
t_{su7}	Setup time, data valid before $\overline{STB}$ ↓	1		µs
t_{h6}	Hold time, data valid after $\overline{STB}$ ↑	1		µs
t_{w6}	Pulse duration, $\overline{STB}$ ↓	1		µs
t_{d10}	Delay time, BUSY ↑ to $\overline{ACK}$ ↓	Defined by printer		
t_{d11}	Delay time, BUSY ↓ to $\overline{ACK}$ ↓	Defined by printer		
t_{w7}	Pulse duration, BUSY ↑	Defined by printer		
t_{w8}	Pulse duration, $\overline{ACK}$ ↓	Defined by printer		
t_{d12}	Delay time, BUSY ↑ after $\overline{STB}$ ↑	Defined by printer		
t_{d13}	Delay time, INT2 ↓ after $\overline{ACK}$ ↓ (see Note 8)		22	ns
t_{d14}	Delay time, INT2 ↑ after $\overline{ACK}$ ↑ (see Note 8)		20	ns
t_{d15}	Delay time, INT2 ↑ after $\overline{ACK}$ ↑ (see Note 8)		24	ns
t_{d16}	Delay time, INT2 ↓ after $\overline{IOR}$ ↑ (see Note 8)		25	ns

NOTE 8: t_{d13}–t_{d16} are all measured with a 15-pF load.

PARAMETER MEASUREMENT INFORMATION

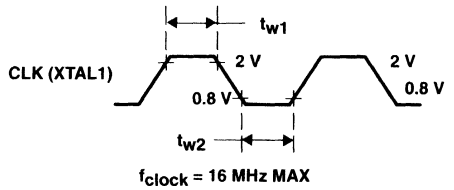
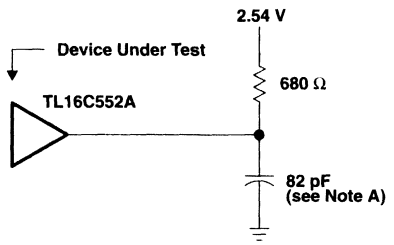


Figure 1. Clock Input (CLK) Voltage Waveform



NOTE A. Includes scope and jig capacitance.

Figure 2. Output Load Circuit

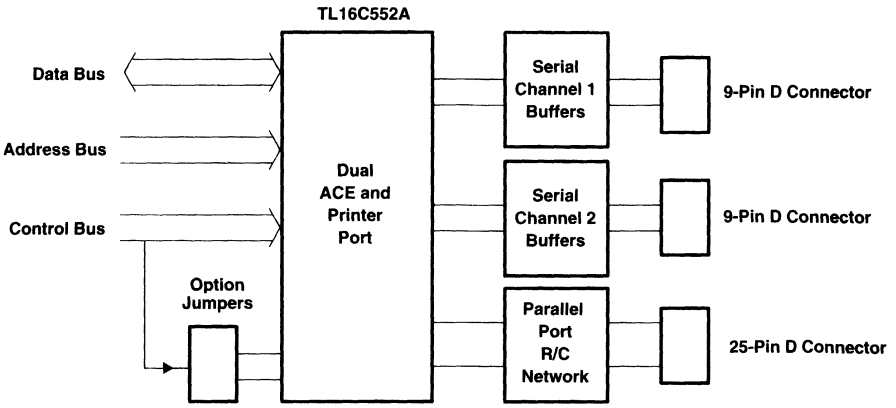


Figure 3. Basic Test Configuration

PARAMETER MEASUREMENT INFORMATION

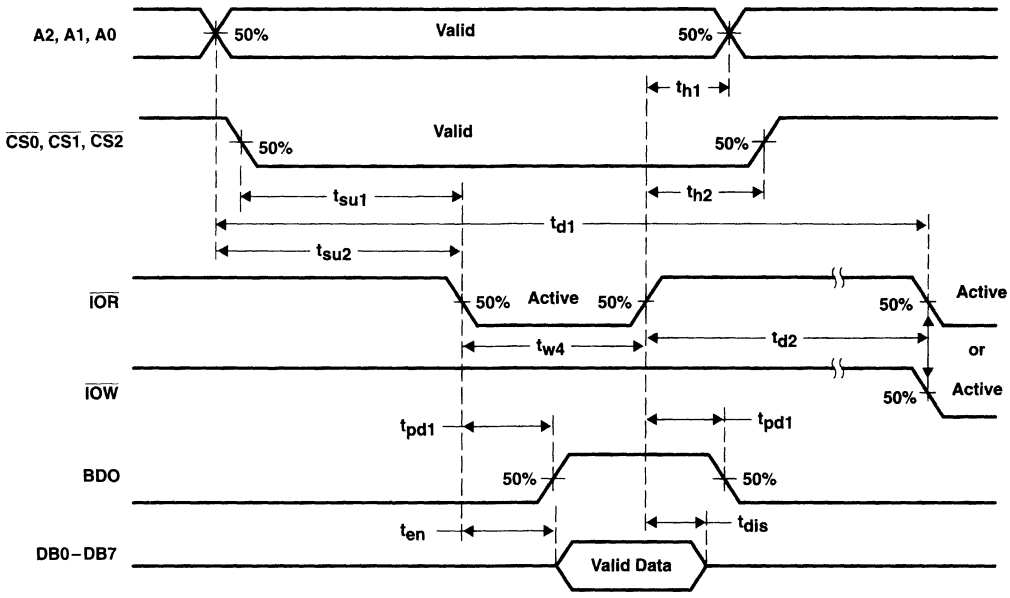


Figure 4. Read Cycle Timing Waveforms

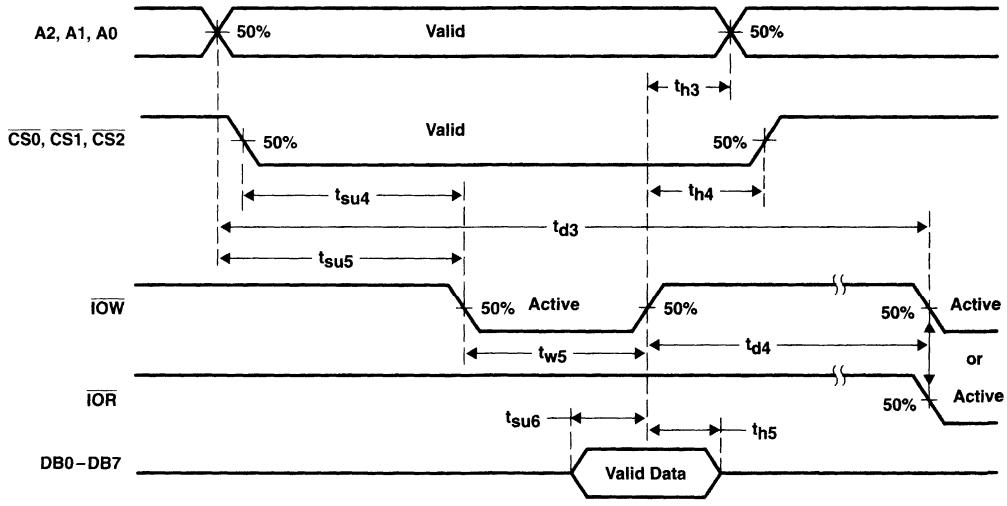


Figure 5. Write Cycle Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

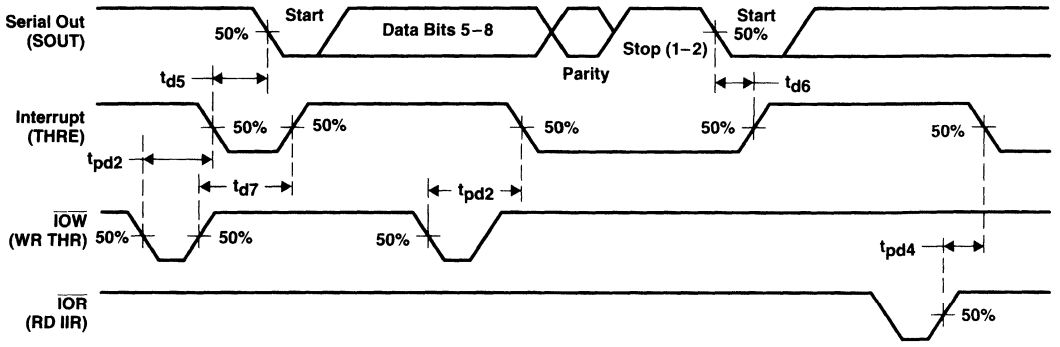


Figure 6. Transmitter Timing Waveforms

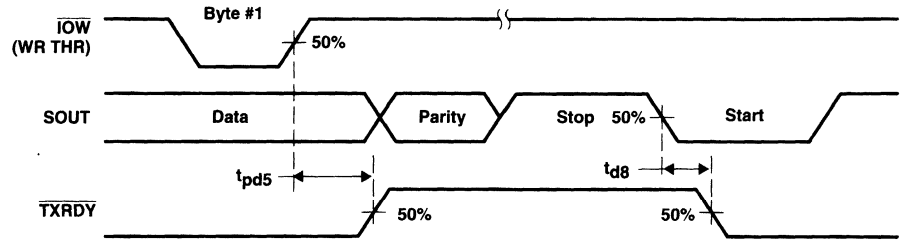


Figure 7. Transmitter Ready Mode 0 Timing Waveforms

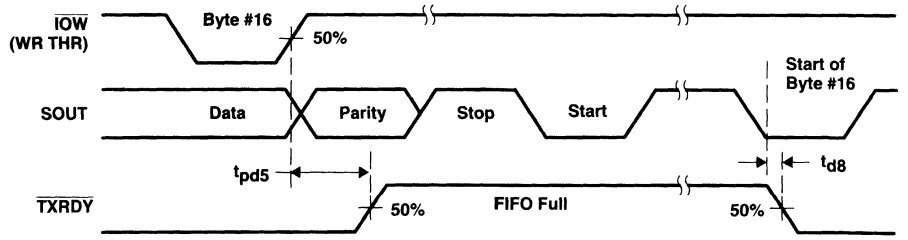


Figure 8. Transmitter Ready Mode 1 Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

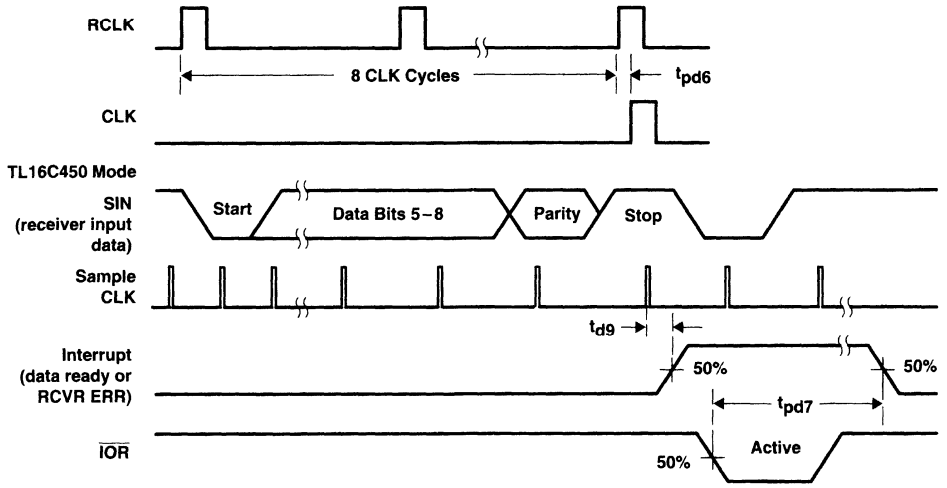


Figure 9. Receiver Timing Waveforms

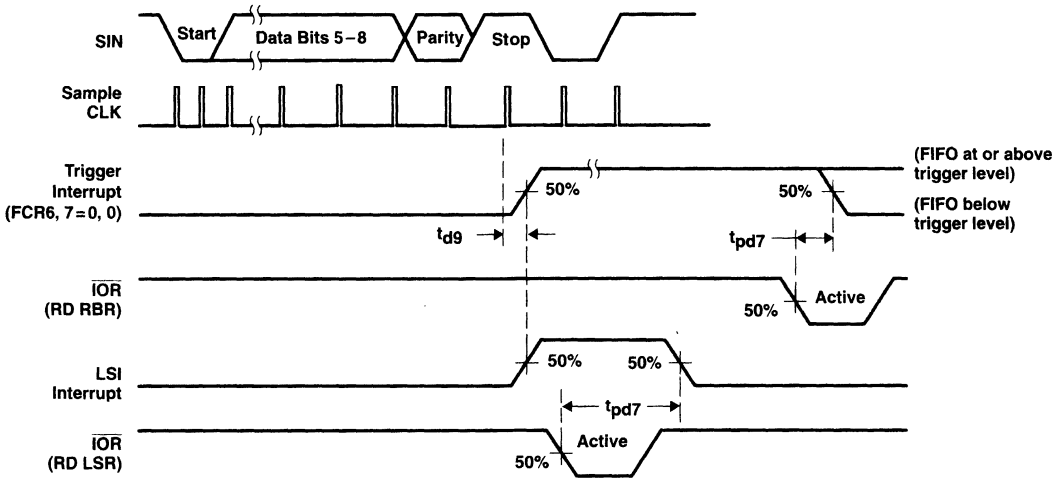


Figure 10. Receiver FIFO First Byte (Sets RDR) Waveforms

PARAMETER MEASUREMENT INFORMATION

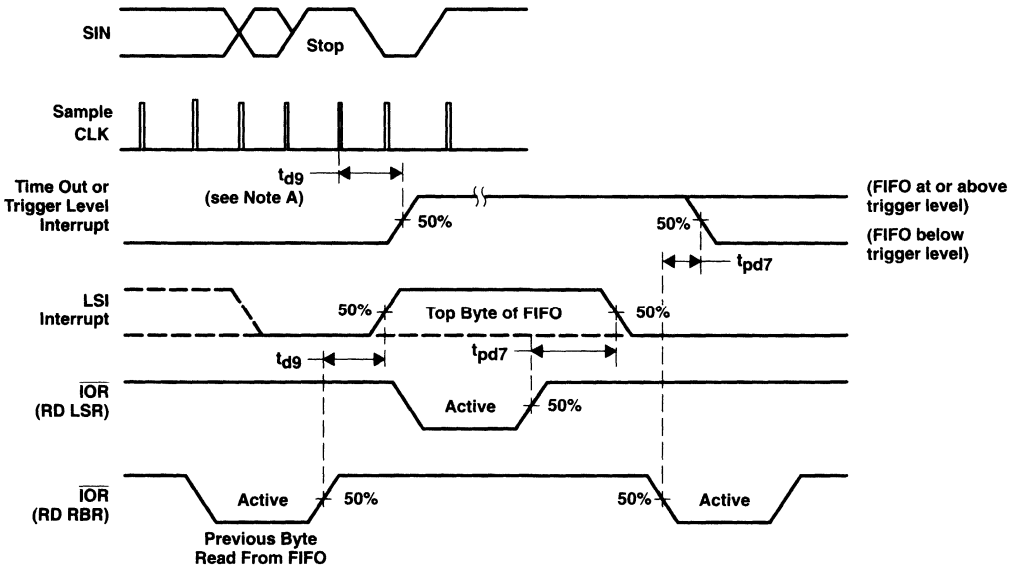


Figure 11. Receiver FIFO After First Byte (After RDR Set) Waveforms

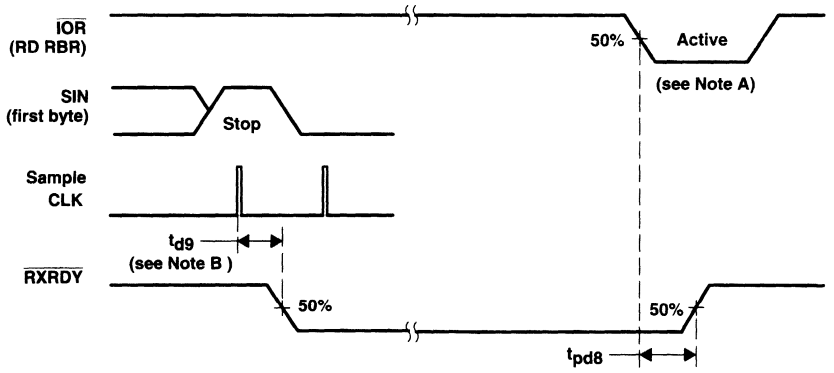
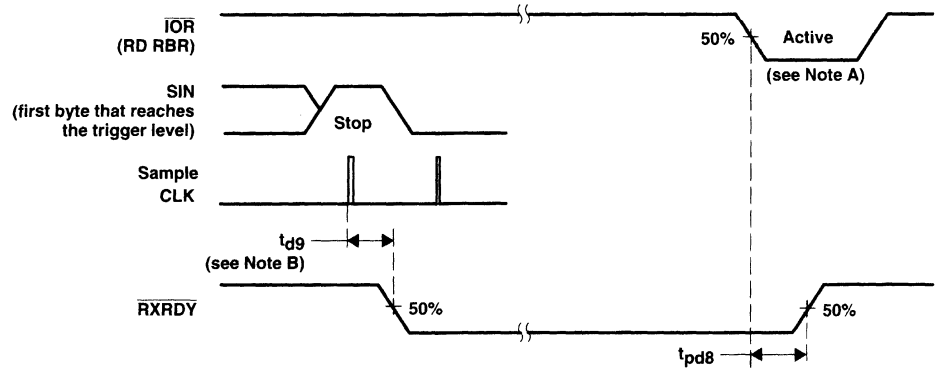


Figure 12. Receiver Ready Mode 0 Waveforms

NOTES: A. This is the reading of the last byte in the FIFO.
B. If FCR0 = 1, t_{d9} = 3 RCLK cycles. For a time-out interrupt, t_{d9} = 8 RCLK cycles.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. This is the reading of the last byte in the FIFO.
B. If FCR0–1, t_{d9} = 3 RCLK cycles. For a trigger change level interrupt, t_{d9} = 8 RCLK.

Figure 13. Receiver Ready Mode 1 Waveforms

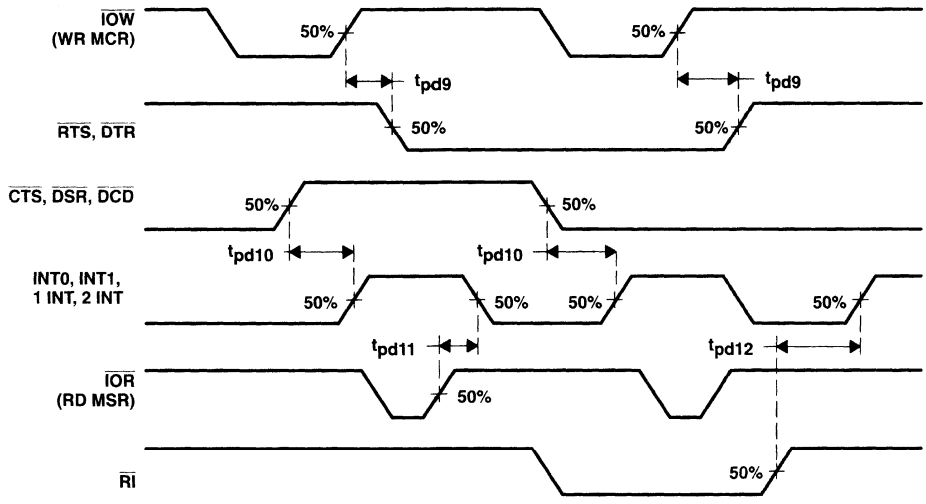


Figure 14. Modem Control Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

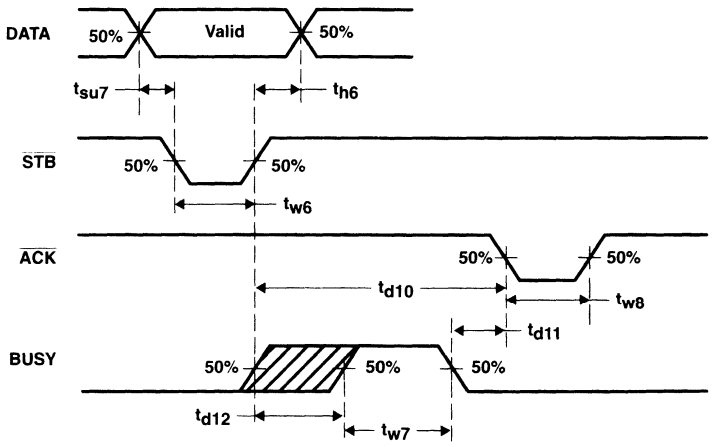
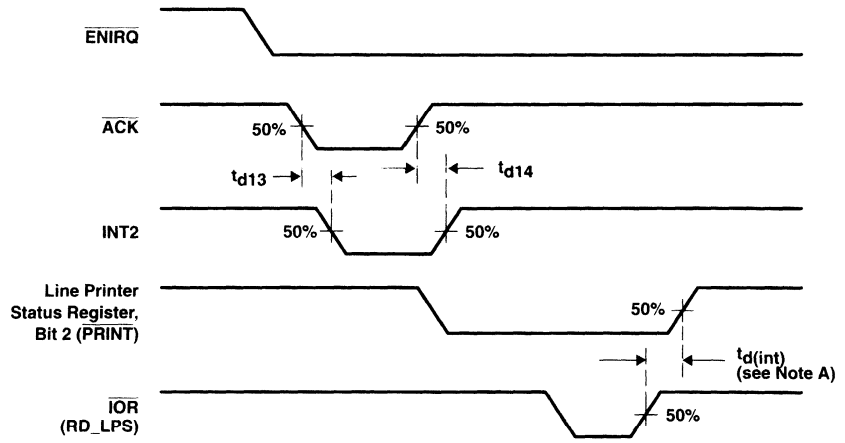


Figure 15. Parallel Port Timing Waveforms



NOTE A. A timing value is not provided for $t_{d(int)}$ in the tables since the line printer status register, bit 2 ($\overline{PRINT}$) is an internal signal.

Figure 16. Parallel Port AT Mode Timing (ENIRQ = Low) Waveforms

PARAMETER MEASUREMENT INFORMATION

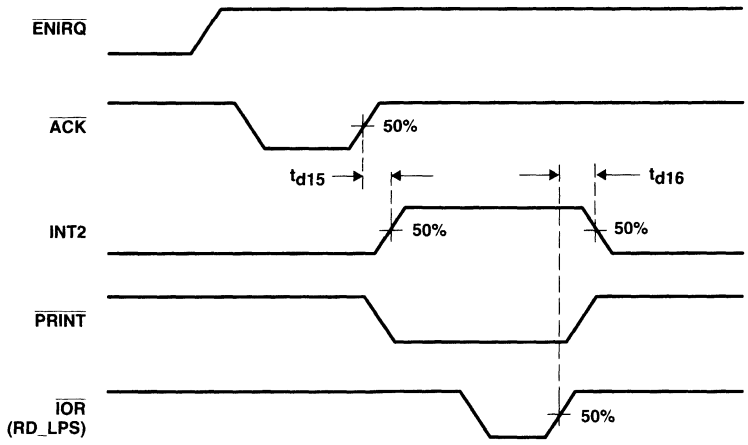


Figure 17. Parallel Port PS/2 Mode Timing (ENIRQ = High) Waveforms

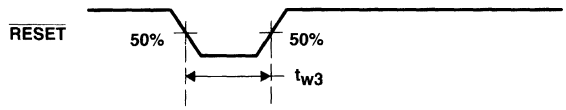


Figure 18. RESET Voltage Waveform

PRINCIPLES OF OPERATION

Three types of information are stored in the internal registers used in the ACE: control, status, and data. Mnemonic abbreviations for the internal registers are shown in Table 1.

Table 1. Internal Register Types With Mnemonics

CONTROL	MNEMONIC	STATUS	MNEMONIC	DATA	MNEMONIC
Line control register	LCR	Line status register	LSR	Receiver buffer register	RBR
FIFO control register	FCR	Modem status register	MSR	Transmitter holding register	THR
Modem control register	MCR				
Divisor latch LSB	DLL				
Divisor latch MSB	DLM				
Interrupt enable register	IER				

The address, read, and write inputs are used with the divisor latch access bit (DLAB) in the line control register (bit 7) to select the register to be written or read (see Table 2). Individual bits within the registers are referred to by the register mnemonic and the bit number in parenthesis. As an example, LCR7 refers to line control register bit 7.

The transmitter buffer register and receiver buffer register are data registers that hold from five to eight bits of data. If less than eight data bits are transmitted, data is right justified to the LSB. Bit 0 of a data word is always the first serial data bit received and transmitted. The ACE data registers are double buffered (TL16C450 mode) or FIFO buffered (FIFO mode) so that read and write operations can be performed when the ACE is performing the parallel-to-serial or serial-to-parallel conversion.

Table 2. Register Selection†

DLAB	A2	A1	A0	MNEMONIC	REGISTER
L	L	L	L	RBR	Receiver buffer register (read only)
L	L	L	L	THR	Transmitter holding register (write only)
L	L	L	H	IER	Interrupt enable register
X	L	H	L	IIR	Interrupt identification register (read only)
X	L	H	L	FCR	FIFO control register (write only)
X	L	H	H	LCR	Line control register
X	H	L	L	MCR	Modem control register
X	H	L	H	LSR	Line status register
X	H	H	L	MSR	Modem status register
X	H	H	H	SCR	Scratch pad register
H	L	L	L	DLL	LSB divisor latch
H	L	L	H	DLM	MSB divisor latch

† The serial channel is accessed when either $\overline{CS0}$ or $\overline{CS1}$ is low.
X = irrelevant, L = low level, H = high level

PRINCIPLES OF OPERATION

accessible registers

The system programmer, using the CPU, has access to and control over any of the ACE registers that are summarized in Table 1. These registers control ACE operations, receive data, and transmit data. Descriptions of these registers follow Table 3.

Table 3. Summary of Accessible Registers

ADDRESS	REGISTER MNEMONIC	REGISTER BIT NUMBER							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	RBR (read only)	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)
0	THR (write only)	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
0†	DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1†	DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
1	IER	0	0	0	0	(EDSSI) Enable modem status interrupt	(ERLSI) Enable receiver line status interrupt	(ETBEI) Enable transmitter holding register empty interrupt	(ERBFI) Enable received data available interrupt
2	FCR (write only)	Receiver Trigger (MSB)	Receiver Trigger (LSB)	Reserved	Reserved	DMA mode select	Transmitter FIFO reset	Receiver FIFO reset	FIFO Enable
2	IIR (read only)	FIFOs Enabled‡	FIFOs Enabled‡	0	0	Interrupt ID Bit 3‡	Interrupt ID Bit 2	Interrupt ID Bit 1	0 If interrupt pending
3	LCR	(DLAB) Divisor latch access bit	Set break	Stick parity	(EPS) Even parity select	(PEN) Parity enable	(STB) Number of stop bits	(WLSB1) Word length select bit 1	(WLSB0) Word length select bit 0
4	MCR	0	0	0	Loop	OUT2 Enable external interrupt (INT0 or INT1)	OUT1 (an unused internal signal)	(RTS) Request to send	(DTR) Data terminal ready
5	LSR	Error in receiver FIFO‡	(TEMT) Transmitter empty	(THRE) Transmitter holding register empty	(BI) Break interrupt	(FE) Framing error	(PE) Parity error	(OE) Overrun error	(DR) Data ready
6	MSR	(DCD) Data carrier detect	(RI) Ring indicator	(DSR) Data set ready	(CTS) Clear to send	(ΔDCD) Delta data carrier detect	(TERI) Trailing edge ring indicator	(ΔDSR) Delta data set ready	(ΔCTS) Delta clear to send
7	SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

† DLAB = 1
‡ These bits are always 0 when FIFOs are disabled.

PRINCIPLES OF OPERATION

FIFO control register (FCR)

This write-only register is at the same location as the IIR. It enables and clears the FIFOs, sets the trigger level of the receiver FIFO, and selects the type of DMA signaling.

- Bit 0: FCR0 enables both the transmitter and receiver FIFOs. All bytes in both FIFOs can be cleared by resetting FCR0. Data is cleared automatically from the FIFOs when changing from the FIFO mode to the TL16C450 mode and vice versa. Programming of other FCR bits is enabled by setting FCR0.
- Bit 1: FCR1 = 1 clears all bytes in the receiver FIFO and resets the counter. This does not clear the shift register.
- Bit 2: FCR2 = 1 clears all bytes in the transmitter FIFO and resets the counter. This does not clear the shift register.
- Bit 3: FCR3 = 1 changes the $\overline{\text{RXRDY}}$ and $\overline{\text{TXRDY}}$ terminals from mode 0 to mode 1 if FCR0 = 1.
- Bits 4 and 5: FCR4 and FCR5 are reserved for future use.
- Bits 6 and 7: FCR6 and FCR7 set the trigger level for the receiver FIFO interrupt as shown in Table 4.

Table 4. Trigger Level For the Receiver FIFO Interrupt

BIT		RECEIVER FIFO TRIGGER LEVEL (BYTES)
7	6	
0	0	01
0	1	04
1	0	08
1	1	14

FIFO interrupt mode operation

The following receiver status occurs when the receiver FIFO and receiver interrupts are enabled:

1. LSR0 is set when a character is transferred from the shift register to the receiver FIFO. When the FIFO is empty, it is cleared.
2. IIR = 06 receiver line status interrupt has higher priority than the received data available interrupt IIR = 04.
3. Receive data available interrupt is issued to the CPU when the programmed trigger level is reached by the FIFO. When the FIFO drops below its programmed trigger level, it is cleared.
4. IIR = 04 (receive data available indicator) also occurs when the FIFO reaches its trigger level. It is cleared when the FIFO drops below the programmed trigger level.

The following receiver FIFO character time-out status occurs when receiver FIFO and receiver interrupts are enabled.

PRINCIPLES OF OPERATION

FIFO interrupt mode operation (continued)

1. A FIFO timeout interrupt occurs when the following conditions exist:
   a. Minimum of one character in FIFO
   b. Last received serial character is longer than four continuous previous character times ago (if two stop bits are programmed, the second one is included in the time delay)
   c. The last CPU read of the FIFO is more than four continuous character times earlier. At 300 baud and 12-bit characters, the FIFO time-out interrupt causes a latency of 160 ms maximum from received character to interrupt issued.
2. By using the RCLK input for a clock signal, the character times can be calculated. The delay is proportional to the baud rate.
3. The time-out timer is reset after the CPU reads the receiver FIFO or after a new character is received when there has been no time-out interrupt.
4. A time-out interrupt is cleared and the timer is reset when the CPU reads a character from the receiver FIFO.

Transmitter interrupts occur as follows when the transmitter and transmitter FIFO interrupts are enabled (FCR0 = 1, IER = 1).

1. When the transmitter FIFO is empty, the transmitter holding register interrupt (IIR = 02) occurs. The interrupt is cleared when the transmitter holding register is written to or the IIR is read. One to sixteen characters can be written to the transmitter FIFO when servicing this interrupt.
2. The transmitter FIFO empty indicators are delayed one character time minus the last stop bit time when the following occurs:

   THRE = 1 and there is not a minimum of two bytes at the same time in transmitter FIFO since the last THRE = 1. The first transmitter interrupt after changing FCR0 is immediate assuming it is enabled.

Receiver FIFO trigger level and character time-out interrupts have the same priority as the received data available interrupt. The transmitter holding register empty interrupt has the same priority as the transmitter FIFO empty interrupt.

FIFO polled mode operation

Clearing IER0, IER1, IER2, IER3, or all with FCR0 = 1 puts the ACE into the FIFO polled mode. receiver and transmitter are controlled separately. Either one or both can be in the polled mode.

In the FIFO polled mode, there is no time-out condition indicated or trigger level reached. However, the receiver and transmitter FIFOs still have the capability of holding characters. The LSR must be read to determine the ACE status.

interrupt enable register (IER)

The IER independently enables the four serial channel interrupt sources that activate the interrupt (INT0 or INT1) output. All interrupts are disabled by clearing IER0 – IER3 of the IER. Interrupts are enabled by setting the appropriate bits of the IER. Disabling the interrupt system inhibits the IIR and the active (high) interrupt output. All other system functions operate in their normal manner, including the setting of the LSR and MSR. The contents of the IER shown in Table 3 are described in the following bulleted list.

- Bit 0: When set, IER0 enables the received data available interrupt and the time-out interrupts in the FIFO mode.

PRINCIPLES OF OPERATION

interrupt enable register (IER) (continued)

- Bit 1: When set, IER1 enables the transmitter holding register empty interrupt.
- Bit 2: When set, IER2 enables the receiver line status interrupt.
- Bit 3: When set, IER3 enables the modem status interrupt.
- Bits 4 – 7: IER4 – IER7 are always cleared.

interrupt identification register (IIR)

In order to minimize software overhead during data character transfers, the serial channel prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows:

- Priority 1 – Receiver line status (highest priority)
- Priority 2 – Receiver data ready or receiver character time out
- Priority 3 – Transmitter holding register empty
- Priority 4 – Modem status (lowest priority)

Information indicating that a prioritized interrupt is pending and the type of interrupt is stored in the IIR. The IIR indicates the highest priority interrupt pending. The contents of the IIR are indicated in Table 5.

Table 5. Interrupt Control Functions

INTERRUPT IDENTIFICATION REGISTER				INTERRUPT SET AND RESET FUNCTIONS			
BIT 3	BIT 2	BIT 1	BIT 0	PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET CONTROL
0	0	0	1	–	None	None	–
0	1	1	0	First	Receiver line status	OE, PE, FE, or BI	LSR read
0	1	0	0	Second	Received data available	Receiver data available or trigger level reached	RBR read until FIFO drops below the trigger level
1	1	0	0	Second	Character time-out indicator	No characters have been removed from or input to the receiver FIFO during the last four character times and there is at least one character in it during this time.	RBR read
0	0	1	0	Third	THRE	THRE	IIR read if THRE is the interrupt source or THR write
0	0	0	0	Fourth	Modem status	$\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$, or $\overline{DCD}$	MSR read

- Bit 0: IIR0 indicates whether an interrupt is pending. When IIR0 is cleared, an interrupt is pending.
- Bits 1 and 2: IIR1 and IIR2 identify the highest priority interrupt pending as indicated in Table 5.
- Bit 3: IIR is always cleared when in the TL16C450 mode. This bit is set along with bit 2 when in the FIFO mode and a trigger change level interrupt is pending.
- Bits 4 and 5: IIR4 and IIR5 are always cleared.
- Bits 6 and 7: IIR6 and IIR7 are set when FCR0 = 1.

PRINCIPLES OF OPERATION

line control register (LCR)

The format of the data character is controlled by the LCR. The LCR can be read. Its contents are described in the following bulleted list and shown in Figure 19.

- Bits 0 and 1: LCR0 and LCR1 are the word length select bits. The number of bits in each serial character is programmed as shown.
- Bit 2: LCR2 is the stop bit select bit. LCR2 specifies the number of stop bits in each transmitted character. The receiver always checks for one stop bit.
- Bit 3: LCR3 is the parity enable bit. When LCR3 is high, a parity bit between the last data word bit and stop bit is generated and checked.
- Bit 4: LCR4 is the even parity select bit. When set, LCR4 enables even parity.
- Bit 5: LCR5 is the stick parity bit. When parity is enabled (LCR3 = 1) and LCR5 = 1, this bit causes the transmission and reception of a parity bit to be in the opposite state from the value of LCR4. This forces parity to a known state and allows the receiver to check the parity bit in a known state.
- Bit 6: LCR6 is the break control bit. When this bit is set, the serial output (SOUT1/SOUT0) is forced to the spacing state (low). The break control bit acts only on the serial output and does not affect the transmitter logic. When the following sequence is used, no invalid characters are transmitted because of the break:

  Step 1: Load a zero byte in response to the transmitter holding register empty (THRE) status indicator.

  Step 2: Set the break in response to the next THRE status indicator.

  Step 3: Wait for the transmitter to be idle when transmitter empty status signal is set high (TEMT = 1); then clear the break when the normal transmission has to be restored.

- Bit 7: LCR7 is the divisor latch access bit (DLAB) bit. Bit 7 must be set to access the divisor latches DLL and DLM of the baud rate generator during a read or write operation. LCR7 must be cleared to access the receiver buffer register, the transmitter holding register, or the interrupt enable register.

PRINCIPLES OF OPERATION

line control register (LCR) (continued)

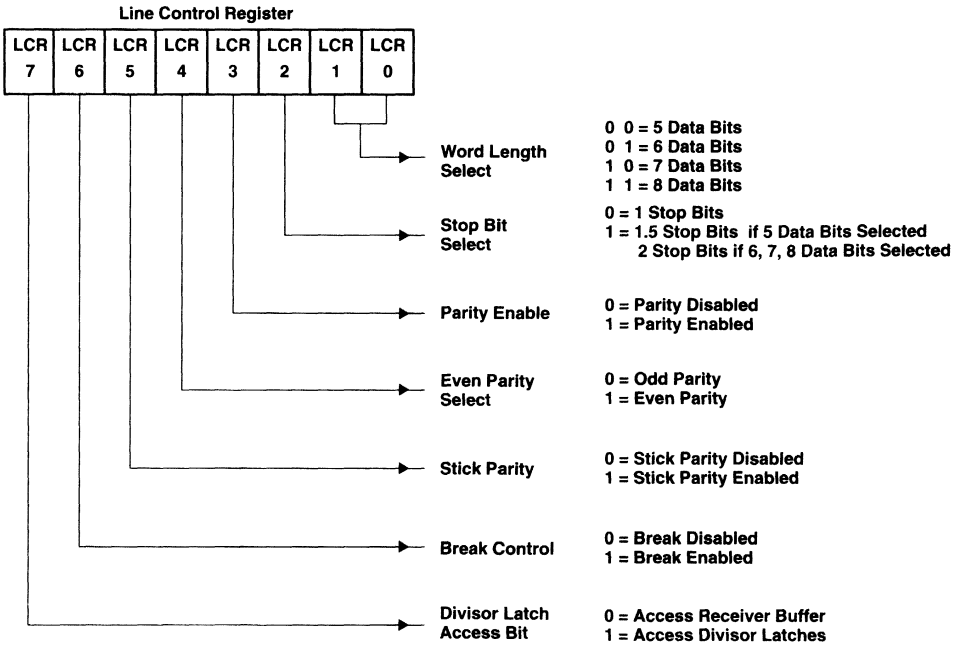


Figure 19. Line Control Register Contents

line printer port

The line printer port contains the functionality of the port included in the TL16C452 but offers a hardware programmable extended mode controlled by the printer enhancement mode (PEMD) terminal. This enhancement is the addition of a direction control bit and an interrupt status bit.

register 0 line printer data register (LPT)

The LPT port is either output only or bidirectional depending on the state of the extended mode terminal and data direction control bits.

Compatibility mode (PEMD = L)

Reads to the LPT data register return the last data that was written to the port. Write operations immediately output data to PD0–PD7.

Extended mode (PEMD = H)

Read operations return either the data last written to the LPT data register if the direction bit is set to write (low) or the data that is present on PD0–PD7 if the direction is set to read (high). Write operations to the LPT data register latch data into the output register; however, they only drive the LPT port when the direction bit is set to write (low).

PRINCIPLES OF OPERATION

line printer port (continued)

The Table 6 summarizes the configuration of the PD port based on the combinations of logic level on the PEMD terminal and value of the direction control bit (DIR).

Table 6. Extended Mode and Direction Control Bit Combinations

PEMD	DIR	PD0–PD7 FUNCTION
L	X	PC/AT mode – output
H	0	PS/2 mode – output
H	1	PS/2 mode – input

register 1 read line printer status register (LPS)

The LPS register is a read-only register that contains interrupt and printer status of the LPT connector terminals. In Table 7 (in the default column) are the values of each bit after reset in the case of the printer being disconnected from the port.

Table 7. LPS Register Bit Description

BIT	DESCRIPTION	DEFAULT
0	Reserved	1
1	Reserved	1
2	$\overline{\text{PRINT}}$	1
3	$\overline{\text{ERR}}$	†
4	SLCT	†
5	PE	†
6	$\overline{\text{ACK}}$	†
7	$\overline{\text{BSY}}$	†

† Outputs are dependent upon device inputs.

- Bits 0 and 1: These bits are reserved and are always set.
- Bit 2: $\overline{\text{PRINT}}$ is the printer interrupt status bit. When cleared, this bit indicates that the printer has acknowledged the previous transfer with an ACK handshake (if bit 4 of the control register is set). The bit is cleared on the active to inactive transition of the $\overline{\text{ACK}}$ signal. This bit is set after a read of the status port.
- Bit 3: $\overline{\text{ERR}}$ is the error status bit that corresponds to $\overline{\text{ERR}}$ terminal input.
- Bit 4: SLCT is the select status bit that corresponds to SLCT terminal input.
- Bit 5: PE is the paper empty status bit that corresponds to the PE terminal input.
- Bit 6: $\overline{\text{ACK}}$ is the acknowledge status bit that corresponds to $\overline{\text{ACK}}$ terminal input.
- Bit 7: $\overline{\text{BSY}}$ (active low) is the busy status bit that corresponds to BUSY terminal input (active high).

PRINCIPLES OF OPERATION

line printer port (continued)

register 2 line printer control register (LPC)

The LPC register is a read/write port that controls the PD0–PD7 direction and drive the printer control lines. Write operations set or clear these bits, while read operations return the state of the last write operation to this register. The bits in this register are defined in Table 8 and described in the following bulleted list.

Table 8. LPC Register Bit Description

BIT	DESCRIPTION
0	STB
1	AFD
2	$\overline{\text{INIT}}$
3	SLIN
4	INT2 EN
5	DIR
6	Reserved 0
7	Reserved 0

- Bit 0: STB is the printer strobe control bit. When STB is set, the $\overline{\text{STB}}$ terminal is asserted on the LPT interface. When STB is cleared, the signal is negated.
- Bit 1: AFD is the auto feed control bit. When AFD is set, the $\overline{\text{AFD}}$ terminal is asserted on the LPT interface. When AFD is cleared, the signal is negated.
- Bit 2: $\overline{\text{INIT}}$ is the initialize printer control bit. When $\overline{\text{INIT}}$ is set, the $\overline{\text{INIT}}$ terminal is negated. When $\overline{\text{INIT}}$ is cleared, the $\overline{\text{INIT}}$ terminal is asserted.
- Bit 3: SLIN is the select input control bit. When SLIN is set, the $\overline{\text{SLIN}}$ signal is asserted on the LPT interface. When SLIN is cleared, the signal is negated.
- Bit 4: INT2 EN is the interrupt request enable control bit. When INT2 EN is set, interrupts from the LPT port are enabled. When INT2 EN is cleared, interrupts are disabled and the INT2 terminal is placed in the high-impedance state.
- Bit 5: DIR is the direction control bit (only used when PEMD is high). When DIR is set, the output buffers in the PD port are disabled allowing data driven from external sources to be read from the PD port. When DIR is cleared, the PD port is in the output mode.
- Bits 6 and 7: These bits are reserved and always cleared.

PRINCIPLES OF OPERATION

line status register (LSR)

The LSR is a single register that provides status indicators. The LSR shown in Table 9 is described in the following bulleted list.

Table 9. Line Status Register Bits

LSR BITS	1	0
LSR0 data ready (DR)	Ready	Not ready
LSR1 overrun error (OE)	Error	No error
LSR2 parity error (PE)	Error	No error
LSR3 framing error (FE)	Error	No error
LSR4 break interrupt (BI)	Break	No break
LSR5 transmitter holding register empty (THRE)	Empty	Not empty
LSR6 transmitter empty (TEMT)	Empty	Not empty
LSR7 receiver FIFO error	Error in FIFO	No error in FIFO

- Bit 0: LSR0 is the data ready (DR) bit. Data ready is set when an incoming character is received and transferred into the receiver buffer register or the FIFO. LSR0 is cleared by a CPU read of the data in the receiver buffer register or the FIFO.
- Bit 1: LSR1 is the overrun error (OE) bit. Overrun error indicates that data in the receiver buffer register is not read by the CPU before the next character is transferred into the receiver buffer register overwriting the previous character. The OE indicator is cleared whenever the CPU reads the contents of the LSR. An overrun error occurs in the FIFO mode after the FIFO is full and the next character is completely received. The overrun error is detected by the CPU on the first LSR read after it happens. The character in the shift register is not transferred to the FIFO, but it is overwritten.
- Bit 2: LSR2 is the parity error (PE) bit. Parity error indicates that the received data character does not have the correct parity as selected by LCR3 and LCR4. The PE bit is set upon detection of a parity error and is cleared when the CPU reads the contents of the LSR. In the FIFO mode, the parity error is associated with a particular character in the FIFO. LSR2 reflects the error when the character is at the top of the FIFO.
- Bit 3: LSR3 is the framing error (FE) bit. Framing error indicates that the received character does not have a valid stop bit. LSR3 is set when the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE indicator is cleared when the CPU reads the contents of the LSR. In the FIFO mode, the framing error is associated with a particular character in the FIFO. LSR3 reflects the error when the character is at the top of the FIFO.
- Bit 4: LSR4 is the break interrupt (BI) bit. Break interrupt is set when the received data input is held in the spacing (low) state for longer than a full-word transmission time (start bit + data bits + parity + stop bits). The BI indicator is cleared when the CPU reads the contents of the LSR. In the FIFO mode, this is associated with a particular character in the FIFO. LSR4 reflects the BI when the break character is at the top of the FIFO. The error is detected by the CPU when its associated character is at the top of the FIFO during the first LSR read. Only one zero character is loaded into the FIFO when BI occurs.

LSR1 – LSR4 are the error conditions that produce a receiver line status interrupt [priority 1 interrupt in the interrupt identification register (IIR)] when any of the conditions are detected. This interrupt is enabled by setting IER2 in the interrupt enable register.

PRINCIPLES OF OPERATION

line status register (LSR) (continued)

- Bit 5: LSR5 is the transmitter holding register empty (THRE) bit. THRE indicates that the ACE is ready to accept a new character for transmission. The THRE bit is set when a character is transferred from the transmitter holding register into the transmitter shift register. LSR5 is cleared by the loading of the transmitter holding register by the CPU. LSR5 is not cleared by a CPU read of the LSR. In the FIFO mode when the transmitter FIFO is empty, this bit is set. It is cleared when one byte is written to the transmitter FIFO. When the THRE interrupt is enabled by IER1, THRE causes a priority 3 interrupt in the IIR. When THRE is the interrupt source indicated in IIR, INTRPT is cleared by a read of the IIR.
- Bit 6: LSR6 is the transmitter empty (TEMT) bit. TEMT is set when the transmitter holding register (THR) and the transmitter shift register (TSR) are both empty. LSR6 is cleared when a character is loaded into the THR and remains low until the character is transferred out of SOUT. TEMT is not cleared by a CPU read of the LSR. In the FIFO mode, when both the transmitter FIFO and shift register are empty, this bit is set.
- Bit 7: LSR7 is the receiver FIFO error bit. The LSR7 bit is always cleared in the TL16C450 mode. In FIFO mode, it is set when at least one of the following data errors is in the FIFO: parity error, framing error, or break interrupt indicator. It is cleared when the CPU reads the LSR if there are no subsequent errors in the FIFO.

NOTE

The LSR may be written. However, this function is intended only for factory test. It should be considered as read only by applications software.

master reset

After power up, the ACE $\overline{\text{RESET}}$ input should be held low for one microsecond to reset the ACE circuits to an idle mode until initialization. A low on $\overline{\text{RESET}}$ causes the following:

1. It initializes the transmitter and receiver clock counters.
2. It clears the LSR except for transmitter shift register empty (TEMT) and transmit holding register empty (THRE), which are set. The MCR is also cleared. All of the discrete lines, memory elements, and miscellaneous logic associated with these register bits are also cleared or turned off. The LCR, divisor latches, receiver buffer register, and transmitter buffer register are not effected.

Following the removal of the reset condition ($\overline{\text{RESET}}$ high), the ACE remains in the idle mode until programmed. A hardware reset of the ACE sets the THRE and TEMT status bit in the LSR. When interrupts are subsequently enabled, an interrupt occurs due to THRE. A summary of the effect of a reset on the ACE is given in Table 10.

PRINCIPLES OF OPERATION

master reset (continued)

Table 10. $\overline{\text{RESET}}$ Affects on Registers and Signals

REGISTER/SIGNAL	RESET CONTROL	RESET
Interrupt enable register	Reset	All bits low (0–3 forced and 4–7 permanent)
Interrupt identification register	Reset	Bit 0 is high, bits 1, 2, 3, 6, and 7 are low, and bits 4–5 are permanently low.
Line control register	Reset	All bits low
Modem control register	Reset	All bits low (5–7 permanent)
FIFO control register	Reset	All bits low
Line status register	Reset	All bits are low, except bits 5 and 6 are high.
Modem status register	Reset	Bits 0–3 low, bits 4–7 input signal
SOUT	Reset	High
Interrupt (receiver errs)	Read LSR/Reset	Low
Interrupt (receiver data ready)	Read RBR/Reset	Low
Interrupt (THRE)	Read IIR/Write THR/Reset	Low
Interrupt (modem status changes)	Read MSR/Reset	Low
$\overline{\text{OUT2}}$	Reset	High
$\overline{\text{RTS}}$	Reset	High
$\overline{\text{DTR}}$	Reset	High
$\overline{\text{OUT1}}$	Reset	High

modem control register (MCR)

The MCR controls the interface with the modem or data set as described in Figure 20. MCR can be written and read. The $\overline{\text{RTS}}$ and $\overline{\text{DTR}}$ outputs are directly controlled by their control bits in this register. A high input asserts a low signal (active) at the output terminals. The MCR bits are shown in the following bulleted list.

- Bit 0: When MCR0 is set, the $\overline{\text{DTR}}$ output is forced low. When MCR0 is cleared, the $\overline{\text{DTR}}$ output is forced high. The $\overline{\text{DTR}}$ output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.
- Bit 1: When MCR1 is set, the $\overline{\text{RTS}}$ output is forced low. When MCR1 is cleared, the $\overline{\text{RTS}}$ output is forced high. The $\overline{\text{RTS}}$ output of the serial channel can be input into an inverting line driver to obtain the proper polarity input at the modem or data set.
- Bit 2: MCR2 has no affect on operation.
- Bit 3: When MCR3 is set, the external serial channel interrupt is enabled.
- Bit 4: MCR4 provides a local loopback feature for diagnostic testing of the channel. When MCR4 is set, SOUT is asserted to the marking (high) state and SIN is disconnected. The output of the transmitter shift register is looped back into the receiver shift register input. The four modem control inputs ($\overline{\text{CTS}}$, $\overline{\text{DSR}}$, $\overline{\text{DCD}}$, and $\overline{\text{RI}}$) are disconnected. The modem control outputs ($\overline{\text{DTR}}$, $\overline{\text{RTS}}$, $\overline{\text{OUT1}}$, and $\overline{\text{OUT2}}$) are internally connected to the four modem control inputs. The modem control output terminals are forced to their inactive (high) state on the TL16C552A. In the diagnostic mode, data transmitted is immediately received. This allows the processor to verify the transmit and receive data paths of the selected serial channel. Interrupt control is fully operational; however, interrupts are generated by controlling the lower four MCR bits internally. Interrupts are not generated by activity on the external terminals represented by those four bits.

PRINCIPLES OF OPERATION

modem control register (MCR) (continued)

- Bits 5 – 7: MCR5 – MCR7 are permanently cleared.

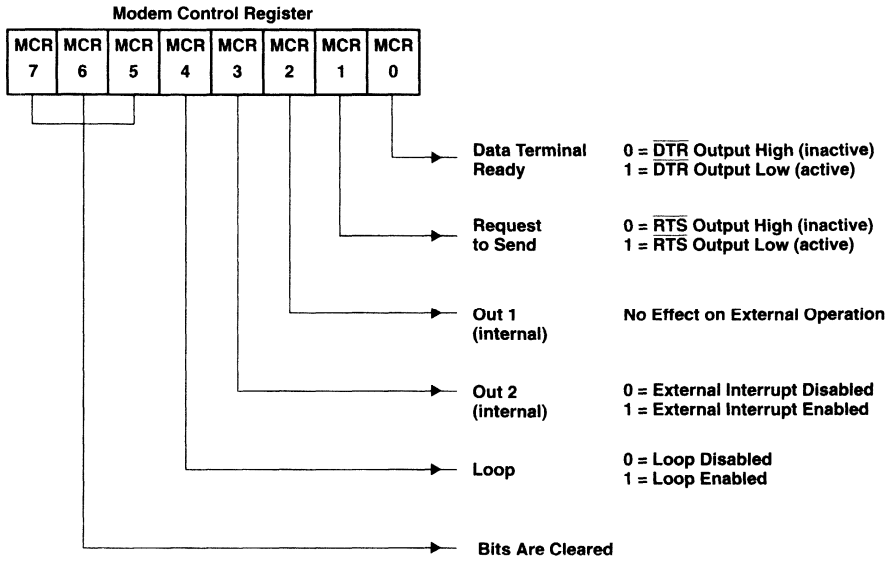


Figure 20. Modem Control Register Contents

modem status register (MSR)

The MSR provides the CPU with status of the modem input lines from the modem or peripheral devices. The MSR allows the CPU to read the serial channel modem signal inputs by accessing the data bus interface of the ACE in addition to the current status of four bits of the MSR that indicate whether the modem inputs have changed since the last reading of the MSR. The delta status bits are set when a control input from the modem changes state and is cleared when the CPU reads the MSR.

The modem input lines are $\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$, and $\overline{DCD}$. MSR4 – MSR7 are status indicators of these lines. A status bit = 1 indicates the input is low. A status bit = 0 indicates that the input is high. When the modem status interrupt in the interrupt enable register is enabled (IER3), an interrupt is generated whenever MSR0 – MSR3 is set. The MSR is a priority 4 interrupt. The contents of the MSR are described in Table 11 and the following bulleted list.

PRINCIPLES OF OPERATION

modem status register (MSR) (continued)

Table 11. Modem Status Register Bits

MSR BIT	MNEMONIC	DESCRIPTION
MSR0	ΔCTS	Delta clear to send
MSR1	ΔDSR	Delta data set ready
MSR2	TERI	Trailing edge of ring indicator
MSR3	ΔDCD	Delta data carrier detect
MSR4	CTS	Clear to send
MSR5	DSR	Data set ready
MSR6	RI	Ring indicator
MSR7	DCD	Data carrier detect

- Bit 0: MSR0 is the delta clear-to-send (ΔCTS) bit. ΔCTS displays that the $\overline{CTS}$ input to the serial channel has changed states since it was last read by the CPU.
- Bit 1: MSR1 is the delta data set ready (ΔDSR) bit. ΔDSR indicates that the $\overline{DSR}$ input to the serial channel has changed states since the last time it was read by the CPU.
- Bit 2: MSR2 is the trailing edge of ring indicator (TERI) bit. TERI indicates that the $\overline{RI}$ input to the serial channel has changed states from low to high since the last time it was read by the CPU. High-to-low transitions on RI do not activate TERI.
- Bit 3: MSR3, delta data carrier detect (ΔDCD) bit. ΔDCD indicates that the $\overline{DCD}$ input to the serial channel has changed states since the last time it was read by the CPU.
- Bit 4: MSR4 is the clear-to-send (CTS) bit. CTS is the complement of the $\overline{CTS}$ input from the modem indicating to the serial channel that the modem is ready to receive data from SOUT. When the serial channel is in the loop mode (MCR4 = 1), MSR4 reflects the value of RTS in the MCR.
- Bit 5: MSR5, data set ready (DSR) bit. DSR is the complement of the $\overline{DSR}$ input from the modem to the serial channel that indicates that the modem is ready to provide received data to the serial channel receiver circuitry. When the channel is in the loop mode (MCR4 = 1), MSR5 reflects the value of DTR in the MCR.
- Bit 6: MSR6, ring indicator (RI) bit. RI is the complement of the $\overline{RI}$ input. When the channel is in the loop mode (MCR4 = 1), MSR6 reflects the value of $\overline{OUT1}$ in the MCR.
- Bit 7: MSR7, data carrier detect (DCD) bit. Data carrier detect indicates the status of the data carrier detect ($\overline{DCD}$) input. When the channel is in the loop mode (MCR4 = 1), MSR7 reflects the value of OUT2 in the MCR.

Reading the MSR clears the delta modem status indicators but has no affect on the other status bits. For LSR and MSR, the setting of status bits is inhibited during status register read operations. If a status condition is generated during a read $\overline{IOR}$ operation, the status bit is not set until the trailing edge of the read. If a status bit is set during a read operation and the same status condition occurs, that status bit is cleared at the trailing edge of the read instead of being set again. In the loop back mode, when modem status interrupts are enabled, the $\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$ and $\overline{DCD}$ input terminals are ignored; however, a modem status interrupt can still be generated by writing to MCR3–MCR0. Applications software should not write to the MSR.

PRINCIPLES OF OPERATION

parallel port registers

The TL16C552A parallel port can connect the device to a Centronics-style printer interface. When chip select 2 ($\overline{CS2}$) is low, the parallel port is selected. Table 13 shows the registers associated with this parallel port. The read or write function of the register is controlled by the state of the read ($\overline{IOR}$) and write ($\overline{IOW}$) terminals as shown. The read data register allows the microprocessor to read the information on the parallel bus.

The read status register allows the microprocessor to read the status of the printer in the six most significant bits. The status bits are printer busy ($\overline{BSY}$), acknowledge ($\overline{ACK}$) (a handshake function), paper empty (PE), printer selected ($\overline{SLCT}$), error ($\overline{ERR}$) and printer interrupt ($\overline{PRINT}$). The read control register allows the state of the control lines to be read. The write control register sets the state of the control lines. They are direction (DIR), interrupt enable (INT2 EN), select in ($\overline{SLIN}$), initialize the printer ($\overline{INIT}$), autofeed the paper ($\overline{AFD}$), and strobe ($\overline{STB}$), which informs the printer of the presence of a valid byte on the parallel bus. The write data register allows the microprocessor to write a byte to the parallel bus. The parallel port is completely compatible with the parallel port implementation used in the IBM serial parallel adaptor.

Table 12. Parallel Port Registers

REGISTER	REGISTER BITS							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Read data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Read status	$\overline{BSY}$	$\overline{ACK}$	PE	SLCT	$\overline{ERR}$	$\overline{PRINT}$	1	1
Read control	0	0	PEMD • DIR	INT2 EN	SLIN	$\overline{INIT}$	AFD	STB
Write data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Write control	0	0	DIR	INT2 EN	SLIN	$\overline{INIT}$	AFD	STB

Table 13. Parallel Port Register Select

CONTROL TERMINALS					REGISTER SELECTED
$\overline{IOR}$	$\overline{IOW}$	$\overline{CS2}$	A1	A0	
L	H	L	L	L	Read data
L	H	L	L	H	Read status
L	H	L	H	L	Read control
L	H	L	H	H	Invalid
H	L	L	L	L	Write data
H	L	L	L	H	Invalid
H	L	L	H	L	Write control
H	L	L	H	H	Invalid

programmable baud generator

The ACE serial channel contains a programmable baud rate generator (BRG) that divides the clock (dc to 8 MHz) by any divisor from 1 to ($2^{16}-1$). The output frequency of the baud generator is 16 x the data rate [divisor # = clock ÷ (baud rate x 16)] referred to in this document as RCLK. Two 8-bit divisor latch registers store the divisor in a 16-bit binary format. These divisor latch registers must be loaded during initialization. Upon loading either of the divisor latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load. The BRG can use any of three different popular frequencies to provide standard baud rates. These frequencies are 1.8432 MHz, 3.072 MHz, and 8 MHz. With these frequencies, standard bit rates from 50 to 512 kbps are available. Tables 14, 15, 16, and 17 illustrate the divisors needed to obtain standard rates using these three frequencies.

PRINCIPLES OF OPERATION

programmable baud generator (continued)

Table 14. Baud Rates Using a 1.8432-MHz Crystal

BAUD RATE DESIRED	DIVISOR (N) USED TO GENERATE 16x CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	–
75	1536	–
110	1047	0.026
134.5	857	0.058
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.690
2400	48	–
3600	32	–
4800	24	–
7200	16	–
9600	12	–
19200	6	–
38400	3	–
56000	2	2.860

Table 15. Baud Rates Using a 3.072-MHz Crystal

BAUD RATE DESIRED	DIVISOR (N) USED TO GENERATE 16x CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	–
75	2560	–
110	1745	0.026
134.5	1428	0.034
150	1280	–
300	640	–
600	320	–
1200	160	–
1800	107	0.312
2000	96	–
2400	80	–
3600	53	0.628
4800	40	–
7200	27	1.230
9600	20	–
19200	10	–
38400	5	–

PRINCIPLES OF OPERATION

programmable baud generator (continued)

Table 16. Baud Rates Using a 8-MHz Clock

BAUD RATE DESIRED	DIVISOR (N) USED TO GENERATE 16x CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	10000	–
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	3333	0.010
300	1667	0.020
600	833	0.040
1200	417	0.080
1800	277	0.080
2000	250	–
2400	208	0.160
3600	139	0.080
4800	104	0.160
7200	69	0.644
9600	52	0.160
19200	26	0.160
38400	13	0.160
56000	9	0.790
128000	4	2.344
256000	2	2.344
512000	1	2.400

Table 17. Baud Rates Using a 16-MHz Clock

BAUD RATE DESIRED	DIVISOR (N) USED TO GENERATE 16x CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	20000	0.00
75	13334	0.00
110	9090	0.01
134.5	7434	0.01
150	6666	0.01
300	3334	−0.02
600	1666	0.04
1200	834	−0.08
1800	554	0.28
2000	500	0.00
2400	416	0.16
3600	278	−0.08
4800	208	0.16
7200	138	0.64
9600	104	0.16
19200	52	0.16
38400	26	0.16
56000	18	−0.79
128000	8	−2.34
256000	4	−2.34
512000	2	−2.34
1000000	1	0.00

PRINCIPLES OF OPERATION

programming

The serial channel of the ACE is programmed by the control registers: LCR, IER, DLL, DLM, MCR, and FCR. These control words define the character length, number of stop bits, parity, baud rate, and modem interface.

While the control registers can be written in any order, the IER should be written last because it controls the interrupt enables. Once the serial channel is programmed and operational, these registers can be updated any time the ACE serial channel is not transmitting or receiving data.

receiver

Serial asynchronous data is input into SIN. The ACE continually searches for a high-to-low transition from the idle state. When the transition is detected, a counter is reset and counts the 16× clock to 7 1/2, which is the center of the start bit. The start bit is valid if SIN is still low. Verifying the start bits prevents the receiver from assembling a false data character due to a low going noise spike on the SIN input.

The LCR determines the number of data bits in a character (LCR0 and LCR1). When parity is used, LCR3 and the polarity of parity LCR4 is needed. Status for the receiver is provided in the LSR. When a full character is received, including parity and stop bits, the data received indicator in LSR0 is set high. The CPU reads the receiver buffer register, which clears LSR0. If the character is not read prior to a new character transfer from the RSR to the RBR, the overrun error status indicator is set in LSR1. If there is a parity error, the parity error is set in LSR2. If a stop bit is not detected, a framing error indicator is set in LSR3.

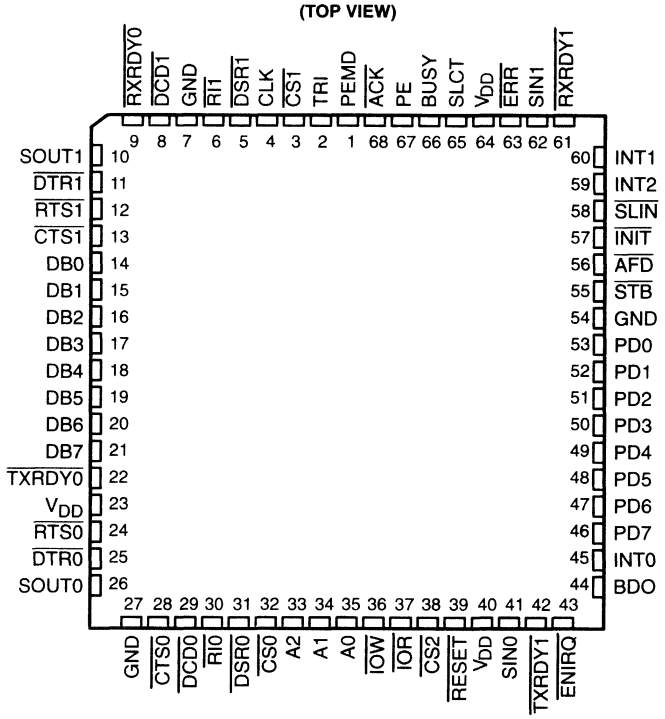
If the data into SIN is a symmetrical square wave, the center of the data cells occurs within ±3.125% of the actual center, providing an error margin of 46.875%. The start bit can begin as much as one 16× clock cycle prior to being detected.

scratchpad register

The scratchpad register is an 8-bit read/write register that has no affect on either channel in the ACE. It is intended to be used by the programmer to hold data temporarily.

- IBM PC/AT™ Compatible
- Two TL16C550 ACEs
- Enhanced Bidirectional Printer Port
- 16-Byte FIFOs Reduce CPU Interrupts
- Up to 16-MHz Clock Rate for up to 1-Mbaud Operation
- Transmit, Receive, Line Status, and Data Set Interrupts on Each Channel Independently Controlled
- Individual Modem Control Signals for Each Channel
- Programmable Serial Interface Characteristics for Each Channel:
  - 5-, 6-, 7-, or 8-Bit Characters
  - Even, Odd, or No Parity Bit Generation and Detection
  - 1-, 1-1/2-, or 2-Stop Bit Generation
- 3-State Outputs Provide TTL Drive for the Data and Control Bus on Each Channel
- Hardware and Software Compatible With TL16C452

FN PACKAGE
(TOP VIEW)



description

The TL16C552AI is an enhanced dual channel version of the popular TL16C550B asynchronous communications element (ACE). The device serves two serial input/output interfaces simultaneously in microcomputer or microprocessor-based systems. Each channel performs serial-to-parallel conversion on data characters received from peripheral devices or modems and parallel-to-serial conversion on data characters

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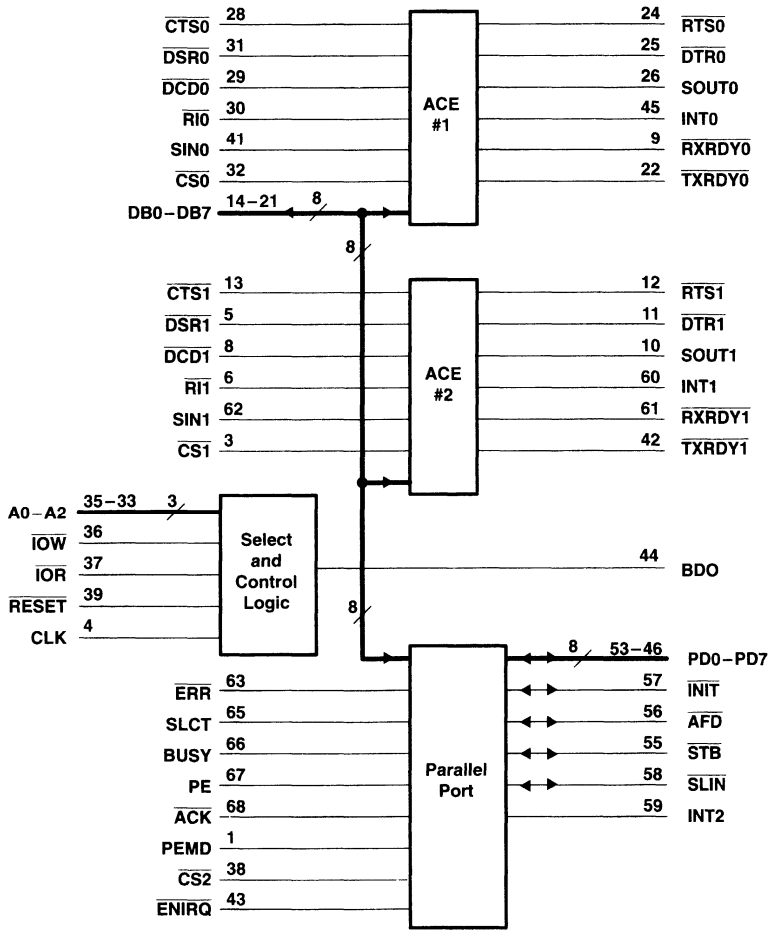
description (continued)

transmitted by the CPU. The complete status of each channel of the dual ACE can be read at any time during functional operation by the CPU. The information obtained includes the type and condition of the transfer operations being performed and the error conditions encountered.

In addition to its dual communications interface capabilities, the TL16C552AI provides the user with a bidirectional parallel data port that fully supports the parallel Centronics-type printer interface. The parallel port and the two serial ports provide IBM PC/AT-compatible computers with a single device to serve the three system ports. A programmable baud rate generator is included that can divide the timing reference clock input by a divisor between 1 and ($2^{16} - 1$).

The TL16C552AI is available in a 68-pin plastic-leaded chip-carrier (FN) package.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{ACK}$	68	I	Line printer acknowledge. $\overline{ACK}$ goes low to indicate a successful data transfer has taken place. $\overline{ACK}$ generates a printer port interrupt during its positive transition.
$\overline{AFD}$	56	I/O	Line printer autofeed. $\overline{AFD}$ is an open-drain line that provides the printer with an active-low signal when continuous form paper is to be autofed to the printer. $\overline{AFD}$ has an internal pullup resistor to V_{DD} of approximately 10 kΩ.
A0, A1, A2	35, 34, 33	I	Address. The address lines A0–A2 select the internal registers during CPU bus operations. See Table 2 for the decode of the serial channels and Table 13 for the decode of the parallel printer port.
BDO	44	O	Bus buffer. BDO is the active-high output and is asserted when either serial channel or the parallel port is read. BDO controls the system bus driver (74LS245).
BUSY	66	I	Line printer busy. BUSY is an input line from the printer that goes high when the printer is not ready to accept data.
CLK	4	I	Clock. CLK is the external clock input to the baud rate divisor of each ACE.
$\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$	32, 3, 38	I	Chip select. Each $\overline{CSx}$ input acts as an enable for the write and read signals for serial channels 1 ($\overline{CS0}$) and 2 ($\overline{CS1}$). $\overline{CS2}$ enables the signals to the printer port.
$\overline{CTS0}$, $\overline{CTS1}$	28, 13	I	Clear to send. The logical state of each $\overline{CTSx}$ terminal is reflected in the CTS bit of the modem status register (CTS is bit 4 of the modem status register, written as MSR4) of each ACE. A change of state in either $\overline{CTS}$ terminal since the previous reading of the associated MSR causes the setting of ΔCTS (MSR0) of each modem status register.
DB0 – DB7	14 – 21	I/O	Data bits DB0–DB7. The data bus provides eight I/O lines with 3-state outputs for the transfer of data, control, and status information between the TL16C552AI and the CPU. These lines are normally in the high-impedance state except during read operations. DB0 is the least significant bit (LSB) and is the first serial data bit to be received or transmitted.
$\overline{DCD0}$, $\overline{DCD1}$	29, 8	I	Data carrier detect. $\overline{DCD}$ is a modem input. Its condition can be tested by the CPU by reading MSR7 (DCD) of the modem status registers. MSR3 (ΔDCD) of the modem status register indicates whether $\overline{DCD}$ has changed states since the previous reading of the MSR. $\overline{DCD}$ has no effect on the receiver.
$\overline{DSR0}$, $\overline{DSR1}$	31, 5	I	Data set ready. The logical state of the $\overline{DSRx}$ terminals is reflected in MSR5 of its associated modem status register. ΔDSR (MSR1) indicates whether the associated $\overline{DSRx}$ terminal has changed states since the previous reading of the MSR.
$\overline{DTR0}$, $\overline{DTR1}$	25, 11	O	Data terminal ready. Each $\overline{DTRx}$ can be set low by setting MCR0, modem control register bit 0 of its associated ACE. $\overline{DTRx}$ is cleared (high) by clearing the DTR bit (MCR0) or whenever a reset occurs. When active (low), $\overline{DTRx}$ indicates that its ACE is ready to receive data.
$\overline{ENIRQ}$	43	I	Parallel port interrupt source mode selection. When $\overline{ENIRQ}$ is low, the AT mode of interrupts is enabled. In AT mode, INT2 is internally connected to $\overline{ACK}$. When $\overline{ENIRQ}$ is tied high, the PS-2 mode of interrupt is enabled and INT2 is internally tied to the inverse of the $\overline{PRINT}$ bit in the line printer status register. INT2 is latched high on the rising edge of $\overline{ACK}$. INT2 is held until the status register is read, which then clears the $\overline{PRINT}$ status bit and INT2.
$\overline{ERR}$	63	I	Line printer error. $\overline{ERR}$ is an input line from the printer. The printer reports an error by holding $\overline{ERR}$ low during the error condition.
GND	7, 27, 54		Ground (0 V). All terminals must be tied to GND for proper operation.
$\overline{INIT}$	57	I/O	Line printer initialize. $\overline{INIT}$ is an open-drain line that provides the printer with an active-low signal that allows the printer initialization routine to be started. $\overline{INIT}$ has an internal pullup resistor to V_{DD} of approximately 10 kΩ.
INT0, INT1	45, 60	O	External serial channel interrupt. Each serial channel interrupt 3-state output (enabled by bit 3 of the MCR) goes active (high) when one of the following interrupts has an active (high) condition and is enabled by the interrupt enable register of its associated channel: receiver error flag, received data available, transmitter holding register empty, and modem status. The interrupt is cleared on appropriate service. Upon reset, the interrupt output is in the high-impedance state.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
INT2	59	O	Printer port interrupt. INT2 is an active-high, 3-state output generated by the positive transition of $\overline{ACK}$. INT2 is enabled by bit 4 of the write control register. Upon reset, INT2 is in the high-impedance state. Its mode is also controlled by $\overline{ENIRQ}$.
$\overline{IOR}$	37	I	Input/output read strobe. $\overline{IOR}$ is an active-low input that enables the selected channel to output data to the data bus (DB0–DB7). The data output depends on the register selected by the address inputs A0, A1, A2, and chip select. Chip select 0 ($\overline{CS0}$) selects ACE #1, chip select 1 ($\overline{CS1}$) selects ACE #2, and chip select 2 ($\overline{CS2}$) selects the printer port.
$\overline{IOW}$	36	I	Input/output write strobe. $\overline{IOW}$ is an active-low input causing data from the data bus to be input to either ACE or to the parallel port. The destination depends on the register selected by the address inputs A0, A1, A2, and chip selects $\overline{CS0}$, $\overline{CS1}$, and $\overline{CS2}$.
PD0–PD7	53–46	I/O	Parallel data bits (0–7). PD0–PD7 provide a byte wide input or output port to the system.
PE	67	I	Line printer paper empty. PE is an input line from the printer that goes high when the printer runs out of paper.
PEMD	1	I	Printer enhancement mode. When low, PEMD enables the write data register to the PD0–PD7 lines. A high on PEMD allows direction control of the PD0–PD7 port by the DIR bit in the control register. PEMD is usually tied low for the printer operation.
$\overline{RESET}$	39	I	Reset. When low, $\overline{RESET}$ forces the TL16C552AI into an idle mode in which all serial data activities are suspended. The modem control register along with its associated outputs are cleared. The line status register is cleared except for the THRE and TEMT bits, which are set. All functions of the device remain in an idle state until programmed to resume serial data activities. $\overline{RESET}$ has a hysteresis level of typically 400 mV.
$\overline{RTS0}$, $\overline{RTS1}$	24, 12	O	Request to send. The $\overline{RTS}$ outputs are set low by setting MCR1 of its UARTs modem control register. Both $\overline{RTS}$ terminals are reset high by $\overline{RESET}$. A low on $\overline{RTS}$ indicates that its ACE has data ready to transmit. In half-duplex operations, $\overline{RTS}$ controls the direction of the line.
$\overline{RXRDY0}$, $\overline{RXRDY1}$	9, 61	O	Receiver ready. Receiver direct memory access (DMA) signaling is also available through this output. One of two types of DMA signaling can be selected using FCR3 when operating in the FIFO mode. Only DMA mode 0 is allowed when operating in the TL16C450 mode. For signal transfer DMA (a transfer is made between CPU bus cycles), mode 0 is used. Multiple transfers that are made continuously until the receiver FIFO has been emptied are supported by mode 1. Mode 0. $\overline{RXRDY}$ is active (low) when in the FIFO mode (FCR0 = 1, FCR3 = 0) or when in the TL16C450 mode (FCR0 = 0) and the receiver FIFO or receiver holding register contain at least one character. When there are no more characters in the FIFO or holding register, $\overline{RXRDY}$ goes inactive (high). Mode 1. $\overline{RXRDY}$ goes active (low) in the FIFO mode (FCR0 = 1) when FCR3 = 1 and the time-out or trigger levels have been reached. $\overline{RXRDY}$ goes inactive (high) when the FIFO or holding register is empty.
$\overline{RI0}$, $\overline{RI1}$	30, 6	I	Ring indicator. The $\overline{RI}$ signal is a modem control input. Its condition is tested by reading MSR6 (RI) of each ACE. The modem status register output TERI (MSR2) indicates whether $\overline{RI}$ has changed from high to low since the previous reading of the modem status register.
SIN0, SIN1	41, 62	I	Serial data. SIN0 and SIN1 move information from the communication line or modem to the TL16C552AI receiver circuits. Mark is a high state and space is a low state. Data on serial data inputs is disabled when operating in the loop mode.
SLCT	65	I	Line printer select. SLCT is an input line from the printer that goes high when the printer is selected.
$\overline{SLIN}$	58	I/O	Line printer select. $\overline{SLIN}$ is an open-drain I/O that selects the printer when active (low). $\overline{SLIN}$ has an internal pullup resistor to V_{DD} of approximately 10 kΩ.
SOUT0, SOUT1	26, 10	O	Serial data outputs. SOUT0 and SOUT1 are the serial data outputs from the ACE transmitter circuitry. A mark is a high state and a space is a low state. Each SOUT is held in the mark condition when the transmitter is disabled ($\overline{RESET}$ is asserted low) the transmitter register is empty, or when in the loop mode.
$\overline{STB}$	55	I/O	Line printer strobe. STB provides communication between the TL16C552AI and the printer. When $\overline{STB}$ is active (low), it provides the printer with a signal to latch the data currently on the parallel port. $\overline{STB}$ has an internal pullup resistor to V_{DD} of approximately 10 kΩ.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
TRI	2	I	3-state output control input. TRI controls the 3-state control of all I/O and output terminals. When TRI is asserted, all I/Os and outputs are in the high-impedance state allowing board level testers to drive the outputs without overdriving internal buffers. TRI is level sensitive and is pulled down with an internal resistor that is approximately 5 kΩ.
$\overline{\text{TXRDY0}}$ $\overline{\text{TXRDY1}}$	22 42	O	Transmitter ready. Two types of DMA signaling are available. Either can be selected using FCR3 when operating in the FIFO mode. Only DMA mode 0 is allowed when operating in the TL16C450 mode. Single-transfer DMA (a transfer is made between CPU bus cycles) is supported by mode 0. Multiple transfers that are made continuously until the transmitter FIFO has been filled are supported by mode 1. Mode 0. When in the FIFO mode (FCR0 = 1, FCR3 = 0) or in the TL16C450 mode (FCR0 = 0) and there are no characters in the transmitter holding register or transmitter FIFO, $\overline{\text{TXRDYx}}$ is active (low). Once $\overline{\text{TXRDYx}}$ is activated (low), it goes inactive after the first character is loaded into the holding register of the transmitter FIFO. Mode 1. $\overline{\text{TXRDY}}$ goes active (low) when in the FIFO mode (FCR0 = 1) when FCR3 = 1 and there are no characters in the transmitter FIFO. When the transmitter FIFO is completely full, $\overline{\text{TXRDY}}$ goes inactive (high).
V_{DD}	23, 40, 64		Power supply. The V_{DD} requirement is 5 V ±5%.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 1) ..... −0.5 V to V_{DD} + 0.3 V
Input voltage range, V_I ..... −0.5 V to 7 V
Output voltage range, V_O ..... −0.5 V to V_{DD} + 0.3 V
Continuous total power dissipation at (or below) 70°C ..... 500 mW
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage levels are with respect to GND.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.75	5	5.25	V
Clock high-level input voltage, $V_{IH(CLK)}$	2		V_{DD}	V
Clock low-level input voltage, $V_{IL(CLK)}$	−0.5		0.8	V
High-level input voltage, V_{IH}	2		V_{DD}	V
Low-level input voltage, V_{IL}	−0.5		0.8	V
Clock frequency, f_{clock}			16	MHz
Operating free-air temperature, T_A	−40		85	°C

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −0.4 mA for DB0–DB7, I_{OH} = −2 mA for PD0–PD7, I_{OH} = −0.4 mA for $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$, and $\overline{SLIN}$ (see Note 2), I_{OH} = −0.4 mA for all other outputs	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA for DB0–DB7, I_{OL} = 12 mA for PD0–PD7, I_{OL} = 10 mA for $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$, and $\overline{SLIN}$ (see Note 2), I_{OL} = 2 mA for all other outputs		0.4	V
I_I	Input current	V_{DD} = 5.25 V, All other terminals are floating		±10	μA
$I_{I(CLK)}$	Clock input current	V_I = 0 to 5.25 V		±10	μA
I_{OZ}	High-impedance output current	V_{DD} = 5.25 V, V_O = 0 with chip deselected or V_O = 5.25 V with chip and write mode selected		±20	μA
I_{DD}	Supply current	V_{DD} = 5.25 V, No loads on outputs, SIN0, SIN1, $\overline{DSR0}$, $\overline{DSR1}$, $\overline{DCD0}$, $\overline{DCD1}$, $\overline{CTS0}$, $\overline{CTS1}$, $\overline{RI0}$ and $\overline{RI1}$ at 2 V, Other inputs at 0.8 V, Baud rate generator f_{clock} = 8 MHz, Baud rate = 56 kbit/s		50	mA

NOTE 2: These four terminals contain an internal pullup resistor to V_{DD} of approximately 10 kΩ.

clock timing requirements over recommended ranges of operating free-air temperature and supply voltage

		MIN	MAX	UNIT
t_{w1}	Pulse duration, CLK ↑ (external clock) (see Figure 1)	31		ns
t_{w2}	Pulse duration, CLK ↓ (external clock) (see Figure 1)	31		ns
t_{w3}	Pulse duration, $\overline{RESET}$	1000		ns

read cycle timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 4)

		MIN	MAX	UNIT
t_{w4}	Pulse duration, $\overline{IOR}$ ↓	80		ns
t_{su1}	Setup time, $\overline{CSx}$ valid before $\overline{IOR}$ ↓ (see Note 3)	15		ns
t_{su2}	Setup time, A2–A0 valid before $\overline{IOR}$ ↓ (see Note 3)	15		ns
t_{h1}	Hold time, A2–A0 valid after $\overline{IOR}$ ↑ (see Note 3)	20		ns
t_{h2}	Hold time, $\overline{CSx}$ valid after $\overline{IOR}$ ↑ (see Note 3)	20		ns
t_{d1}	Delay time, $t_{su2} + t_{w4} + t_{d2}$ (see Note 4)	175		ns
t_{d2}	Delay time, $\overline{IOR}$ ↑ to $\overline{IOR}$ or $\overline{IOW}$ ↓	80		ns

NOTES: 3. The internal address strobe is always active.
4. In the FIFO mode, t_{d1} = 425 ns (min) between reads of the receiver FIFO and the status registers (interrupt identification register and line status register).

write cycle timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 5)

		MIN	MAX	UNIT
t_{w5}	Pulse duration, $\overline{IOW}$ ↓	80		ns
t_{su4}	Setup time, $\overline{CSx}$ valid before $\overline{IOW}$ ↓ (see Note 3)	15		ns
t_{su5}	Setup time, A2–A0 valid before $\overline{IOW}$ ↓ (see Note 3)	15		ns
t_{su6}	Setup time, DB0–DB7 valid before $\overline{IOW}$ ↑	15		ns
t_{h3}	Hold time, A2–A0 valid after $\overline{IOW}$ ↑ (see Note 3)	20		ns
t_{h4}	Hold time, $\overline{CSx}$ valid after $\overline{IOW}$ ↑ (see Note 3)	20		ns
t_{h5}	Hold time, DB0–DB7 valid after $\overline{IOW}$ ↑	15		ns
t_{d3}	Delay time, $t_{su5} + t_{w5} + t_{d4}$	175		ns
t_{d4}	Delay time, $\overline{IOW}$ ↑ to $\overline{IOW}$ or $\overline{IOR}$ ↓	80		ns

NOTE 3: The internal address strobe is always active.

read cycle switching characteristics over recommended ranges of operating free-air temperature and supply voltage, C_L = 100 pF (see Note 5 and Figure 4)

	PARAMETER	MIN	MAX	UNIT
t_{pd1}	Propagation delay time from $\overline{IOR}$ ↓ to BDO ↑ or from $\overline{IOR}$ ↑ to BDO ↓		60	ns
t_{en}	Enable time from $\overline{IOR}$ ↓ to DB0–DB7 valid		60	ns
t_{dis}	Disable time from $\overline{IOR}$ ↑ to DB0–DB7 released	0	60	ns

NOTE 5: V_{OL} and V_{OH} (and the external loading) determine the charge and discharge time.

transmitter switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figures 6, 7, and 8)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{d5}	Delay time, interrupt THRE† ↓ to SOUT ↓ at start	See Figure 6	8	24	RCLK cycles
t_{d6}	Delay time, SOUT ↓ at start to interrupt THRE ↑	See Note 6 and Figure 6	8	9	RCLK cycles
t_{d7}	Delay time, $\overline{IOW}$ (WR THR) ↑ to interrupt THRE ↑	See Note 6 and Figure 6	16	32	RCLK cycles
t_{d8}	Delay time, SOUT ↓ at start to $\overline{TXRDY}$ ↓	C_L = 100 pF, See Figures 7 and 8		8	RCLK cycles
t_{pd2}	Propagation delay time from $\overline{IOW}$ (WR THR) ↓ to interrupt THRE ↓	C_L = 100 pF, See Figure 6		140	ns
t_{pd4}	Propagation delay time from $\overline{IOR}$ (RD IIR) ↑ to interrupt THRE ↓	C_L = 100 pF, See Figure 6		140	ns
t_{pd5}	Propagation delay time from $\overline{IOW}$ (WR THR) ↑ to $\overline{TXRDY}$ ↑	C_L = 100 pF, See Figures 7 and 8		195	ns

† The acronym THRE is for transmitter holding register empty.

NOTE 6: When the transmitter interrupt delay is active, this delay is lengthened by one character time minus the last stop bit time.

receiver switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figures 9 through 13)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{d9}	Delay time from stop to INT ↑	See Note 7		1	RCLK cycle
t_{pd6}	Propagation delay time from RCLK ↑ to sample CLK ↑			100	ns
t_{pd7}	Propagation delay time from $\overline{IOR}$ (RD RBR/RD LSR) ↓ to reset interrupt ↓	C_L = 100 pF		150	ns
t_{pd8}	Propagation delay time from $\overline{IOR}$ (RD RBR) ↓ to $\overline{RXRDY}$ ↑			150	ns

NOTE 7: The receiver data available indicator, the overrun error indicator, the trigger level interrupts, and the active $\overline{RXRDY}$ indicator are delayed three RCLK cycles in the FIFO mode (FCR0 = 1). After the first byte has been received, status indicators (PE, FE, BI) are delayed three RCLK cycles. These indicators are updated immediately for any further bytes received after RDRBR goes active. There are eight RCLK cycle delays for trigger change level interrupts.

modem control switching characteristics over recommended ranges of operating free-air temperature and supply voltage, C_L = 100 pF (see Figure 14)

PARAMETER		MIN	MAX	UNIT
t_{pd9}	Propagation delay time from $\overline{IOW}$ (WR MCR) ↑ to $\overline{RTS}$ ($\overline{DTR}$) ↓↑		100	ns
t_{pd10}	Propagation delay time from modem input ($\overline{CTS}$, $\overline{DSR}$) ↓↑ to interrupt ↑		170	ns
t_{pd11}	Propagation delay time from $\overline{IOR}$ (RD MSR) ↑ to interrupt ↓		140	ns
t_{pd12}	Propagation delay time from $\overline{RI}$ ↑ to interrupt ↑		170	ns

parallel port timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 15, 16, and 17)

		MIN	MAX	UNIT
t_{su7}	Setup time, data valid before $\overline{STB}$ ↓	1		µs
t_{h6}	Hold time, data valid after $\overline{STB}$ ↑	1		µs
t_{w6}	Pulse duration, $\overline{STB}$ ↓	1		µs
t_{d10}	Delay time, BUSY ↑ to $\overline{ACK}$ ↓	Defined by printer		
t_{d11}	Delay time, BUSY ↓ to $\overline{ACK}$ ↓	Defined by printer		
t_{w7}	Pulse duration, BUSY ↑	Defined by printer		
t_{w8}	Pulse duration, $\overline{ACK}$ ↓	Defined by printer		
t_{d12}	Delay time, BUSY ↑ after $\overline{STB}$ ↑	Defined by printer		
t_{d13}	Delay time, INT2 ↓ after $\overline{ACK}$ ↓ (see Note 8)		22	ns
t_{d14}	Delay time, INT2 ↑ after $\overline{ACK}$ ↑ (see Note 8)		20	ns
t_{d15}	Delay time, INT2 ↑ after $\overline{ACK}$ ↑ (see Note 8)		24	ns
t_{d16}	Delay time, INT2 ↓ after $\overline{IOR}$ ↑ (see Note 8)		25	ns

NOTE 8: t_{d13}–t_{d16} are all measured with a 15-pF load.

PARAMETER MEASUREMENT INFORMATION

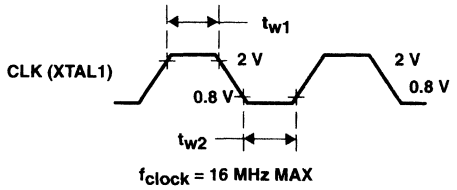
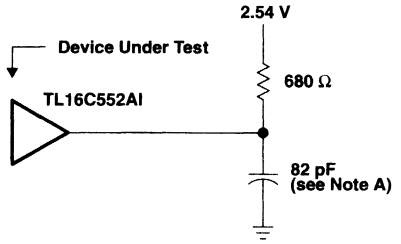


Figure 1. CLK Voltage Waveform



NOTE A: This includes scope and jig capacitance.

Figure 2. Output Load Circuit

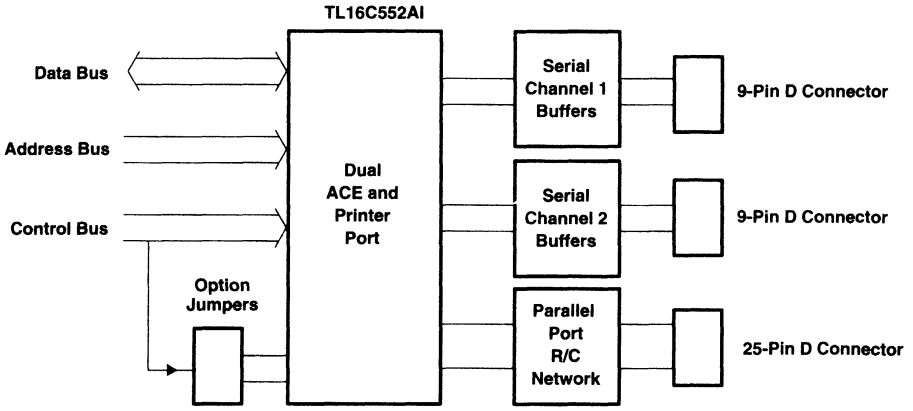


Figure 3. Basic Test Configuration

PARAMETER MEASUREMENT INFORMATION

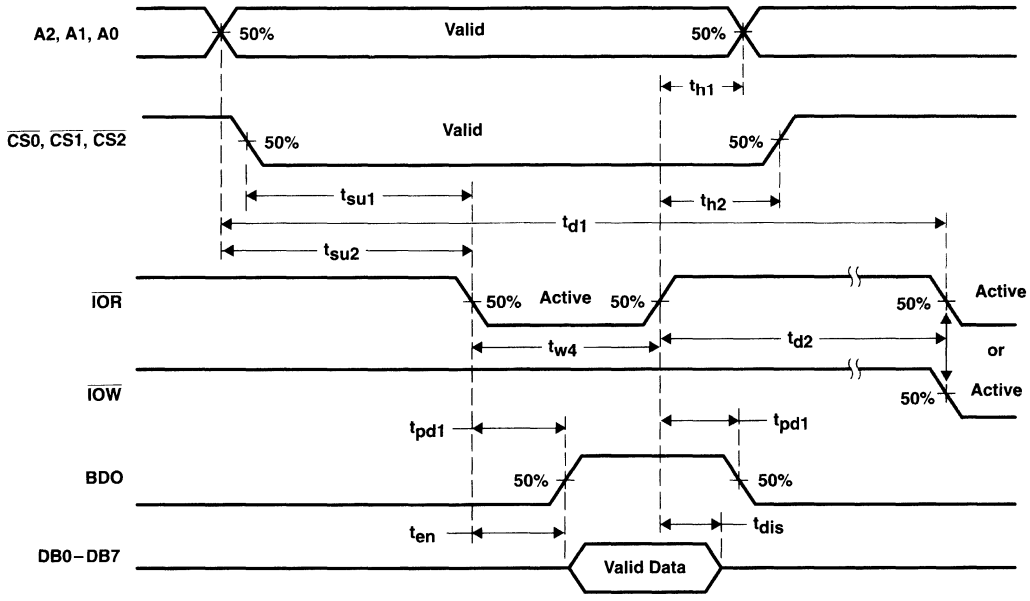


Figure 4. Read Cycle Timing Waveforms

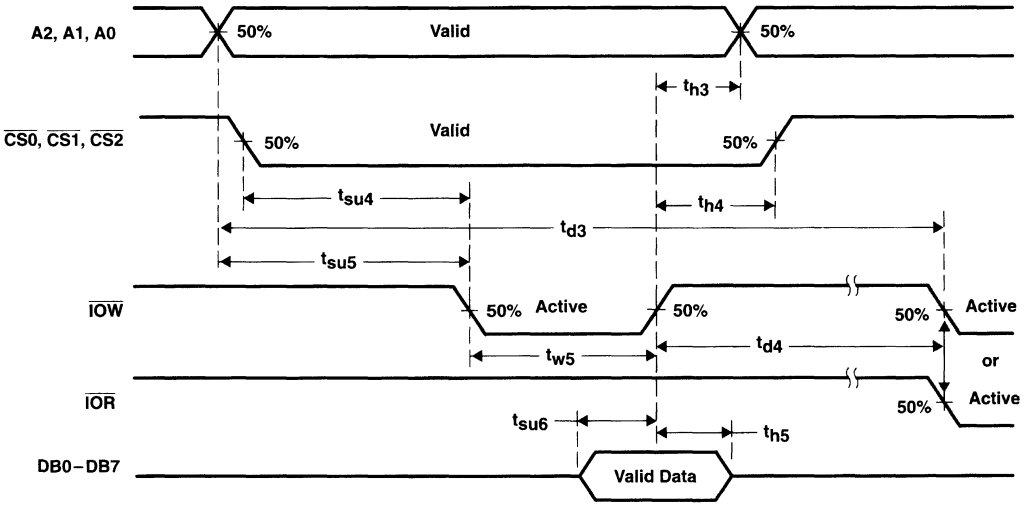


Figure 5. Write Cycle Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

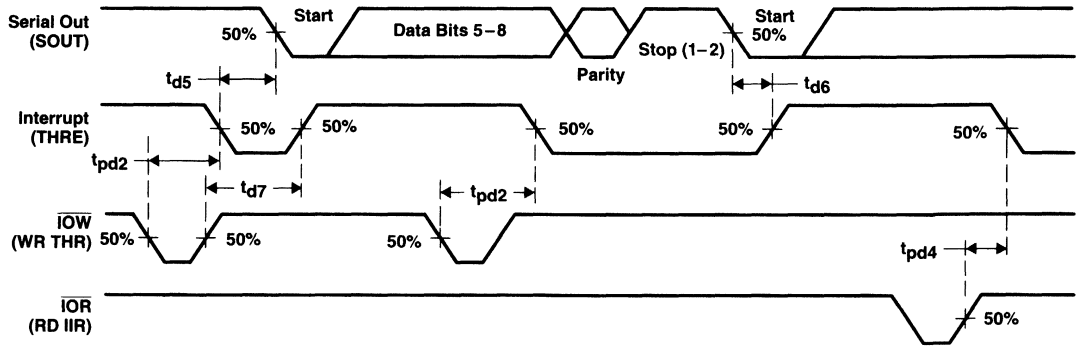


Figure 6. Transmitter Timing Waveforms

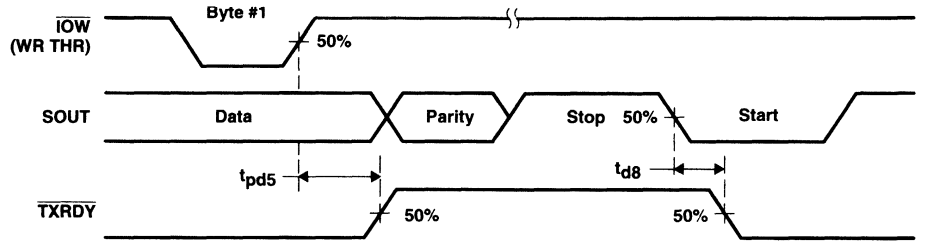


Figure 7. Transmitter Ready Mode 0 Timing Waveforms

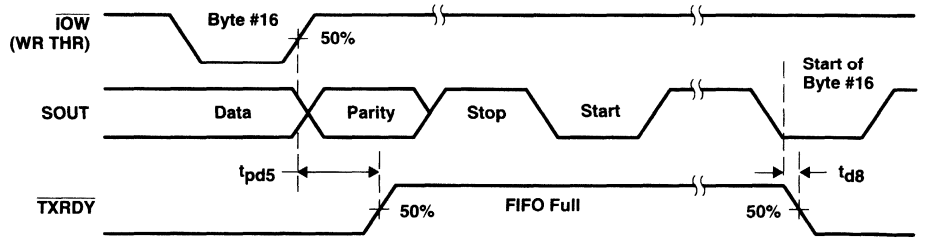


Figure 8. Transmitter Ready Mode 1 Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

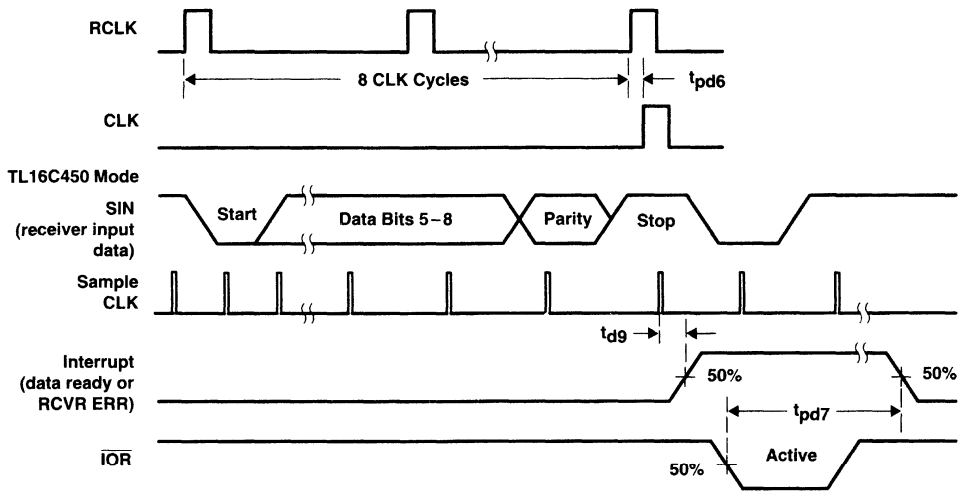


Figure 9. Receiver Timing Waveforms

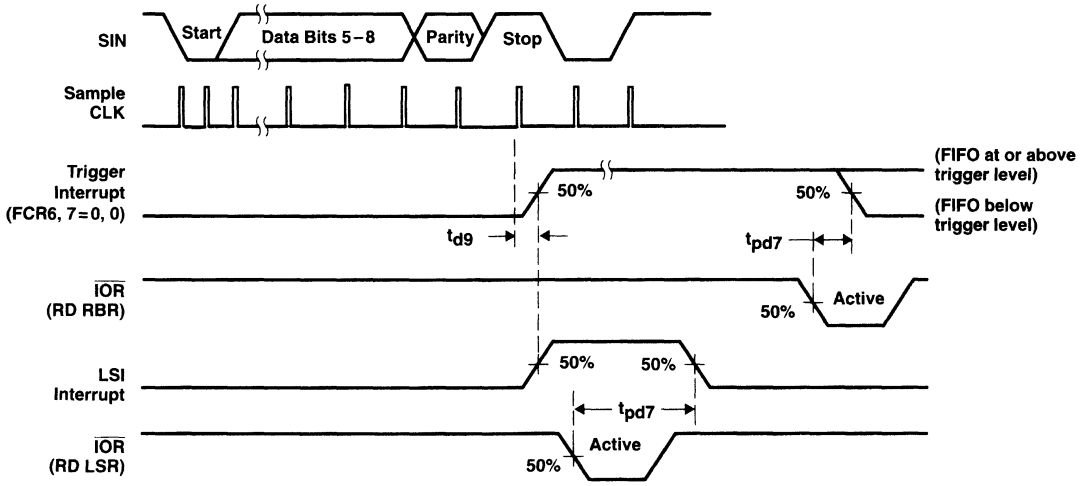
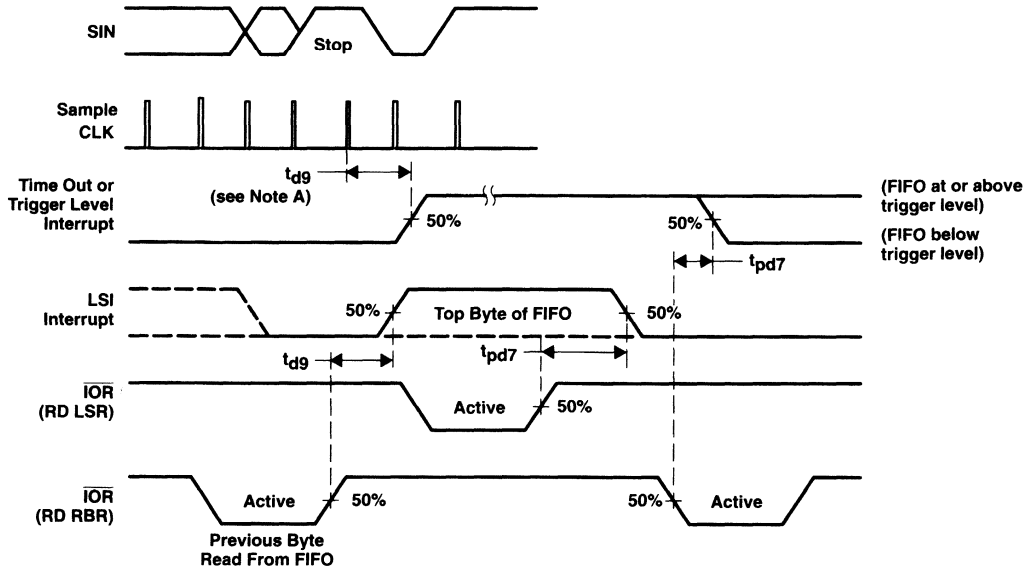


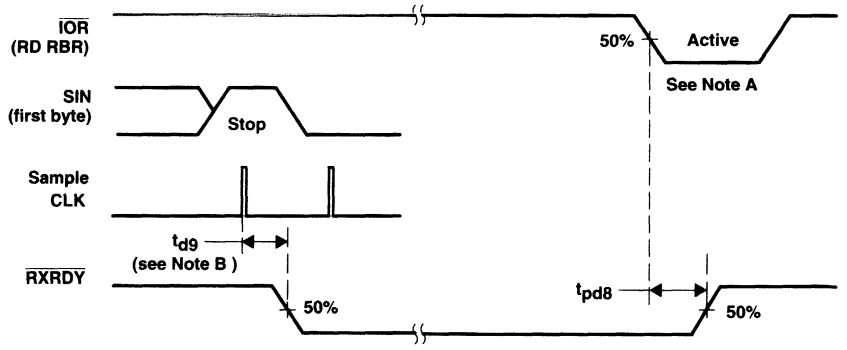
Figure 10. Receiver FIFO First Byte (Sets RDR) Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: This is the reading of the last byte in the FIFO.

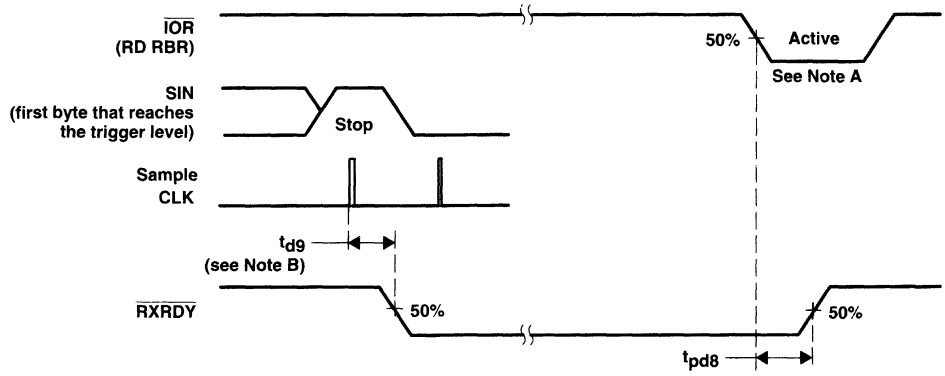
Figure 11. Receiver FIFO After First Byte (After RDR Set) Waveforms



NOTES: A. This is the reading of the last byte in the FIFO.
B. If FCR0 = 1, t_{d9} = 3 RCLK cycles. For a time-out interrupt, t_{d9} = 8 RCLK cycles.

Figure 12. Receiver Ready Mode 0 Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. This is the reading of the last byte in the FIFO.
B. If FCR0–1, t_{d9} = 3 RCLK cycles. For a trigger change level interrupt, t_{d9} = 8 RCLK.

Figure 13. Receiver Ready Mode 1 Waveforms

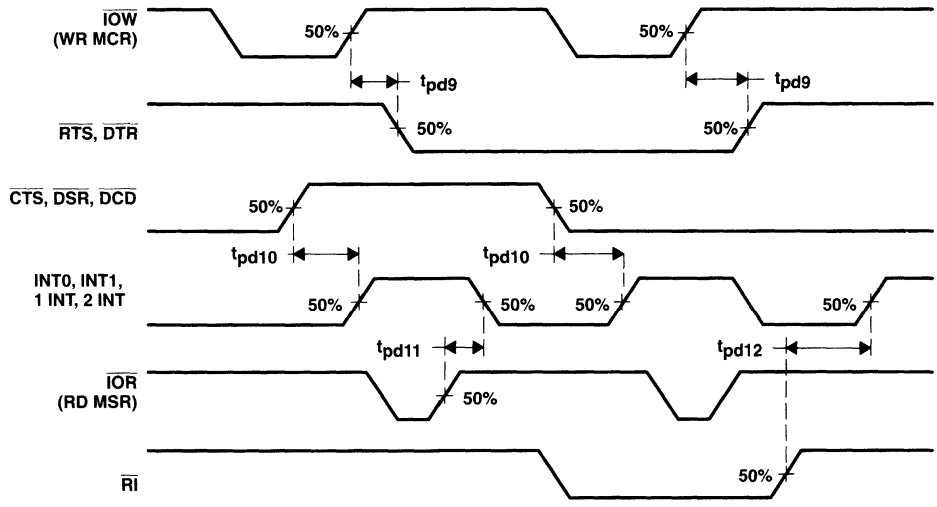


Figure 14. Modem Control Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

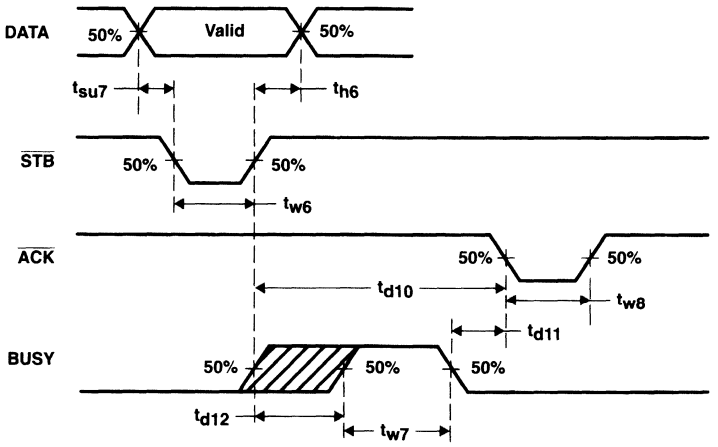
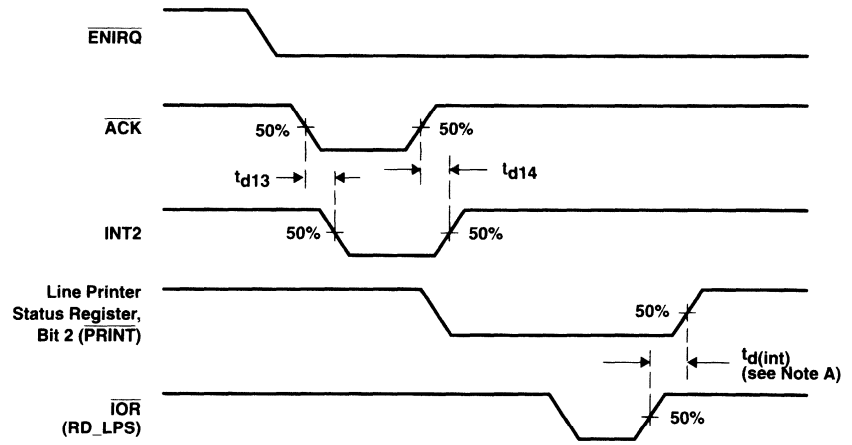


Figure 15. Parallel Port Timing Waveforms



NOTE A: A timing value is not provided for $t_{d(int)}$ in the tables since the line printer status register, bit 2 (PRINT) is an internal signal.

Figure 16. Parallel Port AT Mode Timing (ENIRQ = Low) Waveforms

PARAMETER MEASUREMENT INFORMATION

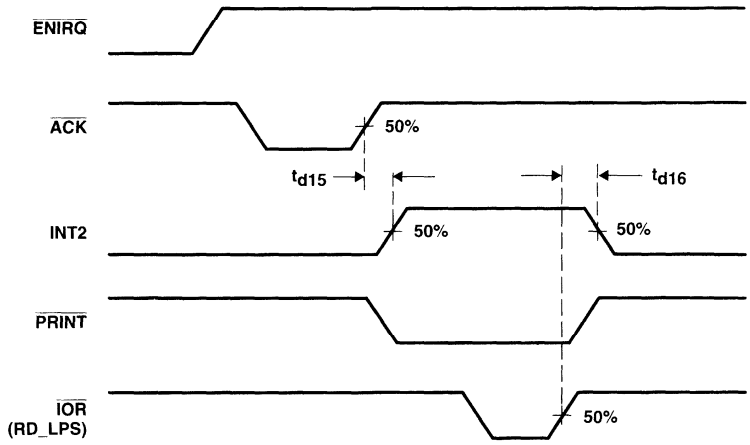


Figure 17. Parallel Port PS/2 Mode Timing (ENIRQ = High) Waveforms

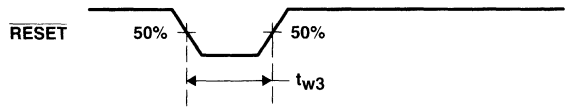


Figure 18. RESET Voltage Waveform

PRINCIPLES OF OPERATION

Three types of information are stored in the internal registers used in the ACE: control, status, and data. Mnemonic abbreviations for the internal registers are shown in Table 1.

Table 1. Internal Register Mnemonic Abbreviations

CONTROL	MNEMONIC	STATUS	MNEMONIC	DATA	MNEMONIC
Line control register	LCR	Line status register	LSR	Receiver buffer register	RBR
FIFO control register	FCR	Modem status register	MSR	Transmitter holding register	THR
Modem control register	MCR				
Divisor latch LSB	DLL				
Divisor latch MSB	DLM				
Interrupt enable register	IER				

The address, read, and write inputs are used with the divisor latch access bit (DLAB) in the line control register (bit 7) to select the register to be written or read (see Table 2). Individual bits within the registers are referred to by the register mnemonic and the bit number in parenthesis. As an example, LCR7 refers to line control register bit 7.

The transmitter holding register and receiver buffer register are data registers that hold from five to eight bits of data. If less than eight data bits are transmitted, data is right justified to the LSB. Bit 0 of a data word is always the first serial data bit received and transmitted. The ACE data registers are double buffered (TL16C450 mode) or FIFO buffered (FIFO mode) so that read and write operations can be performed when the ACE is performing the parallel-to-serial or serial-to-parallel conversion.

Table 2. Register Selection†

DLAB	A2	A1	A0	MNEMONIC	REGISTER
L	L	L	L	RBR	Receiver buffer register (read only)
L	L	L	L	THR	Transmitter holding register (write only)
L	L	L	H	IER	Interrupt enable register
X	L	H	L	IIR	Interrupt identification register (read only)
X	L	H	L	FCR	FIFO control register (write only)
X	L	H	H	LCR	Line control register
X	H	L	L	MCR	Modem control register
X	H	L	H	LSR	Line status register
X	H	H	L	MSR	Modem status register
X	H	H	H	SCR	Scratch pad register
H	L	L	L	DLL	LSB divisor latch
H	L	L	H	DLM	MSB divisor latch

† The serial channel is accessed when either $\overline{CS0}$ or $\overline{CS1}$ is low.
X = irrelevant, L = low level, H = high level

PRINCIPLES OF OPERATION

accessible registers

The system programmer, using the CPU, has access to and control over any of the ACE registers that are summarized in Table 1. These registers control ACE operations, receive data, and transmit data. Descriptions of these registers follow Table 3.

Table 3. Summary of Accessible Registers

ADDRESS	REGISTER MNEMONIC	REGISTER BIT NUMBER							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	RBR (read only)	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)
0	THR (write only)	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
0†	DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1†	DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
1	IER	0	0	0	0	(EDSSI) Enable modem status interrupt	(ERLSI) Enable receiver line status interrupt	(ETBEI) Enable transmitter holding register empty interrupt	(ERBFI) Enable received data available interrupt
2	FCR (write only)	Receiver Trigger (MSB)	Receiver Trigger (LSB)	Reserved	Reserved	DMA mode select	Transmitter FIFO reset	Receiver FIFO reset	FIFO Enable
2	IIR (read only)	FIFOs Enabled‡	FIFOs Enabled‡	0	0	Interrupt ID Bit 3‡	Interrupt ID Bit 2	Interrupt ID Bit 1	0 If interrupt pending
3	LCR	(DLAB) Divisor latch access bit	Set break	Stick parity	(EPS) Even parity select	(PEN) Parity enable	(STB) Number of stop bits	(WLSB1) Word length select bit 1	(WLSB0) Word length select bit 0
4	MCR	0	0	0	Loop	OUT2 Enable external interrupt (INT0 or INT1)	OUT1 (an unused internal signal)	(RTS) Request to send	(DTR) Data terminal ready
5	LSR	Error in Receiver FIFO‡	(TEMT) Transmitter empty	(THRE) Transmitter holding register empty	(BI) Break interrupt	(FE) Framing error	(PE) Parity error	(OE) Overrun error	(DR) Data ready
6	MSR	(DCD) Data carrier detect	(RI) Ring indicator	(DSR) Data set ready	(CTS) Clear to send	(ΔDCD) Delta data carrier detect	(TERI) Trailing edge ring indicator	(ΔDSR) Delta data set ready	(ΔCTS) Delta clear to send
7	SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

† DLAB = 1

‡ These bits are always 0 when FIFOs are disabled.

PRINCIPLES OF OPERATION

FIFO control register (FCR)

This write only register is at the same location as the interrupt identification register. It enables and clears the FIFOs, sets the trigger level of the receiver FIFO, and selects the type of DMA signaling.

- Bit 0: FCR0 enables both the transmitter and receiver FIFOs. All bytes in both FIFOs can be cleared by clearing FCR0. Data is cleared automatically from the FIFOs when changing from the FIFO mode to the TL16C450 mode and vice versa. Programming of other FCR bits is enabled by setting FCR0.
- Bit 1: When set, FCR1 clears all bytes in the receiver FIFO and resets the counter. This does not clear the shift register.
- Bit 2: When set, FCR2 clears all bytes in the transmitter FIFO and resets the counter. This does not clear the shift register.
- Bit 3: When set, FCR3 changes the $\overline{\text{RXRDY}}$ and $\overline{\text{TXRDY}}$ terminals from mode 0 to mode 1 when FCR0 is set.
- Bits 4 and 5: FCR4 and FCR5 are reserved for future use.
- Bits 6 and 7: FCR6 and FCR7 set the trigger level for the receiver FIFO interrupt (see Table 4):

Table 4. Receiver FIFO Trigger Level

BIT		RECEIVER FIFO TRIGGER LEVEL (BYTES)
7	6	
0	0	01
0	1	04
1	0	08
1	1	14

FIFO interrupt mode operation

The following receiver status occurs when the receiver FIFO and receiver interrupts are enabled:

1. LSR0 is set when a character is transferred from the shift register to the receiver FIFO. When the FIFO is empty, it is reset.
2. IIR = 06 receiver line status interrupt has higher priority than the received data available interrupt IIR = 04.
3. Receive data available interrupt is issued to the CPU when the programmed trigger level is reached by the FIFO. When the FIFO drops below its programmed trigger level, it is cleared.
4. IIR = 04 (receive data available indicator) also occurs when the FIFO reaches its trigger level. It is cleared when the FIFO drops below the programmed trigger level.

The following receiver FIFO character time-out status occurs when receiver FIFO and receiver interrupts are enabled.

PRINCIPLES OF OPERATION

FIFO interrupt mode operation (continued)

1. When the following conditions exist, a FIFO character time-out interrupt occurs:
   a. Minimum of one character in FIFO
   b. Last received serial character is longer than four continuous previous character times ago (if two stop bits are programmed, the second one is included in the time delay)
   c. The last CPU read of the FIFO is more than four continuous character times earlier. At 300 baud and 12-bit characters, the FIFO time-out interrupt causes a latency of 160 ms maximum from received character to interrupt issued.
2. By using the RCLK input for a clock signal, the character times can be calculated. The delay is proportional to the baud rate.
3. The time-out timer is reset after the CPU reads the receiver FIFO or after a new character is received when there has been no time-out interrupt.
4. A time-out interrupt is cleared and the timer is reset when the CPU reads a character from the receiver FIFO.

Transmitter interrupts occur as follows when the transmitter and transmitter FIFO interrupts are enabled (FCR0 = 1, IER = 1).

1. When the transmitter FIFO is empty, the transmitter holding register interrupt (IIR = 02) occurs. The interrupt is cleared when the transmitter holding register is written to or the IIR is read. One to sixteen characters can be written to the transmit FIFO when servicing this interrupt.
2. The transmitter FIFO empty indicators are delayed one character time minus the last stop bit time when the following occurs:

   THRE = 1 and there is not a minimum of two bytes at the same time in transmitter FIFO since the last THRE = 1. The first transmitter interrupt after changing FCR0 is immediate assuming it is enabled.

receiver FIFO trigger level and character time-out interrupts have the same priority as the received data available interrupt. The transmitter holding register empty interrupt has the same priority as the transmitter FIFO empty interrupt.

FIFO polled mode operation

Clearing IER0, IER1, IER2, IER3, or all with FCR0 = 1 puts the ACE into the FIFO polled mode. The receiver and transmitter are controlled separately. Either one or both can be in the polled mode.

In the FIFO polled mode, there is no time-out condition indicated or trigger level reached. However, the receiver and transmitter FIFOs still have the capability of holding characters. The LSR must be read to determine the ACE status.

interrupt enable register (IER)

The IER independently enables the four serial channel interrupt sources that activate the interrupt (INT0 or INT1) output. All interrupts are disabled by clearing IER0 – IER3. Interrupts are enabled by setting the appropriate bits of the IER. Disabling the interrupt system inhibits the interrupt identification register and the active (high) interrupt output. All other system functions operate in their normal manner, including the setting of the LSRs and MSRs. The contents of the IER shown in Table 3 are described in the following bulleted list.

- Bit 0: When IER0 is set, IER0 enables the received data available interrupt and the time-out interrupts in the FIFO mode.

PRINCIPLES OF OPERATION

interrupt enable register (IER) (continued)

- Bit 1: When IER1 is set, the transmitter holding register empty interrupt is enabled.
- Bit 2: When IER2 is set, the receiver line status interrupt is enabled.
- Bit 3: When IER3 is set, the modem status interrupt is enabled.
- Bits 4 – 7: IER4 through IER7 are cleared.

In order to minimize software overhead during data character transfers, the serial channel prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows:

- Priority 1 – Receiver line status (highest priority)
- Priority 2 – Receiver data ready or receiver character time out
- Priority 3 – Transmitter holding register empty
- Priority 4 – Modem status (lowest priority)

Information indicating that a prioritized interrupt is pending and the type of interrupt is stored in the IIR. The IIR indicates the highest priority interrupt pending. The contents of the IIR are indicated in Table 5.

Table 5. Interrupt Control Functions

INTERRUPT IDENTIFICATION REGISTER				INTERRUPT SET AND RESET FUNCTIONS			
BIT 3	BIT 2	BIT 1	BIT 0	PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET CONTROL
0	0	0	1	–	None	None	–
0	1	1	0	First	Receiver line status	OE, PE, FE, or BI	LSR read
0	1	0	0	Second	Received data available	Receiver data available or trigger level reached	RBR read until FIFO drops below the trigger level
1	1	0	0	Second	Character time-out indicator	No characters have been removed from or input to the receiver FIFO during the last four character times and there is at least one character in it during this time.	RBR read
0	0	1	0	Third	THRE	THRE	IIR read if THRE is the interrupt source or THR write
0	0	0	0	Fourth	Modem status	$\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$, or $\overline{DCD}$	MSR read

- Bit 0: IIR0 indicates whether an interrupt is pending. When IIR0 is cleared, an interrupt is pending.
- Bits 1 and 2: IIR1 and IIR2 identify the highest priority interrupt pending as indicated in Table 5.
- Bit 3: IIR3 is always cleared when in the TL16C450 mode. This bit is set along with bit 2 when in the FIFO mode and a trigger change level interrupt is pending.
- Bits 4 and 5: IIR4 and IIR5 are always cleared.
- Bits 6 and 7: IIR6 and IIR7 are set when FCR0 = 1.

PRINCIPLES OF OPERATION

line control register (LCR)

The format of the data character is controlled by the LCR. The LCR can be read. Its contents are described in the following bulleted list and shown in Figure 19.

- Bits 0 and 1: LCR0 and LCR1 are the word length select bits. The number of bits in each serial character is programmed as shown.
- Bit 2: LCR2 is the stop bit select bit. LCR2 specifies the number of stop bits in each transmitted character. The receiver always checks for one stop bit.
- Bit 3: LCR3 is the parity enable bit. When LCR3 is set, a parity bit between the last data word bit and stop bit is generated and checked.
- Bit 4: LCR4 is the even parity select bit. When LCR4 is set, even parity is enabled.
- Bit 5: LCR5 is the stick parity bit. When parity is enabled (LCR3 = 1), LCR5 = 1 causes the transmission and reception of a parity bit to be in the opposite state from the value of LCR4. This forces parity to a known state and allows the receiver to check the parity bit in a known state.
- Bit 6: LCR6 is the break control bit. When LCR6 is set, the serial output (SOUT1/SOUT0) is forced to the spacing state (low). The break control bit acts only on the serial output and does not affect the transmitter logic. When the following sequence is used, no invalid characters are transmitted because of the break:

  Step 1: Load a zero byte in response to the transmitter holding register empty (THRE) status indicator.

  Step 2: Set the break in response to the next THRE status indicator.

  Step 3: Wait for the transmitter to be idle when transmitter empty status signal is set high (TEMT = 1); then clear the break when the normal transmission has to be restored.

- Bit 7: LCR7 is the divisor latch access bit (DLAB) bit. LCR7 must be set to access the divisor latches DLL and DLM of the baud rate generator during a read or write operation. LCR7 must be cleared to access the receiver buffer register, the transmitter holding register, or the interrupt enable register.

PRINCIPLES OF OPERATION

line control register (LCR) (continued)

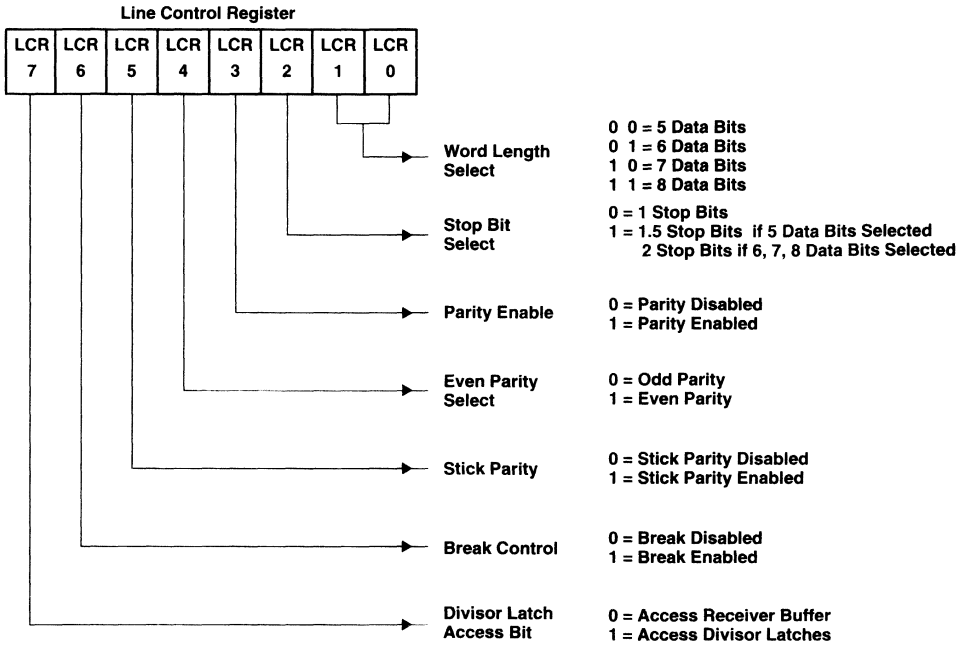


Figure 19. Line Control Register Contents

line printer port

The line printer port contains the functionality of the port included in the TL16C452 but offers a hardware programmable extended mode controlled by the printer enhancement mode (PE) terminal. This enhancement is the addition of a direction control bit and an interrupt status bit.

register 0 line printer data register

The line printer (LPT) port is either output only or bidirectional depending on the state of the extended mode terminal and data direction control bits.

Compatibility mode (PEMD = L)

Reads to the LPT data register return the last data that was written to the port. Write operations immediately output data to PD0–PD7.

Extended mode (PEMD = H)

Read operations return either the data last written to the LPT data register when the direction bit is cleared or return the data that is present on PD0 – PD7 when the direction is set to read. Write operations to the LPT data register latch data into the output register; however, they only drive the LPT port when the direction bit is cleared.

PRINCIPLES OF OPERATION

line printer port (continued)

Table 6 summarizes the configuration of the PD port based on the combinations of logic level on the PEMD terminal and value of the direction control bit (DIR).

Table 6. Extended Mode and Direction Control Bit Combinations

PEMD	DIR	PD0–PD7 FUNCTION
L	X	PC/AT mode – output
H	0	PS/2 mode – output
H	1	PS/2 mode – input

register 1 read line printer status register

The line printer status (LPS) register is a read-only register that contains interrupt and printer status of the LPT connector terminals. Table 7 (in the default column) shows the values of each bit after reset in the case of the printer being disconnected from the port.

Table 7. LPS Register Bit Description

BIT	DESCRIPTION	DEFAULT
0	Reserved	1
1	Reserved	1
2	$\overline{\text{PRINT}}$	1
3	$\overline{\text{ERR}}$	†
4	SLCT	†
5	PE	†
6	$\overline{\text{ACK}}$	†
7	$\overline{\text{BSY}}$	†

† Outputs are dependent upon device inputs.

- Bits 0 and 1: LPS0 and LPS1 are reserved and always set.
- Bit 2: LPS2 is the printer interrupt ($\overline{\text{PRINT}}$, active low) status bit. When cleared, LPS2 indicates that the printer has acknowledged the previous transfer with an ACK handshake (if bit 4 of the control register is set). The bit is cleared on the active-to-inactive transition of the $\overline{\text{ACK}}$ signal. This bit is set after a read of the status port.
- Bit 3: $\overline{\text{ERR}}$ is the error status bit and corresponds to $\overline{\text{ERR}}$ input.
- Bit 4: SLCT is the select status bit and corresponds to SLCT input.
- Bit 5: PE is the paper empty status bit and corresponds to PE input.
- Bit 6: $\overline{\text{ACK}}$ is the acknowledge status bit corresponds to $\overline{\text{ACK}}$ input.
- Bit 7: $\overline{\text{BSY}}$ is the busy status bit and corresponds to BUSY input (active high).

PRINCIPLES OF OPERATION

line printer port (continued)

register 2 line printer control register

The line printer control (LPC) register is a read/write port that controls the PD0–PD7 direction and drive the printer control lines. Write operations set or clear these bits, while read operations return the state of the last write operation to this register. The bits in this register are defined in Table 8 and the following bulleted list.

Table 8. LPC Register Bit Description

BIT	DESCRIPTION
0	STB
1	AFD
2	$\overline{\text{INIT}}$
3	SLIN
4	INT2 EN
5	DIR
6	Reserved 0
7	Reserved 0

- Bit 0: STB is the printer strobe control bit. When STB is set, the $\overline{\text{STB}}$ signal is asserted on the LPT interface. When STB is cleared, the $\overline{\text{STB}}$ signal is negated.
- Bit 1: AFD is the autofeed control bit. When AFD is set, the $\overline{\text{AFD}}$ signal is asserted on the LPT interface. When AFD is cleared, the signal is negated.
- Bit 2: $\overline{\text{INIT}}$ is the initialize printer control bit. When $\overline{\text{INIT}}$ is set, the $\overline{\text{INIT}}$ signal is negated. When $\overline{\text{INIT}}$ is cleared, the $\overline{\text{INIT}}$ signal is asserted on the LPT interface.
- Bit 3: SLIN is the select input control bit. When SLIN is set, the $\overline{\text{SLIN}}$ signal is asserted on the LPT interface. When SLIN is cleared, the signal is negated.
- Bit 4: INT2 EN is the interrupt request enable control bit. When set, INT2 EN enables interrupts from the LPT port. When cleared, INT2 EN disables interrupts and places INT2 signal in the high-impedance state.
- Bit 5: DIR is the direction control bit which is only used when PEMD is high. When DIR is set, the output buffers in the LPD port are disabled allowing data driven from external sources to be read from the LPD port. When DIR is cleared, the LPD port is in the output mode.
- Bits 6 and 7: These bits are reserved and are always cleared.

PRINCIPLES OF OPERATION

line status register (LSR)

The LSR is a single register that provides status indicators. The LSR shown in Table 9 is described in the following bulleted list.

- Bit 0: DR is the data ready bit. When DR is set when an incoming character is received and transferred into the receiver buffer register or the FIFO. LSR0 is cleared by a CPU read of the data in the receiver buffer register or the FIFO.
- Bit 1: OE is the overrun error bit. An OE indicates that data in the receiver buffer register is not read by the CPU before the next character is transferred into the receiver buffer register overwriting the previous character. The OE indicator is cleared whenever the CPU reads the contents of the LSR. An overrun error occurs in the FIFO mode after the FIFO is full and the next character is completely received. The overrun error is detected by the CPU on the first LSR read after it happens. The character in the shift register is not transferred to the FIFO, but it is overwritten.
- Bit 2: PE is the parity error bit. A PE indicates that the received data character does not have the correct parity as selected by LCR3 and LCR4. The PE bit is set upon detection of a parity error and is cleared when the CPU reads the contents of the LSR. In the FIFO mode, the parity error is associated with a particular character in the FIFO. LSR2 reflects the error when the character is at the top of the FIFO.
- Bit 3: FE is the framing error bit. A FE indicates that the received character does not have a valid stop bit. LSR3 is set when the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE indicator is cleared when the CPU reads the contents of the LSR. In the FIFO mode, the framing error is associated with a particular character in the FIFO. LSR3 reflects the error when the character is at the top of the FIFO.
- Bit 4: BI is the break interrupt bit. BI is set when the received data input is held in the spacing (low) state for longer than a full word transmission time (start bit + data bits + parity + stop bits). The BI indicator is cleared when the CPU reads the contents of the LSR. In the FIFO mode, this is associated with a particular character in the FIFO. LSR4 reflects BI when the break character is at the top of the FIFO. The error is detected by the CPU when its associated character is at the top of the FIFO during the first LSR read. Only one zero character is loaded into the FIFO when BI occurs.

LSR1 – LSR4 are the error conditions that produce a receiver line status interrupt (priority 1 interrupt in the interrupt identification register) when any of the conditions are detected. This interrupt is enabled by setting IER2 in the interrupt enable register.

- Bit 5: THRE is the transmitter holding register empty bit. THRE indicates that the ACE is ready to accept a new character for transmission. The THRE bit is set when a character is transferred from the transmitter holding register into the transmitter shift register. LSR5 is cleared by the loading of the transmitter holding register by the CPU. LSR5 is not cleared by a CPU read of the LSR. In the FIFO mode when the transmitter FIFO is empty, this bit is set. It is cleared when one byte is written to the transmitter FIFO. When the THRE interrupt is enabled by IER1, THRE causes a priority 3 interrupt in the IIR. If THRE is the interrupt source indicated in IIR, INTRPT is cleared by a read of the IIR.
- Bit 6: TEMT is the transmitter empty bit. TEMT is set when the transmitter holding register (THR) and the transmitter shift register are both empty. LSR6 is cleared when a character is loaded into the THR and remains cleared until the character is transferred out of SOUT. TEMT is not cleared by a CPU read of the LSR. In the FIFO mode, when both the transmitter FIFO and shift register are empty, TEMT is set.
- Bit 7: LSR7 is the receiver FIFO error bit. The LSR7 bit is always cleared in the TL16C450 mode. In FIFO mode, it is set when at least one of the following data errors is in the FIFO: parity error, framing error, or break interrupt indicator. It is cleared when the CPU reads the LSR if there are no subsequent errors in the FIFO.

PRINCIPLES OF OPERATION

line status register (LSR) (continued)

NOTE

The LSR may be written. However, this function is intended only for factory test. It should be considered as read only by applications software.

Table 9. Line Status Register Bits

LSR BITS	1	0
LSR0 data ready (DR)	Ready	Not ready
LSR1 overrun error (OE)	Error	No error
LSR2 parity error (PE)	Error	No error
LSR3 framing error (FE)	Error	No error
LSR4 break interrupt (BI)	Break	No break
LSR5 transmitter holding register empty (THRE)	Empty	Not empty
LSR6 transmitter empty (TEMT)	Empty	Not empty
LSR7 receiver FIFO error	Error in FIFO	No error in FIFO

master reset

After power up, the ACE $\overline{\text{RESET}}$ input should be held low for one microsecond to reset the ACE circuits to an idle mode until initialization. A low on $\overline{\text{RESET}}$ causes the following:

- It initializes the transmitter and receiver clock counters.
- It clears the LSR except for transmitter shift register empty (TEMT) and transmit holding register empty (THRE), which are set. The MCR is also cleared. All of the discrete lines, memory elements, and miscellaneous logic associated with these register bits are also cleared or turned off. The LCR, divisor latches, receiver buffer register, and transmitter holding buffer register are not affected.

Following the removal of the reset condition ($\overline{\text{RESET}}$ high), the ACE remains in the idle mode until programmed. A hardware reset of the ACE sets the THRE and TEMT status bit in the LSR. When interrupts are subsequently enabled, an interrupt occurs due to THRE. A summary of the effect of a reset on the ACE is given in Table 10.

PRINCIPLES OF OPERATION

master reset (continued)

Table 10. $\overline{\text{RESET}}$ Affects on Registers and Signals

REGISTER/SIGNAL	RESET CONTROL	RESET
Interrupt enable register	Reset	All bits cleared (0–3 forced and 4–7 permanent)
Interrupt identification register	Reset	Bit 0 is set, bits 1, 2, 3, 6, and 7 are cleared, and bits 4–5 are permanently cleared.
Line control register	Reset	All bits cleared
Modem control register	Reset	All bits cleared (5–7 permanent)
FIFO control register	Reset	All bits cleared
Line status register	Reset	All bits are cleared, except bits 5 and 6 are set.
Modem status register	Reset	Bits 0–3 cleared, bits 4–7 input signal
SOUT	Reset	High
Interrupt (RCVR errs)	Read LSR/Reset	Low
Interrupt (receiver data ready)	Read RBR/Reset	Low
Interrupt (THRE)	Read IIR/Write THR/Reset	Low
Interrupt (modem status changes)	Read MSR/Reset	Low
$\overline{\text{OUT2}}$	Reset	High
$\overline{\text{RTS}}$	Reset	High
$\overline{\text{DTR}}$	Reset	High
$\overline{\text{OUT1}}$	Reset	High

modem control register (MCR)

The MCR controls the interface with the modem or data set as described in Figure 20. MCR can be written and read. The $\overline{\text{RTS}}$ and $\overline{\text{DTR}}$ outputs are directly controlled by their control bits in this register. A high input asserts a low signal (active) at the output terminals. The MCR bits are shown in the following bulleted list.

- Bit 0: When MCR0 is set, the $\overline{\text{DTR}}$ output is forced low. When MCR0 is cleared, the $\overline{\text{DTR}}$ output is forced high. The $\overline{\text{DTR}}$ output of the serial channel can be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.
- Bit 1: When MCR1 is set, the $\overline{\text{RTS}}$ output is forced low. When MCR1 is cleared, the $\overline{\text{RTS}}$ output is forced high. The $\overline{\text{RTS}}$ output of the serial channel can be input into an inverting line driver to obtain the proper polarity input at the modem or data set.
- Bit 2: MCR2 has no affect on operation.
- Bit 3: When MCR3 is set, the external serial channel interrupt is enabled.
- Bit 4: MCR4 provides a local loopback feature for diagnostic testing of the channel. When MCR4 is set, SOUT is set to the marking (high) state and the SIN is disconnected. The output of the transmitter shift register is looped back into the receiver shift register input. The four modem control inputs ($\overline{\text{CTS}}$, $\overline{\text{DSR}}$, $\overline{\text{DCD}}$, and $\overline{\text{RI}}$) are disconnected. The modem control outputs ($\overline{\text{DTR}}$, $\overline{\text{RTS}}$, $\overline{\text{OUT1}}$, and $\overline{\text{OUT2}}$) are internally connected to the four modem control inputs. The modem control output terminals are forced to their inactive (high) state on the TL16C552AI. In the diagnostic mode, data transmitted is immediately received. This allows the processor to verify the transmit and receive data paths of the selected serial channel. Interrupt control is fully operational; however, interrupts are generated by controlling the lower four MCR bits internally. Interrupts are not generated by activity on the external terminals represented by those four bits.

PRINCIPLES OF OPERATION

modem control register (MCR) (continued)

- Bits 5 – 7: MCR5 – MCR7 are permanently cleared.

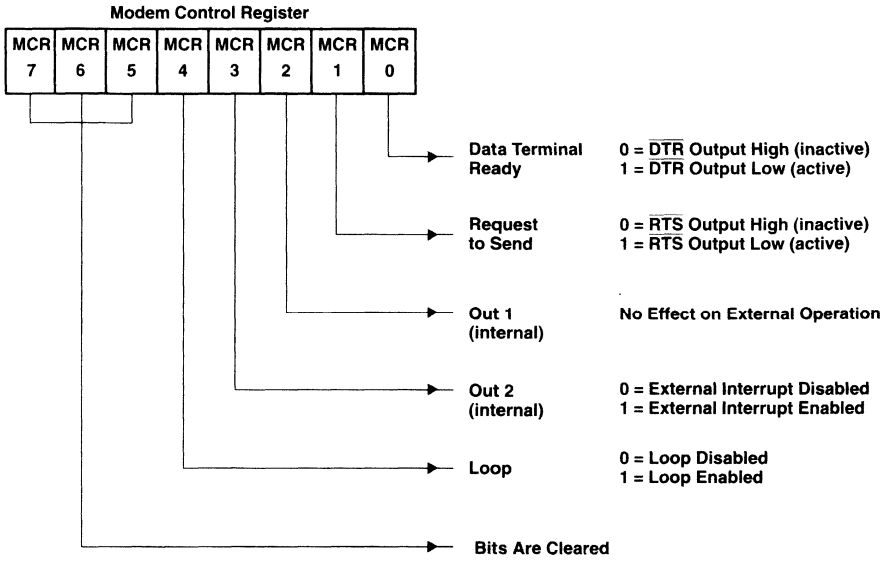


Figure 20. Modem Control Register Contents

modem status register (MSR)

The MSR provides the CPU with status of the modem input lines from the modem or peripheral devices. The MSR allows the CPU to read the serial channel modem signal inputs. This is done by accessing the data bus interface of the ACE in addition to the current status of four bits of the MSR. These four bits indicate whether the modem inputs have changed since the last reading of the MSR. The delta status bits are set when a control input from the modem changes state and is cleared when the CPU reads the MSR.

The modem input lines are $\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$, and $\overline{DCD}$. MSR4 – MSR7 are status indicators of these lines. A set status bit indicates that the input is low. A cleared status bit indicates that the input is high. When the modem status interrupt in the interrupt enable register is enabled (IER3), an interrupt is generated whenever MSR0 – MSR3 is set. The MSR is a priority-4 interrupt. The contents of the MSR are described in Table 11.

- Bit 0: MSR0 is the delta clear-to-send (ΔCTS) bit. ΔCTS displays that the $\overline{CTS}$ input to the serial channel has changed states since it was last read by the CPU.
- Bit 1: MSR1 is the delta data set ready (ΔDSR) bit. ΔDSR indicates that the $\overline{DSR}$ input to the serial channel has changed states since the last time it was read by the CPU.
- Bit 2: MSR2 is the trailing edge of ring indicator (TERI) bit. TERI indicates that the $\overline{RI}$ input to the serial channel has changed states from low to high since the last time it was read by the CPU. High-to-low transitions on RI do not activate TERI.

PRINCIPLES OF OPERATION

modem status register (MSR) (continued)

- Bit 3: MSR3 is the delta data carrier detect (ΔDCD) bit. ΔDCD indicates that the $\overline{DCD}$ input to the serial channel has changed states since the last time it was read by the CPU.
- Bit 4: MSR4 is the clear-to-send (CTS) bit. CTS is the complement of the $\overline{CTS}$ input from the modem indicating to the serial channel that the modem is ready to receive data from SOUT. When the serial channel is in the loop mode (MCR4 is set), MSR4 reflects the value of RTS in the MCR.
- Bit 5: MSR5 is the data set ready (DSR) bit. DSR is the complement of the $\overline{DSR}$ input from the modem to the serial channel that indicates that the modem is ready to provide received data to the serial channel receiver circuitry. When the channel is in the loop mode (MCR4 is set), MSR5 reflects the value of DTR in the MCR.
- Bit 6: MSR6 is the ring indicator (RI) bit. RI is the complement of the $\overline{RI}$ input. When the channel is in the loop mode (MCR4 is set), MSR6 reflects the value of $\overline{OUT1}$ in the MCR.
- Bit 7: MSR7 is the data carrier detect (DCD) bit. Data carrier detect indicates the status of the data carrier detect ($\overline{DCD}$) input. When the channel is in the loop mode (MCR4 is set), MSR7 reflects the value of OUT2 in the MCR.

  Reading the MSR register clears the delta modem status indicators but has no affect on the other status bits. For LSR and MSR, the setting of status bits is inhibited during status register read operations. If a status condition is generated during a read $\overline{IOR}$ operation, the status bit is not set until the trailing edge of the read. When a status bit is set during a read operation and the same status condition occurs, that status bit is cleared at the trailing edge of the read instead of being set again. In the loop back mode, when modem status interrupts are enabled, the $\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$ and $\overline{DCD}$ input terminals are ignored; however, a modem status interrupt can still be generated by writing to MCR3–MCR0. Applications software should not write to the MSR.

Table 11. Modem Status Register Bits

MSR BIT	MNEMONIC	DESCRIPTION
MSR0	ΔCTS	Delta clear to send
MSR1	ΔDSR	Delta data set ready
MSR2	TERI	Trailing edge of ring indicator
MSR3	ΔDCD	Delta data carrier detect
MSR4	CTS	Clear to send
MSR5	DSR	Data set ready
MSR6	RI	Ring indicator
MSR7	DCD	Data carrier detect

PRINCIPLES OF OPERATION

parallel port registers

The TL16C552AI parallel port can connect the device to a Centronics-style printer interface. When chip select 2 ($\overline{CS2}$) is low, the parallel port is selected. Table 13 shows the registers associated with this parallel port. The read or write function of the register is controlled by the state of the read ($\overline{IOR}$) and write ($\overline{IOW}$) terminals as shown. The read data register allows the microprocessor to read the information on the parallel bus.

The read status register allows the microprocessor to read the status of the printer in the six most significant bits. The status bits are printer busy ($\overline{BSY}$, acknowledge ($\overline{ACK}$) (a handshake function), paper empty (PE), printer selected ($\overline{SLCT}$), error ($\overline{ERR}$) and printer interrupt ($\overline{PRINT}$). The read control register allows the state of the control lines to be read. The write control register sets the state of the control lines. They are direction (DIR), interrupt enable (INT2 EN), select in ($\overline{SLIN}$), initialize the printer ($\overline{INIT}$), autofeed the paper ($\overline{AFD}$), and strobe ($\overline{STB}$), which informs the printer of the presence of a valid byte on the parallel bus. The write data register allows the microprocessor to write a byte to the parallel bus. The parallel port is completely compatible with the parallel port implementation used in the IBM serial parallel adaptor.

Table 12. Parallel Port Registers

REGISTER	REGISTER BITS							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Read data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Read status	$\overline{BSY}$	$\overline{ACK}$	PE	SLCT	$\overline{ERR}$	$\overline{PRINT}$	1	1
Read control	0	0	PEMD • DIR	INT2 EN	SLIN	$\overline{INIT}$	AFD	STB
Write data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Write control	0	0	DIR	INT2 EN	SLIN	$\overline{INIT}$	AFD	STB

Table 13. Parallel Port Register Select

CONTROL PINS					REGISTER SELECTED
$\overline{IOR}$	$\overline{IOW}$	$\overline{CS2}$	A1	A0	
L	H	L	L	L	Read data
L	H	L	L	H	Read status
L	H	L	H	L	Read control
L	H	L	H	H	Invalid
H	L	L	L	L	Write data
H	L	L	L	H	Invalid
H	L	L	H	L	Write control
H	L	L	H	H	Invalid

programmable baud rate generator

The ACE serial channel contains a programmable baud rate generator (BRG) that divides the clock (dc to 8 MHz) by any divisor from 1 to ($2^{16}-1$). The output frequency of the baud generator is 16x the data rate [divisor # = clock ÷ (baud rate x 16)] referred to in this document as RCLK. Two 8-bit divisor latch registers store the divisor in a 16-bit binary format. These divisor latch registers must be loaded during initialization. Upon loading either of the divisor latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load. The BRG can use any of three different popular frequencies to provide standard baud rates. These frequencies are 1.8432 MHz, 3.072 MHz, and 8 MHz. With these frequencies, standard bit rates from 50 to 512 kbps are available. Tables 14, 15, 16, and 17 illustrate the divisors needed to obtain standard rates using these three frequencies.

PRINCIPLES OF OPERATION

programmable baud rate generator (continued)

Table 14. Baud Rates Using a 1.8432-MHz Crystal

BAUD RATE DESIRED	DIVISOR (N) USED TO GENERATE 16x CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	–
75	1536	–
110	1047	0.026
134.5	857	0.058
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.690
2400	48	–
3600	32	–
4800	24	–
7200	16	–
9600	12	–
19200	6	–
38400	3	–
56000	2	2.860

Table 15. Baud Rates Using a 3.072-MHz Crystal

BAUD RATE DESIRED	DIVISOR (N) USED TO GENERATE 16x CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	–
75	2560	–
110	1745	0.026
134.5	1428	0.034
150	1280	–
300	640	–
600	320	–
1200	160	–
1800	107	0.312
2000	96	–
2400	80	–
3600	53	0.628
4800	40	–
7200	27	1.230
9600	20	–
19200	10	–
38400	5	–

PRINCIPLES OF OPERATION

programmable baud rate generator (continued)

Table 16. Baud Rates Using a 8-MHz Clock

BAUD RATE DESIRED	DIVISOR (N) USED TO GENERATE 16x CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	10000	–
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	3333	0.010
300	1667	0.020
600	833	0.040
1200	417	0.080
1800	277	0.080
2000	250	–
2400	208	0.160
3600	139	0.080
4800	104	0.160
7200	69	0.644
9600	52	0.160
19200	26	0.160
38400	13	0.160
56000	9	0.790
128000	4	2.344
256000	2	2.344
512000	1	2.400

Table 17. Baud Rates Using a 16-MHz Clock

BAUD RATE DESIRED	DIVISOR (N) USED TO GENERATE 16x CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	20000	0.00
75	13334	0.00
110	9090	0.01
134.5	7434	0.01
150	6666	0.01
300	3334	−0.02
600	1666	0.04
1200	834	−0.08
1800	554	0.28
2000	500	0.00
2400	416	0.16
3600	278	−0.08
4800	208	0.16
7200	138	0.64
9600	104	0.16
19200	52	0.16
38400	26	0.16
56000	18	−0.79
128000	8	−2.34
256000	4	−2.34
512000	2	−2.34
1000000	1	0.00

PRINCIPLES OF OPERATION

programming

The serial channel of the ACE is programmed by the control registers: LCR, IER, DLL, DLM, MCR, and FCR. These control words define the character length, number of stop bits, parity, baud rate, and modem interface.

While the control registers can be written in any order, the IER should be written last because it controls the interrupt enables. Once the serial channel is programmed and operational, these registers can be updated any time the ACE serial channel is not transmitting or receiving data.

receiver

Serial asynchronous data is input into SIN. The ACE continually searches for a high-to-low transition from the idle state. When the transition is detected, a counter is reset and counts the 16× clock to 7 1/2, which is the center of the start bit. The start bit is valid if SIN is still low. Verifying the start bits prevents the receiver from assembling a false data character due to a low-going noise spike on the SIN input.

The LCR determines the number of data bits in a character (LCR0 and LCR1). When parity is used, LCR3 and the polarity of parity LCR4 is needed. Status for the receiver is provided in the LSR. When a full character is received, including parity and stop bits, the data received indicator in LSR0 is set. The CPU reads the receiver buffer register, which clears LSR0. If the character is not read prior to a new character transfer from the RSR to the RBR, the overrun error status indicator is set in LSR1. If there is a parity error, the parity error is set in LSR2. If a stop bit is not detected, a framing error indicator is set in LSR3.

If the data into SIN is a symmetrical square wave, the center of the data cells occurs within ±3.125% of the actual center, providing an error margin of 46.875%. The start bit can begin as much as one 16× clock cycle prior to being detected.

scratchpad register

The scratch register is an 8-bit read/write register that has no affect on either channel in the ACE. It is intended to be used by the programmer to hold data temporarily.

SLLS165B – JANUARY 1994 – REVISED MARCH 1996

- **Integrated Asynchronous Communications Element**
- **Consists of Four Improved TL16C550 ACEs Plus Steering Logic**
- **In FIFO Mode, Each ACE Transmitter and Receiver Is Buffered With 16-Byte FIFO to Reduce the Number of Interrupts to CPU**
- **In TL16C450 Mode, Hold and Shift Registers Eliminate Need for Precise Synchronization Between the CPU and Serial Data**
- **Up to 16-MHz Clock Rate for up to 1-Mbaud Operation**
- **Programmable Baud Rate Generators Allow Division of Any Input Reference Clock by 1 to ($2^{16}-1$) and Generates Internal 16 × Clock**
- **Adds or Deletes Standard Asynchronous Communication Bits (Start, Stop, and Parity) to or From the Serial Data Stream**
- **Independently Controlled Transmit, Receive, Line Status, and Data Set Interrupts**
- **Fully Programmable Serial Interface Characteristics:**
  - **5-, 6-, 7-, or 8-Bit Characters**
  - **Even-, Odd-, or No-Parity Bit**
  - **1-, 1 1/2-, or 2-Stop Bit Generation**
  - **Baud Generation (DC to 256 Kilobits Per Second)**
- **False Start Bit Detection**
- **Complete Status Reporting Capabilities**
- **Line Break Generation and Detection**
- **Internal Diagnostic Capabilities:**
  - **Loopback Controls for Communications Link Fault Isolation**
  - **Break, Parity, Overrun, Framing Error Simulation**
- **Fully Prioritized Interrupt System Controls**
- **Modem Control Functions ($\overline{\text{CTS}}$, $\overline{\text{RTS}}$, $\overline{\text{DSR}}$, $\overline{\text{DTR}}$, $\overline{\text{RI}}$, and $\overline{\text{DCD}}$)**
- **3-State Outputs Provide TTL Drive Capabilities for Bidirectional Data Bus and Control Bus**

description

The TL16C554 is an enhanced quadruple version of the TL16C550B asynchronous communications element (ACE). Each channel performs serial-to-parallel conversion on data characters received from peripheral devices or modems and parallel-to-serial conversion on data characters transmitted by the CPU. The complete status of each channel of the quadruple ACE can be read at any time during functional operation by the CPU. The information obtained includes the type and condition of the operation performed and any error conditions encountered.

The TL16C554 quadruple ACE can be placed in an alternate FIFO mode, which activates the internal FIFOs to allow 16 bytes (plus 3 bits of error data per byte in the receiver FIFO) to be stored in both receive and transmit modes. To minimize system overhead and maximize system efficiency, all logic is on the chip. Two terminal functions have been provided to allow signaling of direct memory access (DMA) transfers. Each ACE includes a programmable baud rate generator that can divide the timing reference clock input by a divisor between 1 and ($2^{16}-1$).

The TL16C554 is available in the 68-pin plastic-leaded chip-carrier (PLCC) FN package.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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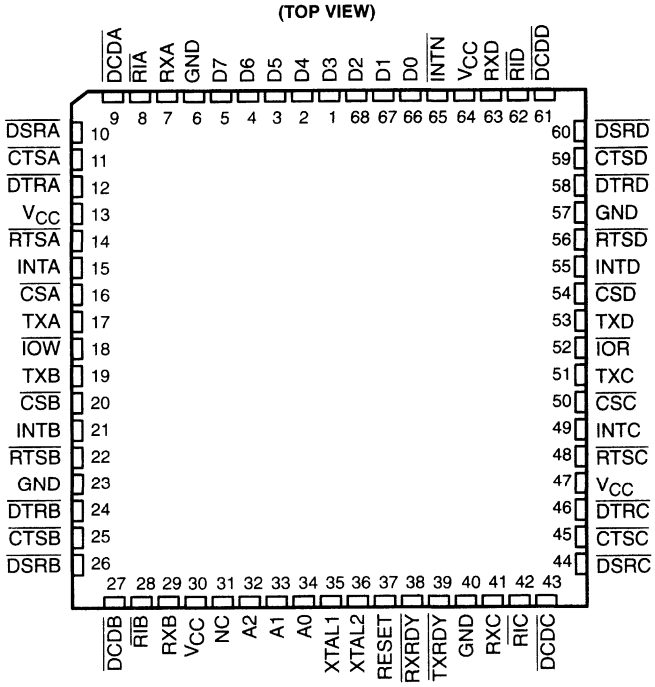
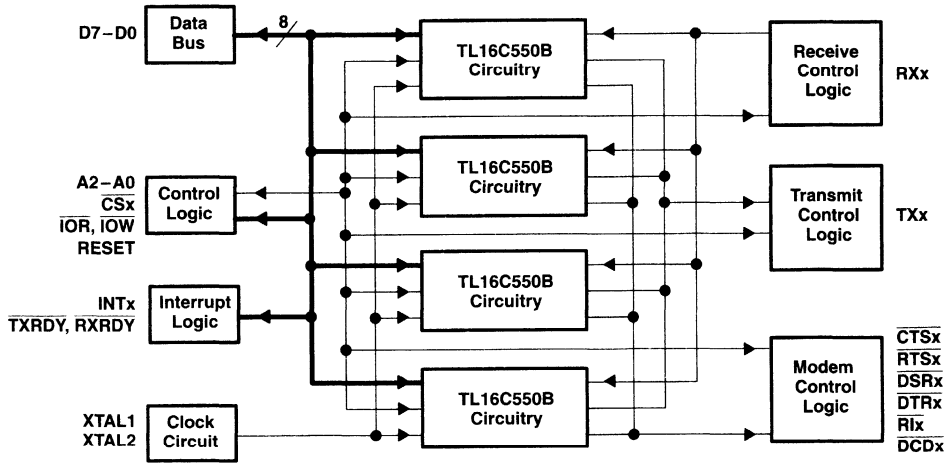
FN PACKAGE
(TOP VIEW)



NC – No internal connection

functional block diagram†



† For TL16C550 circuitry, refer to the TL16C550B data sheet.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
A0 A1 A2	34 33 32	I	Register select terminals. A0, A1, and A2 are three inputs used during read and write operations to select the ACE register to read or write.
$\overline{CSA}$, $\overline{CSB}$, $\overline{CSC}$, $\overline{CSD}$	16, 20, 50, 54	I	Chip select. Each chip select ($\overline{CSx}$) enables read and write operations to its respective channel.
$\overline{CTSA}$, $\overline{CTSB}$, $\overline{CTSC}$, $\overline{CTSD}$	11, 25, 45, 59	I	Clear to send. $\overline{CTSx}$ is a modem status signal. Its condition can be checked by reading bit 4 (CTS) of the modem status register. $\overline{CTS}$ has no affect on the transmit or receive operation.
D7–D0	66–68 1–5	I/O	Data bus. Eight data lines with 3-state outputs provide a bidirectional path for data, control and status information between the TL16C554 and the CPU. D0 is the least significant bit (LSB).
$\overline{DCDA}$, $\overline{DCDB}$, $\overline{DCDC}$, $\overline{DCDD}$	9, 27, 43, 61	I	Data carrier detect. A low on $\overline{DCDx}$ indicates the carrier has been detected by the modem. The condition of this signal is checked by reading bit 7 of the modem status register.
$\overline{DSRA}$, $\overline{DSRB}$, $\overline{DSRC}$, $\overline{DSRD}$	10, 26, 44, 60	I	Data set ready. $\overline{DSRx}$ is a modem status signal. Its condition can be checked by reading bit 5 (DSR) of the modem status register. $\overline{DSR}$ has no affect on the transmit or receive operation.
$\overline{DTRA}$, $\overline{DTRB}$, $\overline{DTRC}$, $\overline{DTRD}$	12, 24, 46, 58	O	Data terminal ready. $\overline{DTRx}$ is an output that indicates to a modem or data set that the ACE is ready to establish communications. It is placed in the active state by setting the DTR bit of the modem control register. $\overline{DTRx}$ is placed in the inactive state (high) either as a result of the master reset during loop mode operation or clearing bit 0 ($\overline{DTR}$) of the modem control register.
$\overline{INTN}$	65	I	Interrupt normal. $\overline{INTN}$ operates in conjunction with bit 3 of the modem status register and affects operation of the interrupts (INTA, INTB, INTC, and INTD) for the four universal asynchronous receiver/transceivers (UARTs) per the following table.
			$\overline{INTN}$ / **OPERATION OF INTERRUPTS** Brought low or allowed to float: Interrupts are enabled according to the state of OUT2 (MCR bit 3). When the MCR bit 3 is cleared, the 3-state interrupt output of that UART is in the high-impedance state. When the MCR bit 3 is set, the interrupt output of the UART is enabled. Brought high: Interrupts are always enabled, overriding the OUT2 enables.
GND	6, 23, 40, 57		Signal and power ground
INTA, INTB, INTC, INTD	15, 21, 49, 55	O	External interrupt output. The INTx outputs go high (when enabled by the interrupt register) and inform the CPU that the ACE has an interrupt to be serviced. Four conditions that cause an interrupt to be issued are: a receiver error, receiver data available or time out (FIFO mode only), transmitter holding register empty, and an enabled modem status interrupt. The interrupt is disabled when it is serviced or as the result of a master reset.
$\overline{IOR}$	52	I	Read strobe. A low level on $\overline{IOR}$ transfers the contents of the TL16C554 data bus to the external CPU bus.
$\overline{IOW}$	18	I	Write strobe. $\overline{IOW}$ allows the CPU to write into the selected by the address register.
RESET	37	I	Master reset. When active, RESET clears most ACE registers and sets the state of various signals. The transmitter output and the receiver input is disabled during reset time.
$\overline{RIA}$, $\overline{RIB}$, $\overline{RIC}$, $\overline{RID}$	8, 28, 42, 62	I	Ring detect indicator. A low on $\overline{RIx}$ indicates the modem has received a ring signal from the telephone line. The condition of this signal can be checked by reading bit 6 of the modem status register.
$\overline{RTSA}$, $\overline{RTSB}$, $\overline{RTSC}$, $\overline{RTSD}$	14, 22, 48, 56	O	Request to send. When active, $\overline{RTSx}$ informs the modem or data set that the ACE is ready to receive data. Writing a 1 in the modem control register sets this bit to a low state. After reset, this terminal is set high. These terminals have no affect on the transmit or receive operation.
RXA, RXB RXC, RXD	7, 29, 41, 63	I	Serial input. RXx is a serial data input from a connected communications device. During loopback mode, the RXx input is disabled from external connection and connected to the TXx output internally.
$\overline{RXRDY}$	38	O	Receive ready. $\overline{RXRDY}$ goes low when the receive FIFO is full. It can be used as a single transfer or multitransfer.
TXA, TXB TXC, TXD	17, 19, 51, 53	O	Transmit outputs. TXx is a composite serial data output that is connected to a communications device. TXA, TXB, TXC, and TXD are set to the marking (high) state as a result of reset.

Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{\text{TXRDY}}$	39	O	Transmit ready. $\overline{\text{TXRDY}}$ goes low when the transmit FIFO is full. It can be used as a single transfer or multitransfer function.
V_{CC}	13, 30, 47, 64		Power supply
XTAL1	35	I	Crystal input 1 or external clock input. A crystal can be connected to XTAL1 and XTAL2 to utilize the internal oscillator circuit. An external clock can be connected to drive the internal clock circuits.
XTAL2	36	O	Crystal output 2 or buffered clock output (see XTAL1).

absolute maximum ratings over free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Input voltage range at any input, V_I ..... −0.5 V to 7 V
Output voltage range, V_O ..... −0.5 V to V_{CC} + 3 V
Continuous total power dissipation at (or below) 70°C ..... 500 mW
Operating free-air temperature range, T_A ..... −0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage levels are with respect to GND.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Clock high-level input voltage at XTAL1, $V_{IH(CLK)}$	2		V_{CC}	V
Clock low-level input voltage at XTAL1, $V_{IL(CLK)}$	−0.5		0.8	V
High-level input voltage, V_{IH}	2		V_{CC}	V
Low-level input voltage, V_{IL}	−0.5		0.8	V
Clock frequency, f_{clock}			16	MHz
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}‡	High-level output voltage	I_{OH} = –1 mA	2.4			V
V_{OL}‡	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
I_{lkg}	Input leakage current	V_{CC} = 5.25 V, GND = 0, V_I = 0 to 5.25 V, All other terminals floating			±10	µA
I_{OZ}	High-impedance output current	V_{CC} = 5.25 V, GND = 0, V_O = 0 to 5.25 V, Chip selected in write mode or chip deselected			±20	µA
I_{CC}	Supply current	V_{CC} = 5.25 V, T_A = 25°C, RX, $\overline{DSR}$, $\overline{DCD}$, CTS, and $\overline{RI}$ at 2 V, All other inputs at 0.8 V, XTAL1 at 4 MHz, No load on outputs, Baud rate = 50 kilobits per second			50	mA
$C_{i(XTAL1)}$	Clock input capacitance	V_{CC} = 0, V_{SS} = 0, All other terminals grounded, f = 1 MHz, T_A = 25°C		15	20	pF
$C_{o(XTAL2)}$	Clock output capacitance			20	30	pF
C_i	Input capacitance			6	10	pF
C_o	Output capacitance			10	20	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ These parameters apply for all outputs except XTAL2.

clock timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 1)

		MIN	MAX	UNIT
t_{w1}	Pulse duration, clock high (external clock)	31		ns
t_{w2}	Pulse duration, clock low (external clock)	31		ns
t_{w3}	Pulse duration, RESET	1000		ns

read cycle timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 4)

		MIN	MAX	UNIT
t_{w4}	Pulse duration, $\overline{IOR}$ low	75		ns
t_{su1}	Setup time, $\overline{CSx}$ valid before $\overline{IOR}$ low (see Note 2)	10		ns
t_{su2}	Setup time, A2–A0 valid before $\overline{IOR}$ low (see Note 2)	15		ns
t_{h1}	Hold time, A2–A0 valid after $\overline{IOR}$ high (see Note 2)	0		ns
t_{h2}	Hold time, $\overline{CSx}$ valid after $\overline{IOR}$ high (see Note 2)	0		ns
t_{d1}	Delay time, $t_{su2} + t_{w4} + t_{d2}$ (see Note 3)	140		ns
t_{d2}	Delay time, $\overline{IOR}$ high to $\overline{IOR}$ or $\overline{IOW}$ low	50		ns

NOTES: 2. The internal address strobe is always active.
3. In the FIFO mode, t_{d1} = 425 ns (min) between reads of the receiver FIFO and the status registers (interrupt identification register and line status register).

write cycle timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 5)

		MIN	MAX	UNIT
t_{w5}	Pulse duration, $\overline{IOW}\downarrow$	50		ns
t_{su3}	Setup time, $\overline{CSx}$ valid before $\overline{IOW}\downarrow$ (see Note 2)	10		ns
t_{su4}	Setup time, A2–A0 valid before $\overline{IOW}\downarrow$ (see Note 2)	15		ns
t_{su5}	Setup time, D7–D0 valid before $\overline{IOW}\uparrow$	10		ns
t_{h3}	Hold time, A2–A0 valid after $\overline{IOW}\uparrow$ (see Note 2)	5		ns
t_{h4}	Hold time, $\overline{CSx}$ valid after $\overline{IOW}\uparrow$ (see Note 2)	5		ns
t_{h5}	Hold time, D7–D0 valid after $\overline{IOW}\uparrow$	25		ns
t_{d3}	Delay time, $t_{su4} + t_{w5} + t_{d4}$	120		ns
t_{d4}	Delay time, $\overline{IOW}\uparrow$ to $\overline{IOW}$ or $\overline{IOR}\downarrow$	55		ns

NOTE 2: The internal address strobe is always active.

read cycle switching characteristics over recommended ranges of operating free-air temperature and supply voltage, C_L = 100 pF (see Note 4 and Figure 4)

	PARAMETER	MIN	MAX	UNIT
t_{en}	Enable time, $\overline{IOR}\downarrow$ to D7–D0 valid		30	ns
t_{dis}	Disable time, $\overline{IOR}\uparrow$ to D7–D0 released	0	20	ns

NOTE 4: V_{OL} and V_{OH} (and the external loading) determine the charge and discharge time.

transmitter switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figures 6, 7, and 8)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{d5}	Delay time, INTx$\downarrow$ to TXx$\downarrow$ at start		8	24	RCLK cycles
t_{d6}	Delay time, TXx$\downarrow$ at start to INTx$\uparrow$	See Note 5	8	8	RCLK cycles
t_{d7}	Delay time, $\overline{IOW}$ high or low (WR THR) to INTx$\uparrow$	See Note 5	16	32	RCLK cycles
t_{d8}	Delay time, TXx$\downarrow$ at start to $\overline{TXRDY}\downarrow$	C_L = 100 pF		8	RCLK cycles
t_{pd1}	Propagation delay time, $\overline{IOW}$ (WR THR)$\downarrow$ to INTx$\downarrow$	C_L = 100 pF		35	ns
t_{pd2}	Propagation delay time, $\overline{IOR}$ (RD IIR)$\uparrow$ to INTx$\downarrow$	C_L = 100 pF		30	ns
t_{pd3}	Propagation delay time, $\overline{IOW}$ (WR THR)$\uparrow$ to $\overline{TXRDY}\uparrow$	C_L = 100 pF		50	ns

NOTE 5: If the transmitter interrupt delay is active, this delay is lengthened by one character time minus the last stop bit time.

receiver switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figures 9 through 13)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{d9}	Delay time, stop bit to INTx↑ or stop bit to $\overline{RXRDY}$↓ or read RBR to set interrupt	See Note 6		1	RCLK cycle
t_{pd4}	Propagation delay time, Read RBR/LSR to INTx↓/LSR interrupt↓	C_L = 100 pF, See Note 7		40	ns
t_{pd5}	Propagation delay time, $\overline{IOR}$ RCLK↓ to $\overline{RXRDY}$↑	See Note 7		30	ns

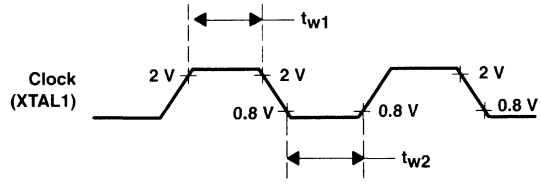
NOTES: 6. The receiver data available indicator, the overrun error indicator, the trigger level interrupts, and the active $\overline{RXRDY}$ indicator are delayed three RCLK (internal receiver timing clock) cycles in the FIFO mode (FCR0 = 1). After the first byte has been received, status indicators (PE, FE, BI) are delayed three RCLK cycles. These indicators are updated immediately for any further bytes received after $\overline{IOR}$ goes active for a read from the RBR register. There are eight RCLK cycle delays for trigger change level interrupts.

7. RCLK is an internal signal derived from divisor latch LSB (DLL) and divisor latch MSB (DLM) divisor latches.

modem control switching characteristics over recommended ranges of operating free-air temperature and supply voltage, C_L = 100 pF (see Figure 14)

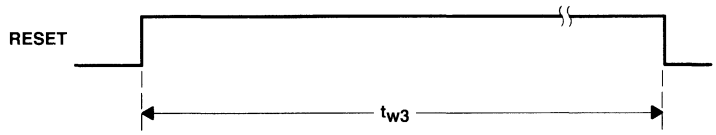
	PARAMETER	MIN	MAX	UNIT
t_{pd6}	Propagation delay time, $\overline{IOW}$ (WR MCR)↑ to $\overline{RTSx}$, $\overline{DTRx}$↑		50	ns
t_{pd7}	Propagation delay time, modem input $\overline{CTSx}$, $\overline{DSRx}$, and $\overline{DCDx}$ ↓↑ to INTx↑		30	ns
t_{pd8}	Propagation delay time, $\overline{IOR}$ (RD MSR)↑ to interrupt↓		35	ns
t_{pd9}	Propagation delay time, $\overline{RIx}$↑ to $\overline{INTx}$↑		30	ns

PARAMETER MEASUREMENT INFORMATION



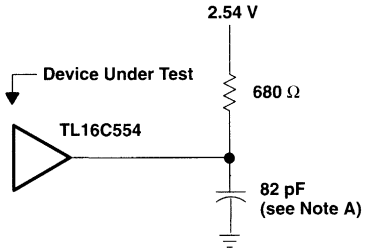
f_{clock} = 16 MHz MAX

(a) CLOCK INPUT VOLTAGE WAVEFORM



(b) RESET VOLTAGE WAVEFORM

Figure 1. Clock Input and RESET Voltage Waveforms



NOTE A: This includes scope and jig capacitance.

Figure 2. Output Load Circuit

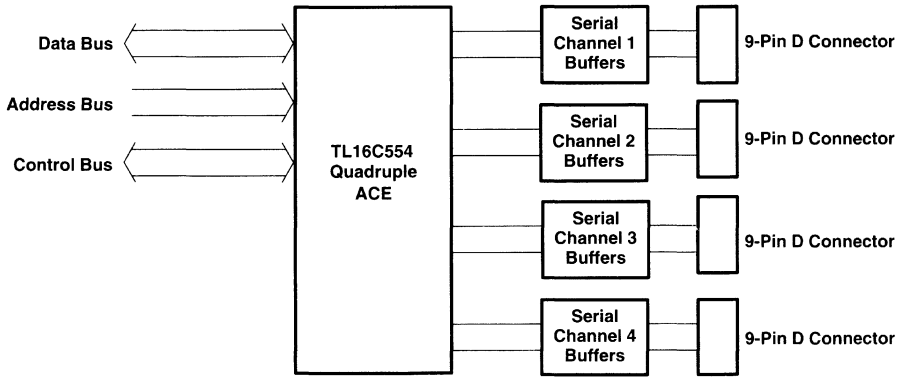


Figure 3. Basic Test Configuration

PARAMETER MEASUREMENT INFORMATION

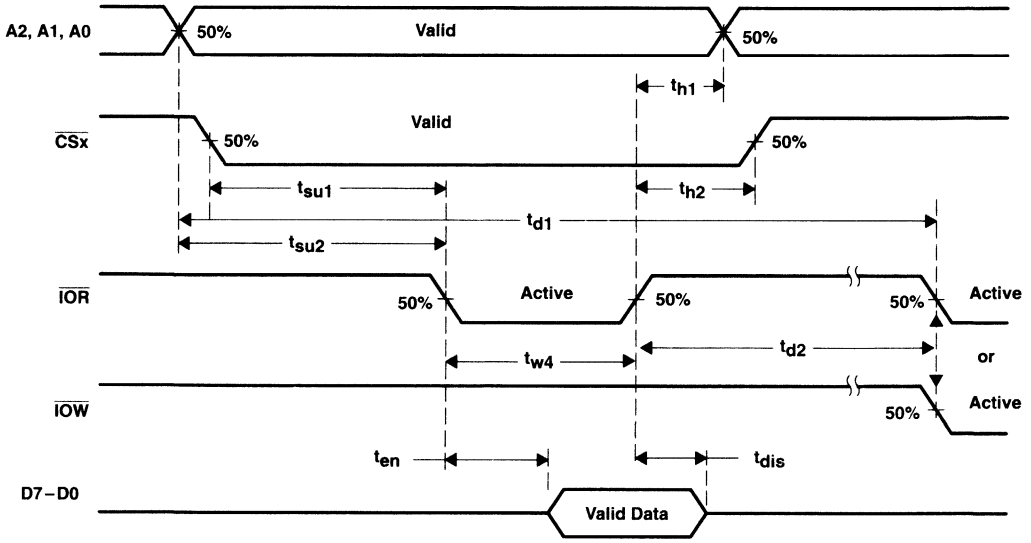


Figure 4. Read Cycle Timing Waveforms

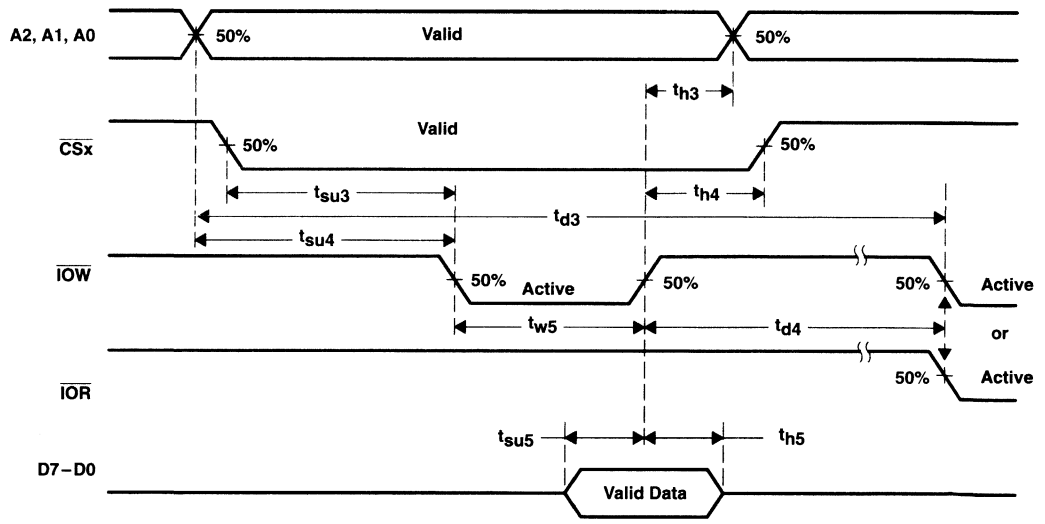


Figure 5. Write Cycle Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

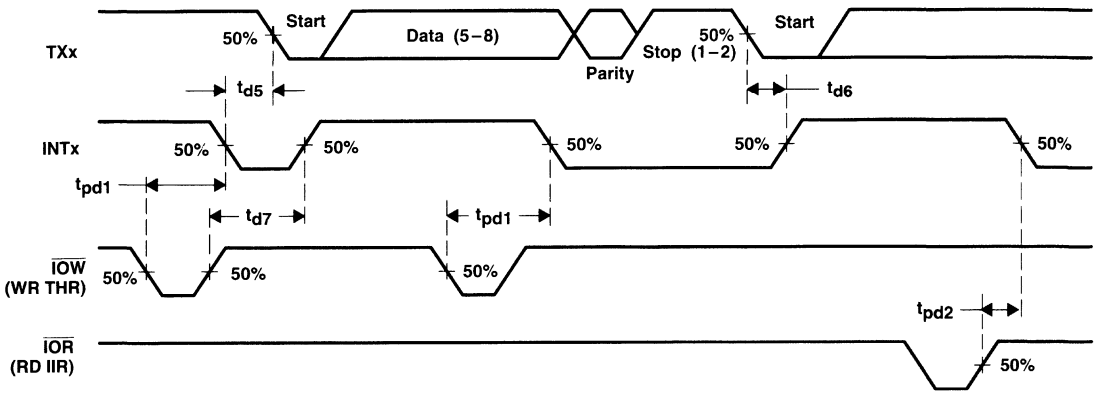


Figure 6. Transmitter Timing Waveforms

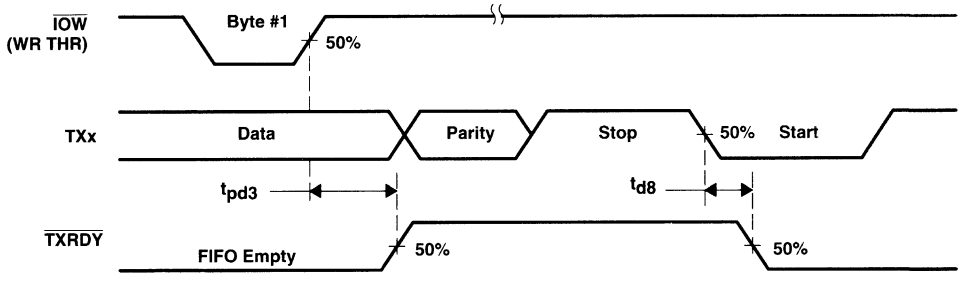


Figure 7. Transmitter Ready Mode 0 Timing Waveforms

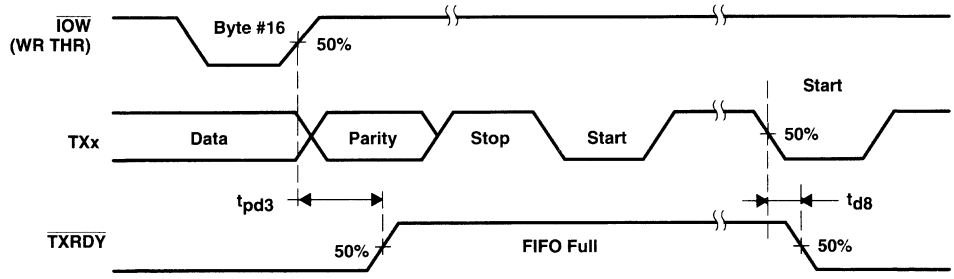


Figure 8. Transmitter Ready Mode 1 Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

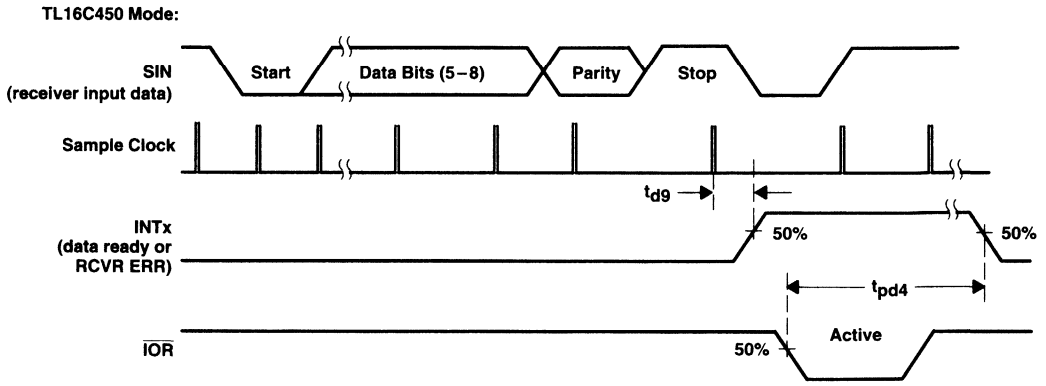


Figure 9. Receiver Timing Waveforms

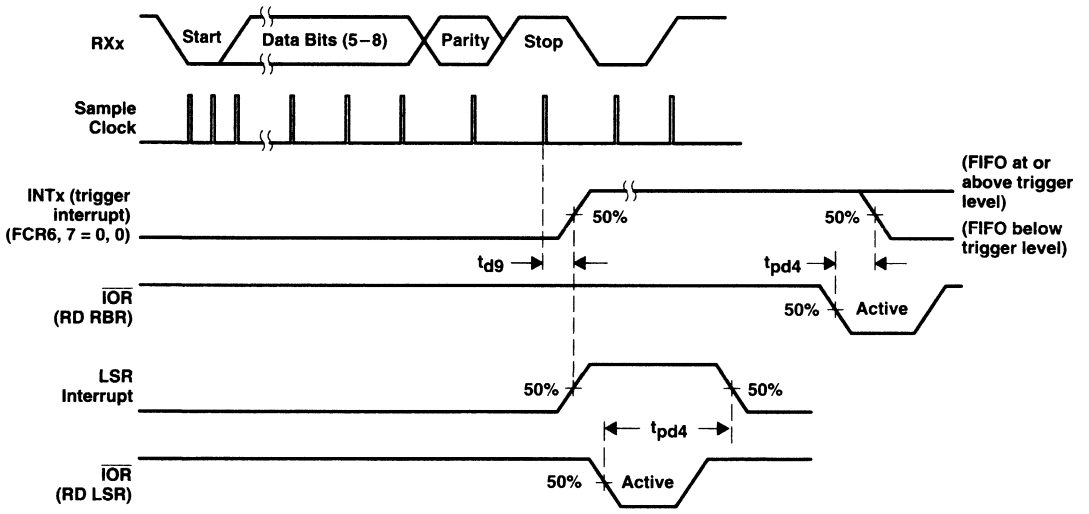
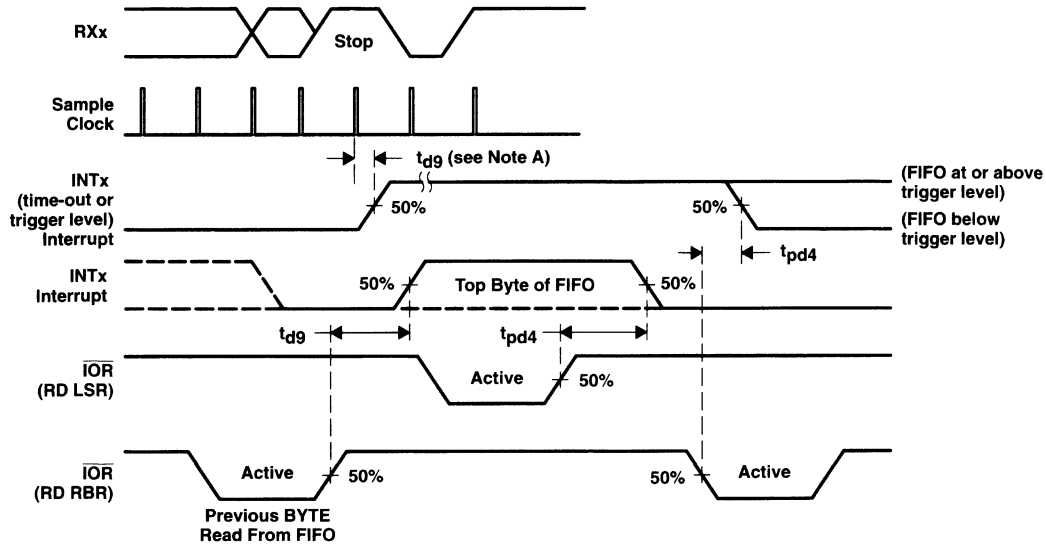


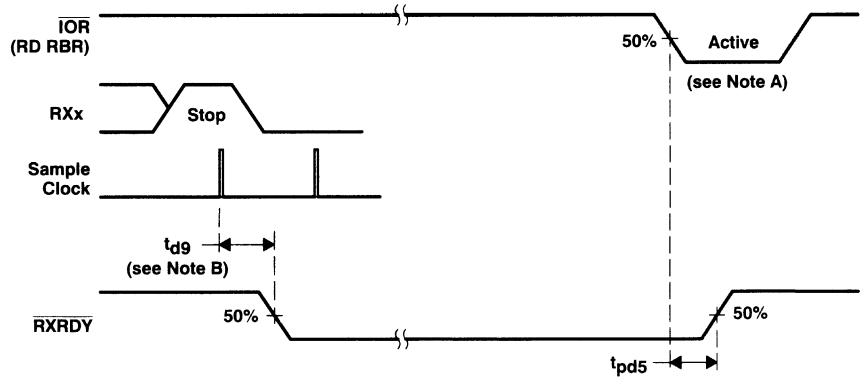
Figure 10. Receiver FIFO First Byte (Sets RDR) Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: This is the reading of the last byte in the FIFO.

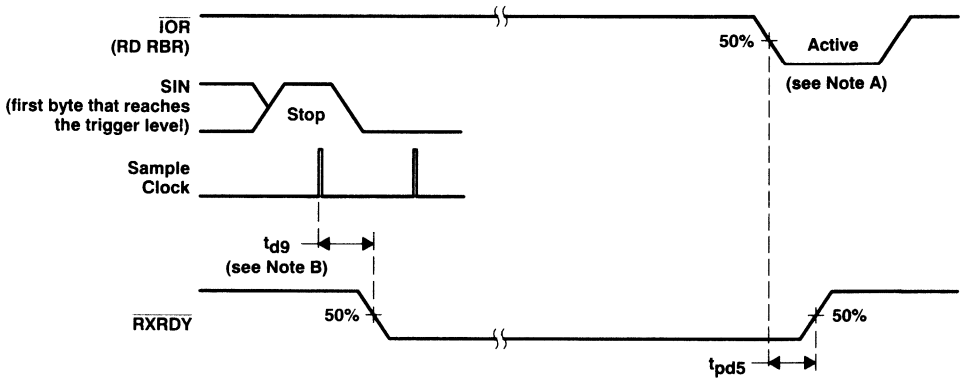
Figure 11. Receiver FIFO After First Byte (After RDR Set) Waveforms



NOTES: B. This is the reading of the last byte in the FIFO.
C. If FCR0 = 1, then t_{d9} = 3 RCLK cycles. For a time-out interrupt, t_{d9} = 8 RCLK cycles.

Figure 12. Receiver Ready Mode 0 Timing Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. This is the reading of the last byte in the FIFO.
B. If FCR0 = 1, t_{d9} = 3 RCLK cycles. For a trigger change level interrupt, t_{d9} = 8 RCLK.

Figure 13. Receiver Ready Mode 1 Timing Waveforms

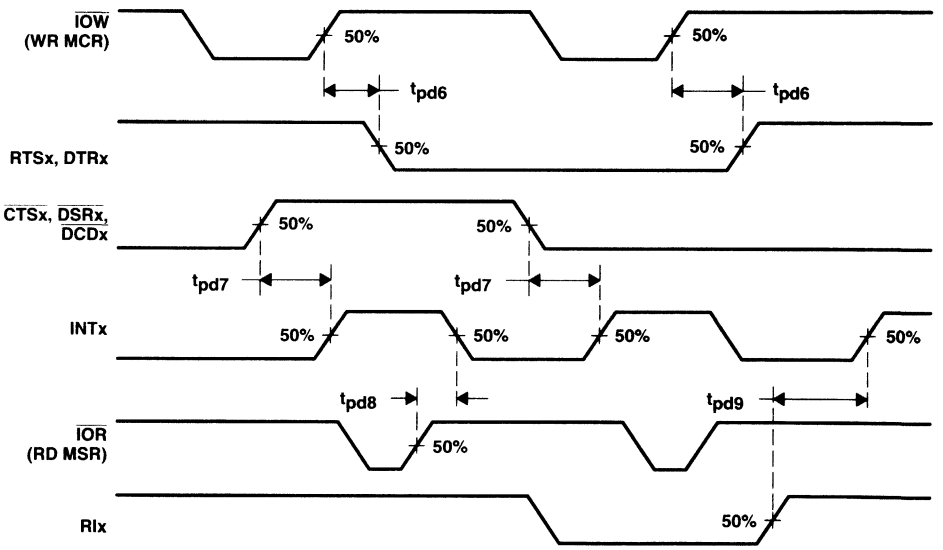


Figure 14. Modem Control Timing Waveforms

PRINCIPLES OF OPERATION

Three types of information are stored in the internal registers used in the ACE: control, status, and data. Mnemonic abbreviations for the registers are shown in Table 1. Table 2 defines the address location of each register and whether it is read only, write only, or read writable.

Table 1. Internal Register Mnemonic Abbreviations

CONTROL	MNEMONIC	STATUS	MNEMONIC	DATA	MNEMONIC
Line control register	LCR	Line status register	LSR	Receiver buffer register	RBR
FIFO control register	FCR	Modem status register	MSR	Transmitter holding register	THR
Modem control register	MCR				
Divisor latch LSB	DLL				
Divisor latch MSB	DLM				
Interrupt enable register	IER				

Table 2. Register Selection†

DLAB‡	A2§	A1§	A0§	READ MODE	WRITE MODE
0	0	0	0	Receiver buffer register	Transmitter holding register
0	0	0	1		Interrupt enable register
X	0	1	0	Interrupt identification register	FIFO control register
X	0	1	1		Line control register
X	1	0	0		Modem control register
X	1	0	1	Line status register	
X	1	1	0	Modem status register	
X	1	1	1	Scratchpad register	Scratchpad register
1	0	0	0		LSB divisor latch
1	0	0	1		MSB divisor latch

X = irrelevant, 0 = low level, 1 = high level
† The serial channel is accessed when either $\overline{CSA}$ or $\overline{CSD}$ is low.
‡ DLAB is the divisor latch access bit and bit 7 in the LCR.
§ A2–A0 are device terminals.

Individual bits within the registers are referred to by the register mnemonic and the bit number in parentheses. For example, LCR7 refers to line control register bit 7. The transmitter buffer register and receiver buffer register are data registers that hold from five to eight bits of data. If less than eight data bits are transmitted, data is right justified to the LSB. Bit 0 of a data word is always the first serial data bit received and transmitted. The ACE data registers are double buffered (TL16450 mode) or FIFO buffered (FIFO mode) so that read and write operations can be performed when the ACE is performing the parallel-to-serial or serial-to-parallel conversion.

PRINCIPLES OF OPERATION

accessible registers

The system programmer, using the CPU, has access to and control over any of the ACE registers that are summarized in Table 1. These registers control ACE operations, receive data, and transmit data. Descriptions of these registers follow Table 3.

Table 3. Summary of Accessible Registers

ADDRESS	REGISTER MNEMONIC	REGISTER ADDRESS							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	RBR (read only)	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)
0	THR (write only)	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
0†	DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1†	DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
1	IER	0	0	0	0	(EDSSI) Enable modem status interrupt	(ERLSI) Enable receiver line status interrupt	(ETBEI) Enable transmitter holding register empty interrupt	(ERBI) Enable received data available interrupt
2	FCR (write only)	Receiver Trigger (MSB)	Receiver Trigger (LSB)	Reserved	Reserved	DMA mode select	Transmit FIFO reset	Receiver FIFO reset	FIFO Enable
2	IIR (read only)	FIFOs Enabled‡	FIFOs Enabled‡	0	0	Interrupt ID Bit (3)‡	Interrupt ID Bit (2)	Interrupt ID Bit (1)	0 If interrupt pending
3	LCR	(DLAB) Divisor latch access bit	Set break	Stick parity	(EPS) Even parity select	(PEN) Parity enable	(STB) Number of stop bits	(WLSB1) Word length select bit 1	(WLSB0) Word length select bit 0
4	MCR	0	0	0	Loop	OUT2 Enable external interrupt (INT)	Reserved	(RTS) Request to send	(DTR) Data terminal ready
5	LSR	Error in receiver FIFO‡	(TEMT) Transmitter registers empty	(THRE) Transmitter holding register empty	(BI) Break interrupt	(FE) Framing error	(PE) Parity error	(OE) Overrun error	(DR) Data ready
6	MSR	(DCD) Data carrier detect	(RI) Ring indicator	(DSR) Data set ready	(CTS) Clear to send	(ΔDCD) Delta data carrier detect	(TERI) Trailing edge ring indicator	(ΔDSR) Delta data set ready	(ΔCTS) Delta clear to send
7	SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

† DLAB = 1
‡ These bits are always 0 when FIFOs are disabled.

PRINCIPLES OF OPERATION

FIFO control register (FCR)

The FCR is a write-only register at the same location as the IIR. It enables the FIFOs, sets the trigger level of the receiver FIFO, and selects the type of DMA signalling.

- Bit 0: FCR0 enables the transmit and receiver FIFOs. All bytes in both FIFOs can be cleared by clearing FCR0. Data is cleared automatically from the FIFOs when changing from the FIFO mode to the TL16C450 mode (see FCR bit 0) and vice versa. Programming of other FCR bits is enabled by setting FCR0.
- Bit 1: When set, FCR1 clears all bytes in the receiver FIFO and resets its counter. This does not clear the shift register.
- Bit 2: When set, FCR2 clears all bytes in the transmit FIFO and resets the counter. This does not clear the shift register.
- Bit 3: When set, FCR3 changes $\overline{\text{RXRDY}}$ and $\overline{\text{TXRDY}}$ from mode 0 to mode 1 if FCR0 is set.
- Bits 4 and 5: FCR4 and FCR5 are reserved for future use.
- Bits 6 and 7: FCR6 and FCR7 sets the trigger level for the receiver FIFO interrupt (see Table 4).

Table 4. Receiver FIFO Trigger Level

BIT		RECEIVER FIFO TRIGGER LEVEL (BYTES)
7	6	
0	0	01
0	1	04
1	0	08
1	1	14

FIFO interrupt mode operation

The following receiver status occurs when the receiver FIFO and receiver interrupts are enabled.

1. LSR0 is set when a character is transferred from the shift register to the receiver FIFO. When the FIFO is empty, it is reset.
2. IIR = 06 receiver line status interrupt has higher priority than the receive data available interrupt IIR = 04.
3. Receive data available interrupt is issued to the CPU when the programmed trigger level is reached by the FIFO. As soon as the FIFO drops below its programmed trigger level, it is cleared.
4. IIR = 04 (receive data available indicator) also occurs when the FIFO reaches its trigger level. It is cleared when the FIFO drops below the programmed trigger level.

The following receiver FIFO character time-out status occurs when receiver FIFO and receiver interrupts are enabled.

PRINCIPLES OF OPERATION

FIFO interrupt mode operation (continued)

1. When the following conditions exist, a FIFO character time-out interrupt occurs:
   a. Minimum of one character in FIFO
   b. Last received serial character is longer than four continuous previous character times ago. (If two stop bits are programmed, the second one is included in the time delay.)
   c. The last CPU read of the FIFO is more than four continuous character times earlier. At 300 baud and 12-bit characters, the FIFO time-out interrupt causes a latency of 160 ms maximum from received character to interrupt issued.
2. By using the XTAL1 input for a clock signal, the character times can be calculated. The delay is proportional to the baud rate.
3. The time-out timer is reset after the CPU reads the receiver FIFO or after a new character is received. This occurs when there has been no time-out interrupt.
4. A time-out interrupt is cleared and the timer is reset when the CPU reads a character from the receiver FIFO.

Transmit interrupts occurs as follows when the transmitter and transmit FIFO interrupts are enabled (FCR0 = 1, IER = 1).

1. When the transmitter FIFO is empty, the transmitter holding register interrupt (IIR = 02) occurs. The interrupt is cleared when the transmitter holding register is written to or the IIR is read. One to sixteen characters can be written to the transmit FIFO when servicing this interrupt.
2. The transmitter FIFO empty indicators are delayed one character time minus the last stop bit time whenever the following occurs:

   THRE = 1, and there has not been a minimum of two bytes at the same time in transmit FIFO since the last THRE = 1. The first transmitter interrupt after changing FCR0 is immediate, however, assuming it is enabled.

Receiver FIFO trigger level and character time-out interrupts have the same priority as the receive data available interrupt. The transmitter holding register empty interrupt has the same priority as the transmitter FIFO empty interrupt.

FIFO polled mode operation

Clearing IER0, IER1, IER2, IER3, or all to zero with FCR0 = 1 puts the ACE into the FIFO polled mode. receiver and transmitter are controlled separately. Either or both can be in the polled mode.

In the FIFO polled mode, there is no time-out condition indicated or trigger level reached. However, the receiver and transmit FIFOs still have the capability of holding characters. The LSR must be read to determine the ACE status.

interrupt enable register (IER)

The IER independently enables the four serial channel interrupt sources that activate the interrupt (INTA, B, C, D) output. All interrupts are disabled by clearing IER0 – IER3 of the IER. Interrupts are enabled by setting the appropriate bits of the IER. Disabling the interrupt system inhibits the IIR and the active (high) interrupt output. All other system functions operate in their normal manner, including the setting of the LSR and MSR. The contents of the IER are shown in Table 3 and described in the following bulleted list.

PRINCIPLES OF OPERATION

interrupt enable register (IER) (continued)

- Bit 0: When IER0 is set, IER0 enables the received data available interrupt and the time-out interrupts in the FIFO mode.
- Bit 1: When IER1 is set, the transmitter holding register empty interrupt is enabled.
- Bit 2: When IER2 is set, the receiver line status interrupt is enabled.
- Bit 3: When IER3 is set, the modem status interrupt is enabled.
- Bits 4 – 7: IER4 – IER7. These four bits of the IER are cleared.

interrupt identification register (IIR)

In order to minimize software overhead during data character transfers, the serial channel prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows:

- Priority 1 – Receiver line status (highest priority)
- Priority 2 – Receiver data ready or receiver character time out
- Priority 3 – Transmitter holding register empty
- Priority 4 – Modem status (lowest priority)

Information indicating that a prioritized interrupt is pending and the type of interrupt that is stored in the IIR. The IIR indicates the highest priority interrupt pending. The contents of the IIR are indicated in Table 5.

Table 5. Interrupt Control Functions

INTERRUPT IDENTIFICATION REGISTER				INTERRUPT SET AND RESET FUNCTIONS			
BIT 3	BIT 2	BIT 1	BIT 0	PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET CONTROL
0	0	0	1	—	None	None	—
0	1	1	0	First	Receiver line status	OE, PE, FE, or BI	LSR read
0	1	0	0	Second	Received data available	Receiver data available or trigger level reached	RBR read until FIFO drops below the trigger level
1	1	0	0	Second	Character time-out indicator	No characters have been removed from or input to the receiver FIFO during the last four character times, and there is at least one character in it during this time.	RBR read
0	0	1	0	Third	THRE	THRE	IIR read if THRE is the interrupt source or THR write
0	0	0	0	Fourth	Modem status	$\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$, or $\overline{DCD}$	

PRINCIPLES OF OPERATION

interrupt identification register (IIR) (continued)

- Bit 0: IIR0 indicates whether an interrupt is pending. When IIR0 is cleared, an interrupt is pending.
- Bits 1 and 2: IIR1 and IIR2 identify the highest priority interrupt pending as indicated in Table 5.
- Bit 3: IIR3 is always cleared when in the TL16C450 mode. This bit is set along with bit 2 when in the FIFO mode and a trigger change level interrupt is pending.
- Bits 4 and 5: IIR4 and IIR5 are always cleared.
- Bits 6 and 7: IIR6 and IIR7 are set when FCR0 = 1.

line control register (LCR)

The format of the data character is controlled by the LCR. The LCR may be read. Its contents are described in the following bulleted list and shown in Figure 15.

- Bits 0 and 1: LCR0 and LCR1 are word length select bits. These bits program the number of bits in each serial character and is shown in Figure 15.
- Bit 2: LCR2 is the stop bit select bit. This bit specifies the number of stop bits in each transmitted character. The receiver always checks for one stop bit.
- Bit 3: LCR3 is the parity enable bit. When LCR3 is set, a parity bit between the last data word bit and stop bit is generated and checked.
- Bit 4: LCR4 is the even parity select bit. When this bit is set and parity is enabled (LCR3 is set), even parity is selected. When this bit is cleared and parity is enabled, odd parity is selected.
- Bit 5: LCR5 is the stick parity bit. When parity is enabled (LCR3 is set) and this bit is set, the transmission and reception of a parity bit is placed in the opposite state from the value of LCR4. This forces parity to a known state and allows the receiver to check the parity bit in a known state.
- Bit 6: LCR6 is a break control bit. When this bit is set,, the serial outputs TXx are forced to the spacing state (low). The break control bit acts only on the serial output and does not affect the transmitter logic. If the following sequence is used, no invalid characters are transmitted because of the break.

  Step 1. Load a zero byte in response to the transmitter holding register empty (THRE) status indicator.

  Step 2. Set the break in response to the next THRE status indicator.

  Step 3. Wait for the transmitter to be idle when transmitter empty status signal is set (TEMT = 1); then clear the break when the normal transmission has to be restored.
- Bit 7: LCR7 is the divisor latch access bit (DLAB) bit. This bit must be set to access the divisor latches DLL and DLM of the baud rate generator during a read or write operation. LCR7 must be cleared to access the receiver buffer register, the transmitter holding register, or the interrupt enable register.

PRINCIPLES OF OPERATION

line control register (LCR) (continued)

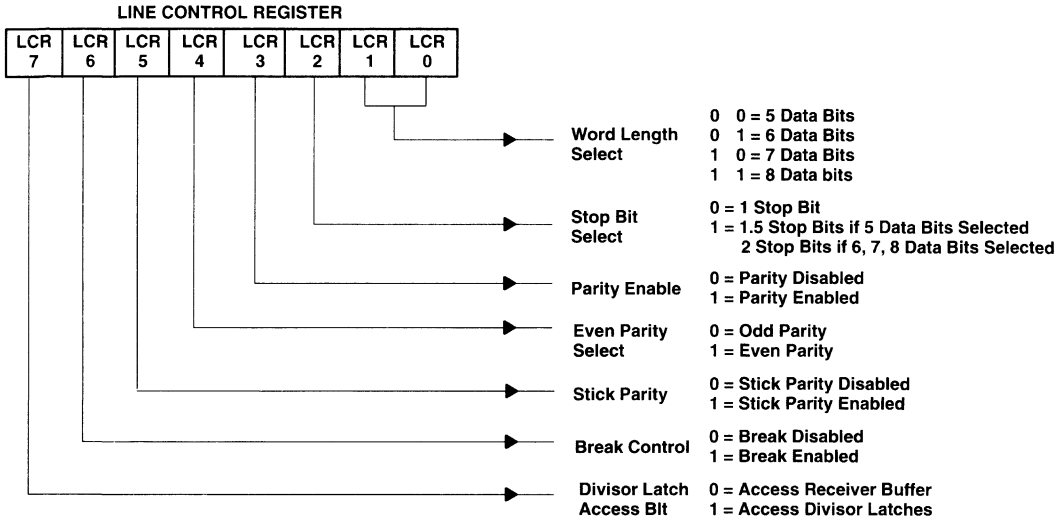


Figure 15. Line Control Register Contents

line status register (LSR)

The LSR is a single register that provides status indicators. The LSR shown in Table 6 is described in the following bulleted list.

- Bit 0: LSR0 is the data ready (DR) bit. Data ready is set when an incoming character is received and transferred into the receiver buffer register or the FIFO. LSR0 is cleared by a CPU read of the data in the receiver buffer register or the FIFO.
- Bit 1: LSR1 is the overrun error (OE) bit. An overrun error indicates that data in the receiver buffer register is not read by the CPU before the next character is transferred into the receiver buffer register overwriting the previous character. The OE indicator is cleared whenever the CPU reads the contents of the LSR. An overrun error occurs in the FIFO mode after the FIFO is full and the next character is completely received. The overrun error is detected by the CPU on the first LSR read after it happens. The character in the shift register is not transferred to the FIFO, but it is overwritten.
- Bit 2: LSR2 is the parity error (PE) bit. A parity error indicates that the received data character does not have the correct parity as selected by LCR3 and LCR4. The PE bit is set upon detection of a parity error and is cleared when the CPU reads the contents of the LSR. In the FIFO mode, the parity error is associated with a particular character in the FIFO. LSR2 reflects the error when the character is at the top of the FIFO.
- Bit 3: LSR3 is the framing error (FE) bit. A framing error indicates that the received character does not have a valid stop bit. LSR3 is set when the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE indicator is cleared when the CPU reads the contents of the LSR. In the FIFO mode, the framing error is associated with a particular character in the FIFO. LSR3 reflects the error when the character is at the top of the FIFO.

PRINCIPLES OF OPERATION

line status register (LSR) (continued)

- Bit 4: LSR4 is the break interrupt (BI) bit. Break interrupt is set when the received data input is held in the spacing (low) state for longer than a full word transmission time (start bit + data bits + parity + stop bits). The BI indicator is cleared when the CPU reads the contents of the LSR. In the FIFO mode, this is associated with a particular character in the FIFO. LSR2 reflects the BI when the break character is at the top of the FIFO. The error is detected by the CPU when its associated character is at the top of the FIFO during the first LSR read. Only one zero character is loaded into the FIFO when BI occurs.

LSR1 – LSR4 are the error conditions that produce a receiver line status interrupt (priority 1 interrupt in the interrupt identification register when any of the conditions are detected. This interrupt is enabled by setting IER2 in the interrupt enable register.

- Bit 5: LSR5 is the transmitter holding register empty (THRE) bit. THRE indicates that the ACE is ready to accept a new character for transmission. The THRE bit is set when a character is transferred from the transmitter holding register (THR) into the transmitter shift register (TSR). LSR5 is cleared by the loading of the THR by the CPU. LSR5 is not cleared by a CPU read of the LSR. In the FIFO mode, when the transmit FIFO is empty this bit is set. It is cleared when one byte is written to the transmit FIFO. When the THRE interrupt is enabled by IER1, THRE causes a priority 3 interrupt in the IIR. If THRE is the interrupt source indicated in IIR, INTRPT is cleared by a read of the IIR.
- Bit 6: LSR6 is the transmitter register empty (TEMT) bit. TEMT is set when the THR and the TSR are both empty. LSR6 is cleared when a character is loaded into THR and remains low until the character is transferred out of TXx. TEMT is not cleared by a CPU read of the LSR. In the FIFO mode, when both the transmitter FIFO and shift register are empty, this bit is set.
- Bit 7: LSR7 is the receiver FIFO error bit. The LSR7 bit is cleared in the TL16C450 mode (see FCR bit 0). In the FIFO mode, it is set when at least one of the following data errors is in the FIFO: parity error, framing error, or break interrupt indicator. It is cleared when the CPU reads the LSR if there are no subsequent errors in the FIFO.

NOTE

The LSR may be written. However, this function is intended only for factory test. It should be considered as read only by applications software.

Table 6. Line Status Register Bits

LSR BITS	1	0
LSR0 data ready (DR)	Ready	Not ready
LSR1 overrun error (OE)	Error	No error
LSR2 parity error (PE)	Error	No error
LSR3 framing error (FE)	Error	No error
LSR4 break interrupt (BI)	Break	No break
LSR5 transmitter holding register empty (THRE)	Empty	Not empty
LSR6 transmitter register empty (TEMT)	Empty	Not empty
LSR7 receiver FIFO error	Error in FIFO	No error in FIFO

PRINCIPLES OF OPERATION

modem control register (MCR)

The MCR controls the interface with the modem or data set as described in Figure 16. MCR can be written and read. The $\overline{RTS}$ and $\overline{DTR}$ outputs are directly controlled by their control bits in this register. A high input asserts a low signal (active) at the output terminals. MCR bits 0, 1, 2, 3, and 4 are shown as follows:

- Bit 0: When MCR0 is set, the $\overline{DTR}$ output is forced low. When MCR0 is cleared, the $\overline{DTR}$ output is forced high. The $\overline{DTR}$ output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.
- Bit1: When MCR1 is set, the $\overline{RTS}$ output is forced low. When MCR1 is cleared, the $\overline{RTS}$ output is forced high. The $\overline{RTS}$ output of the serial channel may be input into an inverting line driver to obtain the proper polarity input at the modem or data set.
- Bit 2: MCR2 has no affect on operation
- Bit 3: When MCR3 is set, the external serial channel interrupt is enabled.
- Bit 4: MCR4 provides a local loopback feature for diagnostic testing of the channel. When MCR4 is set, serial output TXx is set to the marking (high) state and SIN is disconnected. The output of the TSR is looped back into the RSR input. The four modem control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$) are disconnected. The modem control outputs ($\overline{DTR}$ and $\overline{RTS}$) are internally connected to the four modem control inputs. The modem control output terminals are forced to their inactive (high) state on the TL16C554. In the diagnostic mode, data transmitted is immediately received. This allows the processor to verify the transmit and receive data paths of the selected serial channel. Interrupt control is fully operational; however, interrupts are generated by controlling the lower four MCR bits internally. Interrupts are not generated by activity on the external terminals represented by those four bits.
- Bit 5 – Bit 7: MCR5, MCR6, and MCR7 are permanently cleared.

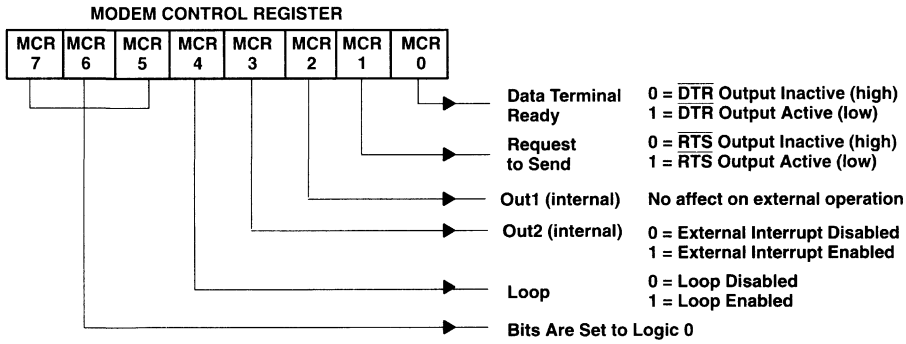


Figure 16. Modem Control Register Contents

PRINCIPLES OF OPERATION

modem status register (MSR)

The MSR provides the CPU with status of the modem input lines for the modem or peripheral devices. The MSR allows the CPU to read the serial channel modem signal inputs by accessing the data bus interface of the ACE in addition to the current status of four bits of the MSR that indicate whether the modem inputs have changed since the last reading of the MSR. The delta status bits are set when a control input from the modem changes states and are cleared when the CPU reads the MSR.

The modem input lines are $\overline{CTS}$, DSR, and $\overline{DCD}$. MSR4 – MSR7 are status indicators of these lines. A status bit = 1 indicates the input is low. When the status bit is cleared, the input is high. When the modem status interrupt in the IER is enabled (IIR3 is set), an interrupt is generated whenever MSR0 – MSR3 is set. The MSR is a priority 4 interrupt. The contents of the MSR are described in Table 7.

- Bit 0: MSR0 is the delta clear-to-send (ΔCTS) bit. DCTS indicates that the $\overline{CTS}$ input to the serial channel has changed state since it was last read by the CPU.
- Bit 1: MSR1 is the delta data set ready (ΔDSR) bit. ΔDSR indicates that the $\overline{DSR}$ input to the serial channel has changed states since the last time it was read by the CPU.
- Bit 2: MSR2 is the trailing edge of ring indicator (TERI) bit. TERI indicates that the $\overline{RIx}$ input to the serial channel has changed states from low to high since the last time it was read by the CPU. High-to-low transitions on RI do not activate TERI.
- Bit 3: MSR3 is the delta data carrier detect (ΔDCD) bit. ΔDCD indicates that the $\overline{DCD}$ input to the serial channel has changed states since the last time it was read by the CPU.
- Bit 4: MSR4 is the clear-to-send (CTS) bit. CTS is the complement of the $\overline{CTS}$ input from the modem indicating to the serial channel that the modem is ready to receive data from SOUT. When the serial channel is in the loop mode (MCR4 = 1), MSR4 reflects the value of RTS in the MCR.
- Bit 5: MSR5 is the data set ready DSR bit. DSR is the complement of the $\overline{DSR}$ input from the modem to the serial channel that indicates that the modem is ready to provide received data from the serial channel receiver circuitry. When the channel is in the loop mode (MCR4 is set), MSR5 reflects the value of DTR in the MCR.
- Bit 6: MSR6 is the ring indicator (RI) bit. RI is the complement of the $\overline{RIx}$ inputs. When the channel is in the loop mode (MCR4 is set), MSR6 reflects the value of $\overline{OUT1}$ in the MCR.
- Bit 7: MSR7 is the data carrier detect (DCD) bit. Data carrier detect indicates the status of the data carrier detect ($\overline{DCD}$) input. When the channel is in the loop mode (MCR4 is set), MSR7 reflects the value of OUT2 in the MCR.

Reading the MSR clears the delta modem status indicators but has no affect on the other status bits. For LSR and MSR, the setting of status bits is inhibited during status register read operations. If a status condition is generated during a read $\overline{IOR}$ operation, the status bit is not set until the trailing edge of the read. When a status bit is set during a read operation and the same status condition occurs, that status bit is cleared at the trailing edge of the read instead of being set again. In the loopback mode when modem status interrupts are enabled, $\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$ and $\overline{DCD}$ inputs are ignored; however, a modem status interrupt can still be generated by writing to MCR3–MCR0. Applications software should not write to the MSR.

PRINCIPLES OF OPERATION

modem status register (MSR) (continued)

Table 7. Modem Status Register Bits

MSR BIT	MNEMONIC	DESCRIPTION
MSR0	ΔCTS	Delta clear to send
MSR1	ΔDSR	Delta data set ready
MSR2	TERI	Trailing edge of ring indicator
MSR3	ΔDCD	Delta data carrier detect
MSR4	CTS	Clear to send
MSR5	DSR	Data set ready
MSR6	RI	Ring indicator
MSR7	DCD	Data carrier detect

programming

The serial channel of the ACE is programmed by the control registers LCR, IER, DLL, DLM, MCR, and FCR. These control words define the character length, number of stop bits, parity, baud rate, and modem interface.

While the control registers can be written in any order, the IER should be written last because it controls the interrupt enables. Once the serial channel is programmed and operational, these registers can be updated any time the ACE serial channel is not transmitting or receiving data.

programmable baud rate generator

The ACE serial channel contains a programmable baud rate generator (BRG) that divides the clock (dc to 8 MHz) by any divisor from 1 to ($2^{16}-1$). Two 8-bit divisor latch registers store the divisor in a 16-bit binary format. These divisor latch registers must be loaded during initialization. Upon loading either of the divisor latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load. The BRG can use any of three different popular frequencies to provide standard baud rates. These frequencies are 1.8432 MHz, 3.072 MHz, and 8 MHz. With these frequencies, standard bit rates from 50 kbps to 512 kbps are available. Tables 8, 9, 10, and 11 illustrate the divisors needed to obtain standard rates using these three frequencies. The output frequency of the baud rate generator is 16× the data rate [divisor # = clock + (baud rate × 16)] referred to in this document as RCLK.

PRINCIPLES OF OPERATION

programmable baud rate generator (continued)

Table 8. Baud Rates Using a 1.8432-MHz Crystal

BAUD RATE DESIRED	DIVISOR (N) USED TO GENERATE 16× CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	—
75	1536	—
110	1047	0.026
134.5	857	0.058
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.690
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
56000	2	2.860

Table 9. Baud Rates Using a 3.072-MHz Crystal

BAUD RATE DESIRED	DIVISOR (N) USED TO GENERATE 16× CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	—
75	2560	—
110	1745	0.026
134.5	1428	0.034
150	1280	—
300	640	—
600	320	—
1200	160	—
1800	107	0.312
2000	96	—
2400	80	—
3600	53	0.628
4800	40	—
7200	27	1.230
9600	20	—
19200	10	—
38400	5	—

PRINCIPLES OF OPERATION

programmable baud rate generator (continued)

Table 10. Baud Rates Using a 8-MHz Clock

BAUD RATE DESIRED	DIVISOR (N) USED TO GENERATE 16× CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	10000	—
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	333	0.010
300	1667	0.020
600	883	0.040
1200	417	0.080
1800	277	0.080
2000	250	—
2400	208	0.160
3600	139	0.080
4800	104	0.160
7200	69	0.644
9600	52	0.160
19200	26	0.160
38400	13	0.160
56000	9	0.790
128000	4	2.344
256000	2	2.344
512000	1	2.400

PRINCIPLES OF OPERATION

programmable baud rate generator (continued)

Table 11. Baud Rates Using a 16-MHz Clock

BAUD RATE DESIRED	DIVISOR (N) USED TO GENERATE 16× CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	20000	0
75	13334	0.00
110	9090	0.01
134.5	7434	0.01
150	6666	0.01
300	3334	−0.02
600	1666	0.04
1200	834	−0.08
1800	554	0.28
2000	500	0.00
2400	416	0.16
3600	278	−0.08
4800	208	0.16
7200	138	0.64
9600	104	0.16
19200	52	0.16
38400	26	0.16
56000	18	−0.79
128000	8	−2.34
256000	4	−2.34
512000	2	−2.34
1000000	1	0.00

receiver

Serial asynchronous data is input into the RXx terminal. The ACE continually searches for a high-to-low transition from the idle state. When the transition is detected, a counter is reset and counts the 16× clock to 7 1/2, which is the center of the start bit. The start bit is valid when the RXx is still low. Verifying the start bits prevents the receiver from assembling a false data character due to a low going noise spike on the RXx input.

The LCR determines the number of data bits in a character (LCR0, LCR1). When parity is enabled, LCR3 and the polarity of parity LCR4 are needed. Status for the receiver is provided in the LSR. When a full character is received including parity and stop bits, the data received indicator in LSR0 is set. The CPU reads the RBR, which clears LSR0. If the character is not read prior to a new character transfer from the RSR to the RBR, the overrun error status indicator is set in LSR1. If there is a parity error, the parity error is set in LSR2. If a stop bit is not detected, a framing error indicator is set in LSR3.

In the FIFO mode operation, the data character and the associated error bits are stored in the receiver FIFO. If the data into RXx is a symmetrical square wave, the center of the data cells occurs within ±3.125% of the actual center, providing an error margin of 46.875%. The start bit can begin as much as one 16× clock cycle prior to being detected.

PRINCIPLES OF OPERATION

reset

After power up, the ACE RESET input should be held high for one microsecond to reset the ACE circuits to an idle mode until initialization. A high on RESET causes the following:

1. It initializes the transmitter and receiver internal clock counters
2. It clears the LSR, except for transmitter register empty (TEMT) and transmit holding register empty (THRE), which are set. The MCR is also cleared. All of the discrete lines, memory elements, and miscellaneous logic associated with these register bits are also cleared or turned off. The LCR, divisor latches, RBR, and transmitter buffer register are not affected.

$\overline{\text{RXRDY}}$ operation

In mode 0, $\overline{\text{RXRDY}}$ is asserted (low) when the receive FIFO is not empty; it is released (high) when the FIFO is empty. In this way, the receiver FIFO is read when $\overline{\text{RXRDY}}$ is asserted (low).

In mode 1, $\overline{\text{RXRDY}}$ is asserted (low) when the receive FIFO has filled to the trigger level or a character time-out has occurred (four character times with no transmission of characters); it is released (high) when the FIFO is empty. In this mode, multiple received characters are read by the DMA device, reducing the number of times it is interrupted.

$\overline{\text{RXRDY}}$ and $\overline{\text{TXRDY}}$ outputs from each of the four internal ACEs of the TL16C554 are ANDed together internally. This combined signal is brought out externally to $\overline{\text{RXRDY}}$ and $\overline{\text{TXRDY}}$.

Following the removal of the reset condition (RESET low), the ACE remains in the idle mode until programmed. A hardware reset of the ACE sets the THRE and TEMT status bits in the LSR. When interrupts are subsequently enabled, an interrupt occurs due to THRE. A summary of the effect of a reset on the ACE is given in Table 12.

Table 12. RESET Affects on Registers and Signals

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt enable register	Reset	All bits cleared (0–3 forced and 4–7 permanent)
Interrupt identification register	Reset	Bit 0 is set, bits 1, 2, 3, 6, and 7 are cleared, Bits 4–5 are permanently cleared
Line control register	Reset	All bits cleared
Modem control register	Reset	All bits cleared (5–7 permanent)
FIFO control register	Reset	All bits cleared
Line status register	Reset	All bits cleared, except bits 5 and 6 are set
Modem status register	Reset	Bits 0–3 cleared, bits 4–7 input signals
TXx	Reset	High
Interrupt (RCVR ERRS)	Read LSR/Reset	Low
Interrupt (receiver data ready)	Read RBR/Reset	Low
Interrupt (THRE)	Read IIR/Write THR/Reset	Low
Interrupt (modem status changes)	Read MSR/Reset	Low
$\overline{\text{RTS}}$	Reset	High
$\overline{\text{DTR}}$	Reset	High

PRINCIPLES OF OPERATION

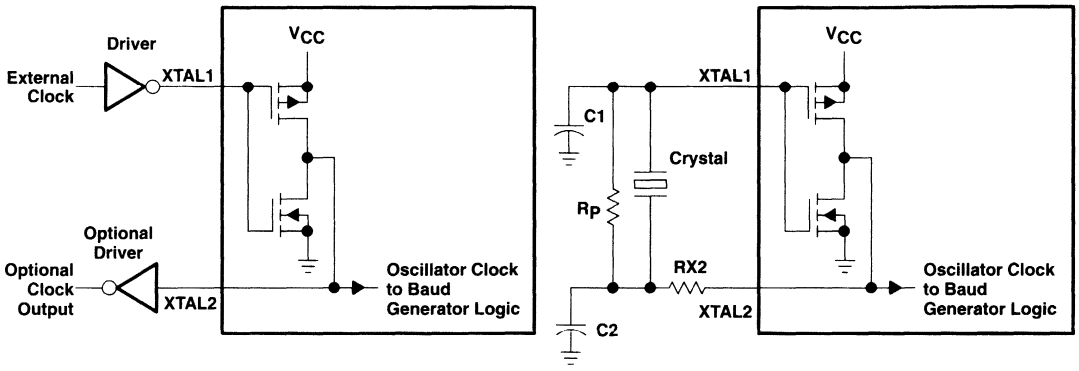
scratchpad register

The scratch register is an 8-bit read/write register that has no affect on either channel in the ACE. It is intended to be used by the programmer to hold data temporarily.

$\overline{\text{TXRDY}}$ operation

In mode 0, $\overline{\text{TXRDY}}$ is asserted (low) when the transmit FIFO is empty; it is released (high) when the FIFO contains at least one byte. In this way, the FIFO is written with 16 bytes when $\overline{\text{TXRDY}}$ is asserted (low).

In mode 1, $\overline{\text{TXRDY}}$ is asserted (low) when the transmit FIFO is not full; in this mode, the transmit FIFO is written with another byte when $\overline{\text{TXRDY}}$ is asserted (low).



TYPICAL CRYSTAL OSCILLATOR NETWORK

CRYSTAL	Rp	RX2	C1	C2
3.1 MHz	1 MΩ	1.5 kΩ	10–30 pF	40–60 pF
1.8 MHz	1 MΩ	1.5 kΩ	10–30 pF	40–60 pF

Figure 17. Typical Clock Circuits

TL16C750
ASYNCHRONOUS COMMUNICATIONS ELEMENT WITH 64-BYTE FIFOs AND AUTOFLOW CONTROL

SLLS191B – JANUARY 1995 – REVISED MARCH 1996

- Pin-to-Pin Compatible With the Existing TL16C550B/C
- Programmable 16- or 64-Byte FIFOs to Reduce CPU Interrupts
- Programmable Auto-$\overline{\text{RTS}}$ and Auto-$\overline{\text{CTS}}$
- In Auto-$\overline{\text{CTS}}$ Mode, $\overline{\text{CTS}}$ Controls Transmitter
- In Auto-$\overline{\text{RTS}}$ Mode, Receiver FIFO Contents and Threshold Control $\overline{\text{RTS}}$
- Serial and Modem Control Outputs Drive a RJ11 Cable Directly When Equipment Is on the Same Power Drop
- Capable of Running With All Existing TL16C450 Software
- After Reset, All Registers Are Identical to the TL16C450 Register Set
- Up to 16-MHz Clock Rate for Up to 1-Mbaud Operation
- In the TL16C450 Mode, Hold and Shift Registers Eliminate the Need for Precise Synchronization Between the CPU and Serial Data
- Programmable Baud Rate Generator Allows Division of Any Input Reference Clock by 1 to ($2^{16}-1$) and Generates an Internal 16 × Clock
- Standard Asynchronous Communication Bits (Start, Stop, and Parity) Added or Deleted to or From the Serial Data Stream
- 5-V and 3-V Operation
- Register Selectable Sleep Mode and Low-Power Mode
- Independent Receiver Clock Input
- Independently Controlled Transmit, Receive, Line Status, and Data Set Interrupts
- Fully Programmable Serial Interface Characteristics:
  - 5-, 6-, 7-, or 8-Bit Characters
  - Even-, Odd-, or No-Parity Bit Generation and Detection
  - 1-, 1 1/2-, or 2-Stop Bit Generation
  - Baud Generation (DC to 1 Mbits Per Second)
- False Start Bit Detection
- Complete Status Reporting Capabilities
- 3-State Output CMOS Drive Capabilities for Bidirectional Data Bus and Control Bus
- Line Break Generation and Detection
- Internal Diagnostic Capabilities:
  - Loopback Controls for Communications Link Fault Isolation
  - Break, Parity, Overrun, Framing Error Simulation
- Fully Prioritized Interrupt System Controls
- Modem Control Functions ($\overline{\text{CTS}}$, $\overline{\text{RTS}}$, $\overline{\text{DSR}}$, $\overline{\text{DTR}}$, $\overline{\text{RI}}$, and $\overline{\text{DCD}}$)
- Available in 44-Pin PLCC and 64-Pin SQFP

description

The TL16C750 is a functional upgrade of the TL16C550C asynchronous communications element (ACE), which in turn is a functional upgrade of the TL16C450. Functionally equivalent to the TL16C450 on power up (character or TL16C450 mode), the TL16C750, like the TL16C550C, can be placed in an alternate mode (FIFO mode). This relieves the CPU of excessive software overhead by buffering received and transmitted characters. The receiver and transmitter FIFOs store up to 64 bytes including three additional bits of error status per byte for the receiver FIFO. The user can choose between a 16-byte FIFO mode or an extended 64-byte FIFO mode. In the FIFO mode, there is a selectable autoflow control feature that can significantly reduce software overload and increase system efficiency by automatically controlling serial data flow through the $\overline{\text{RTS}}$ output and the $\overline{\text{CTS}}$ input signals (see Figure 1).

The TL16C750 performs serial-to-parallel conversion on data received from a peripheral device or modem and parallel-to-serial conversion on data received from its CPU. The CPU can read the ACE status at any time. The ACE includes complete modem control capability and a processor interrupt system that can be tailored to minimize software management of the communications link.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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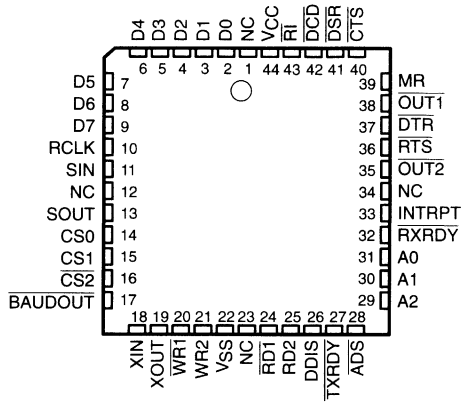
description (continued)

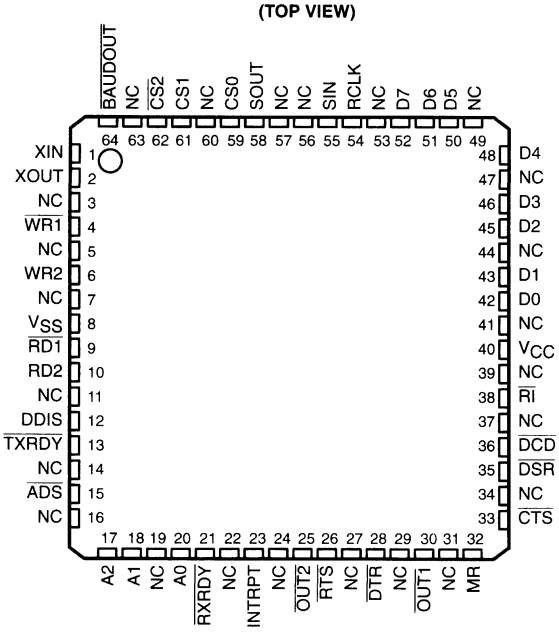
The TL16C750 ACE includes a programmable baud rate generator capable of dividing a reference clock by divisors from 1 to ($2^{16} - 1$) and producing a 16× reference clock for the internal transmitter logic. Provisions are also included to use this 16× clock for the receiver logic. The ACE accommodates a 1-Mbaud serial rate (16-MHz input clock) so a bit time is 1 µs and a typical character time is 10 µs (start bit, 8 data bits, stop bit).

Two of the TL16C450 terminal functions have been changed to $\overline{\text{TXRDY}}$ and $\overline{\text{RXRDY}}$, which provide signaling to a direct memory access (DMA) controller.

FN PACKAGE
(TOP VIEW)

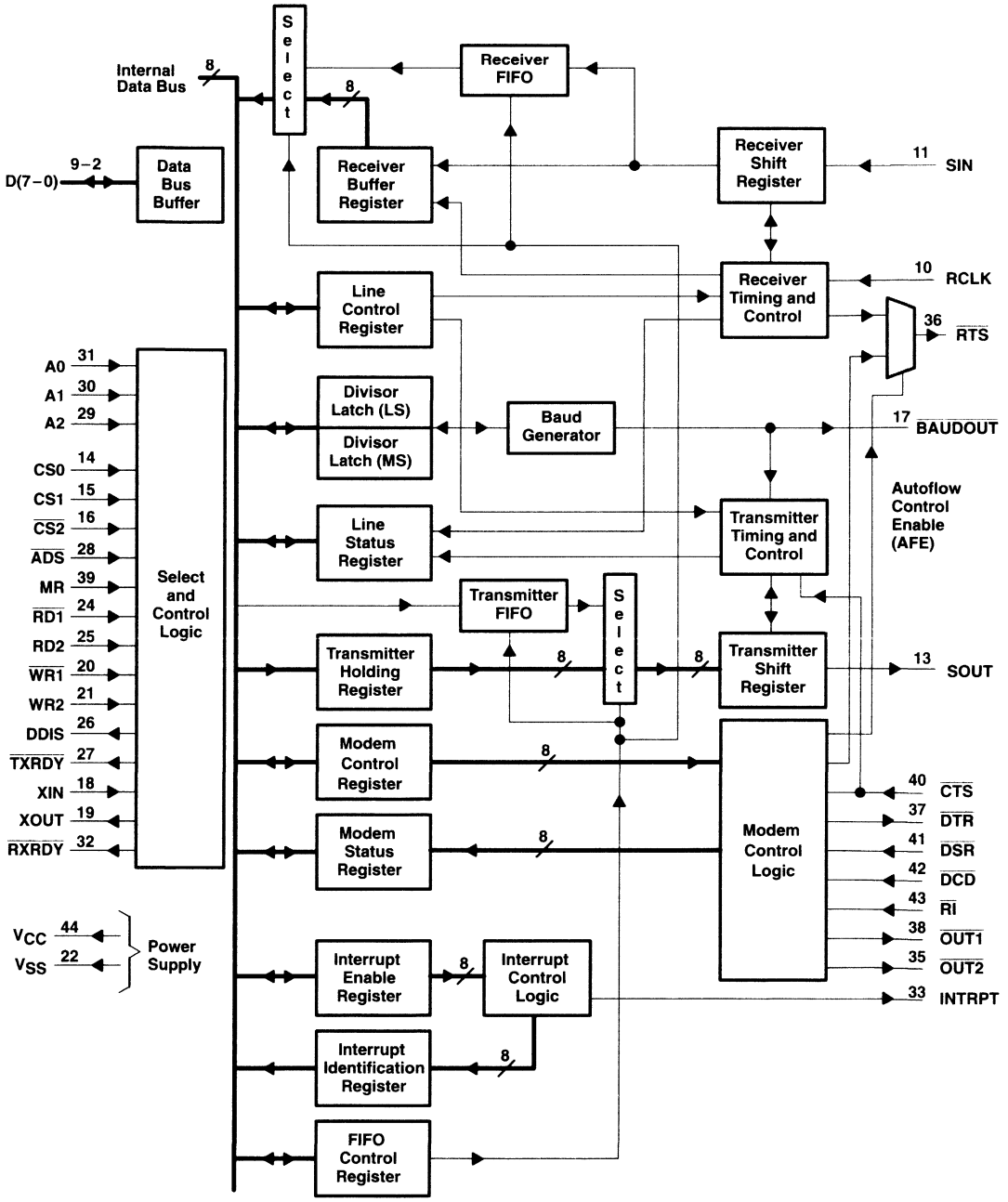


PM PACKAGE
(TOP VIEW)



NC – No internal connection

functional block diagram



NOTE A: Terminal numbers shown are for the FN package.

Terminal Functions

TERMINAL NAME	NO. FN	NO. PM	I/O	DESCRIPTION
A0 A1 A2	31 30 29	20 18 17	I	Register select. A0–A2 are used during read and write operations to select the ACE register to read from or write to. Refer to Table 1 for register addresses and $\overline{ADS}$ signal description.
$\overline{ADS}$	28	15	I	Address strobe. When $\overline{ADS}$ is active (low), the register select signals (A0, A1, and A2) and chip select signals ($\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$) drive the internal select logic directly; when $\overline{ADS}$ is high, the register select and chip select signals are held at the logic levels they were in when the low-to-high transition of $\overline{ADS}$ occurred.
$\overline{BAUDOUT}$	17	64	O	Baud out. $\overline{BAUDOUT}$ is a 16× clock signal for the transmitter section of the ACE. The clock rate is established by the reference oscillator frequency divided by a divisor specified by the baud generator divisor latches. $\overline{BAUDOUT}$ can also be used for the receiver section by tying this output to RCLK.
CS0 CS1 $\overline{CS2}$	14 15 16	59 61 62	I	Chip select. When CS0 and CS1 are high and $\overline{CS2}$ is low, the ACE is selected. When any of these inputs are inactive, the ACE remains inactive. Refer to the $\overline{ADS}$ signal description.
$\overline{CTS}$	40	33	I	Clear to send. $\overline{CTS}$ is a modem status signal. Its condition can be checked by reading bit 4 (CTS) of the modem status register. Bit 0 (ΔCTS) of the modem status register indicates that $\overline{CTS}$ has changed states since the last read from the modem status register. When the modem status interrupt is enabled, $\overline{CTS}$ changes states, and the auto-$\overline{CTS}$ mode is not enabled, an interrupt is generated. $\overline{CTS}$ is also used in the auto-$\overline{CTS}$ mode to control the transmitter.
D0 D1 D2 D3 D4 D5 D6 D7	2 3 4 5 6 7 8 9	42 43 45 46 48 50 51 52	I/O	Data bus. Eight data lines with 3-state outputs provide a bidirectional path for data, control, and status information between the ACE and the CPU. As inputs, they use fail safe CMOS compatible input buffers.
$\overline{DCD}$	42	36	I	Data carrier detect. $\overline{DCD}$ is a modem status signal. Its condition can be checked by reading bit 7 (DCD) of the modem status register. Bit 3 (ΔDCD) of the modem status register indicates that $\overline{DCD}$ has changed states since the last read from the modem status register. When the modem status interrupt is enabled and $\overline{DCD}$ changes state, an interrupt is generated.
DDIS	26	12	O	Driver disable. DDIS is active (high) when the CPU is not reading data. When active, DDIS can disable an external transceiver.
$\overline{DSR}$	41	35	I	Data set ready. $\overline{DSR}$ is a modem status signal. Its condition can be checked by reading bit 5 (DSR) of the modem status register. Bit 1 (ΔDSR) of the modem status register indicates $\overline{DSR}$ has changed states since the last read from the modem status register. When the modem status interrupt is enabled and the $\overline{DSR}$ changes states, an interrupt is generated.
$\overline{DTR}$	37	28	O	Data terminal ready. When active (low), $\overline{DTR}$ informs a modem or data set that the ACE is ready to establish communication. $\overline{DTR}$ is placed in the active state by setting the DTR bit of the modem control register to one. $\overline{DTR}$ is placed in the inactive condition either as a result of a master reset, during loop mode operation, or clearing the DTR bit.
INTRPT	33	23	O	Interrupt. When active (high), INTRPT informs the CPU that the ACE has an interrupt to be serviced. Four conditions that cause an interrupt to be issued are: a receiver error, received data that is available or timed out (FIFO mode only), an empty transmitter holding register, or an enabled modem status interrupt. INTRPT is reset (deactivated) either when the interrupt is serviced or as a result of a master reset.
MR	39	32	I	Master reset. When active (high), MR clears most ACE registers and sets the levels of various output signals (refer to Table 2).
$\overline{OUT1}$ $\overline{OUT2}$	38 35	30 25	O	Outputs 1 and 2. These are user-designated output terminals that are set to their active (low) level by setting their respective modem control register (MCR) bits (OUT1 and OUT2). $\overline{OUT1}$ and $\overline{OUT2}$ are set to their inactive (high) level as a result of master reset, during loop mode operations, or by clearing bit 2 (OUT1) or bit 3 (OUT2) of the MCR.
RCLK	10	54	I	Receiver clock. RCLK is the 16× baud rate clock for the receiver section of the ACE.

Terminal Functions (Continued)

TERMINAL NAME	NO. FN	NO. PM	I/O	DESCRIPTION
$\overline{RD1}$ RD2	24 25	9 10	I	Read inputs. When either $\overline{RD1}$ or RD2 is active (low or high respectively) while the ACE is selected, the CPU is allowed to read status information or data from a selected ACE register. Only one of these inputs is required for the transfer of data during a read operation; the other input should be tied in its inactive state (i.e., RD2 tied low or $\overline{RD1}$ tied high).
$\overline{RI}$	43	38	I	Ring indicator. $\overline{RI}$ is a modem status signal. Its condition can be checked by reading bit 6 (RI) of the modem status register. Bit 2 (TERI) of the modem status register indicates that $\overline{RI}$ has transitioned from a low to a high level since the last read from the modem status register. If the modem status interrupt is enabled when this transition occurs, an interrupt is generated.
$\overline{RTS}$	36	26	O	Request to send. When active, $\overline{RTS}$ informs the modem or data set that the ACE is ready to receive data. $\overline{RTS}$ is set to its active level by setting the RTS MCR bit and is set to its inactive (high) level either as a result of a master reset, during loop mode operations, or by clearing bit 1 (RTS) of the MCR. In the auto-$\overline{RTS}$ mode, $\overline{RTS}$ is set to its inactive level by the receiver threshold control logic.
$\overline{RXRDY}$	32	21	O	Receiver ready. Receiver direct memory access (DMA) signalling is available with $\overline{RXRDY}$. When operating in the FIFO mode, one of two types of DMA signalling can be selected through the FIFO control register bit 3 (FCR3). When operating in the TL16C450 mode, only DMA mode 0 is allowed. Mode 0 supports single-transfer DMA in which a transfer is made between CPU bus cycles. Mode 1 supports multitransfer DMA in which multiple transfers are made continuously until the receiver FIFO has been emptied. In DMA mode 0 (FCR0 = 0 or FCR0 = 1, FCR3 = 0), when there is at least one character in the receiver FIFO or receiver holding register, $\overline{RXRDY}$ is active (low). When $\overline{RXRDY}$ has been active but there are no characters in the FIFO or holding register, $\overline{RXRDY}$ goes inactive (high). In DMA mode 1 (FCR0 = 1, FCR3 = 1), when the trigger level or the timeout has been reached, $\overline{RXRDY}$ goes active (low); when it has been active but there are no more characters in the FIFO or holding register, it goes inactive (high).
SIN	11	55	I	Serial data. SIN is the input from a connected communications device.
SOUT	13	58	O	Composite serial data output to a connected communication device. SOUT is set to the marking (high) level as a result of master reset.
$\overline{TXRDY}$	27	13	O	Transmitter ready. Transmitter DMA signalling is available with $\overline{TXRDY}$. When operating in the FIFO mode, one of two types of DMA signalling can be selected through FCR3. When operating in the TL16C450 mode, only DMA mode 0 is allowed. Mode 0 supports single-transfer DMA in which a transfer is made between CPU bus cycles. Mode 1 supports multitransfer DMA in which multiple transfers are made continuously until the transmit FIFO has been filled.
V_{CC}	44	40		5-V supply voltage
V_{SS}	22	8		Supply common
$\overline{WR1}$ WR2	20 21	4 6	I	Write inputs. When either input is active (low or high respectively) and while the ACE is selected, the CPU is allowed to write control words or data into a selected ACE register. Only one of these inputs is required to transfer data during a write operation; the other input should be tied in its inactive state (i.e., WR2 tied low or $\overline{WR1}$ tied high).
XIN XOUT	18 19	1 2	I/O	External clock. XIN and XOUT connect the ACE to the main timing reference (clock or crystal).

detailed description

autoflow control

Auto-flow control is composed of auto-$\overline{CTS}$ and auto-$\overline{RTS}$. With auto-$\overline{CTS}$, $\overline{CTS}$ must be active before the transmit FIFO can emit data (see Figure 1). With auto-$\overline{RTS}$, $\overline{RTS}$ becomes active when the receiver is empty or the threshold has not been reached. When $\overline{RTS}$ is connected to $\overline{CTS}$, data transmission does not occur unless the receive FIFO has empty space. Thus, overrun errors are eliminated when ACE1 and ACE2 are TLC16C750s with enabled autoflow control. If not, overrun errors occur if the transmit data rate exceeds the receive FIFO read latency.

autoflow control (continued)

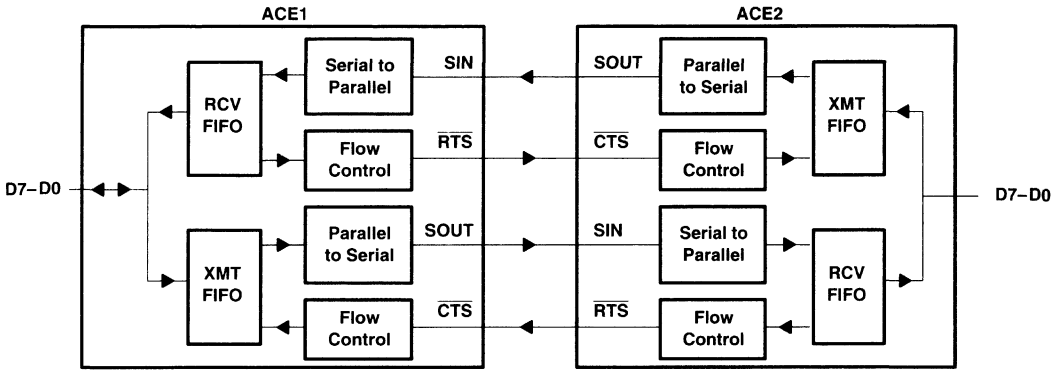


Figure 1. Autoflow Control (auto-$\overline{\text{RTS}}$ and auto-$\overline{\text{CTS}}$) Example

auto-$\overline{\text{RTS}}$ (see Figure 1)

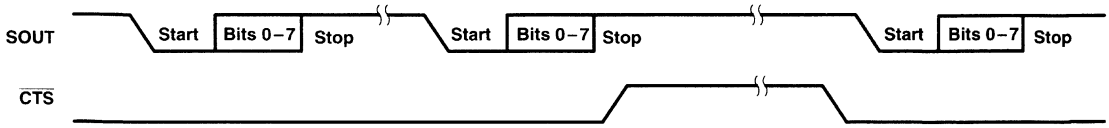
Auto-$\overline{\text{RTS}}$ data flow control originates in the receiver timing and control block (see functional block diagram) and is linked to the programmed receiver FIFO trigger level. When the receiver FIFO level reaches a trigger level of 1, 4, 8, or 14 in 16-byte mode or 1, 16, 32, or 56 in 64-byte mode, $\overline{\text{RTS}}$ is deasserted. The sending ACE may send an additional byte after the trigger level is reached (assuming the sending ACE has another byte to send) because it may not recognize the deassertion of $\overline{\text{RTS}}$ until after it has begun sending the additional byte. $\overline{\text{RTS}}$ is automatically reasserted once the receiver FIFO is emptied by reading the receiver buffer register. The reassertion signals the sending ACE to continue transmitting data.

auto-$\overline{\text{CTS}}$ (see Figure 1)

The transmitter circuitry checks $\overline{\text{CTS}}$ before sending the next data byte. When $\overline{\text{CTS}}$ is active, the transmitter sends the next byte. To stop the transmitter from sending the following byte, $\overline{\text{CTS}}$ must be released before the middle of the last stop bit that is currently being sent. The auto-$\overline{\text{CTS}}$ function reduces interrupts to the host system. When flow control is enabled, the $\overline{\text{CTS}}$ state changes and does not trigger host interrupts because the device automatically controls its own transmitter. Without auto-$\overline{\text{CTS}}$, the transmitter sends any data present in the transmit FIFO and a receiver overrun error can result.

enabling auto-$\overline{\text{RTS}}$ and auto-$\overline{\text{CTS}}$

The auto-$\overline{\text{RTS}}$ and auto-$\overline{\text{CTS}}$ modes of operation are activated by setting bit 5 of the modem control register (MCR) to 1 (see Figure 2).

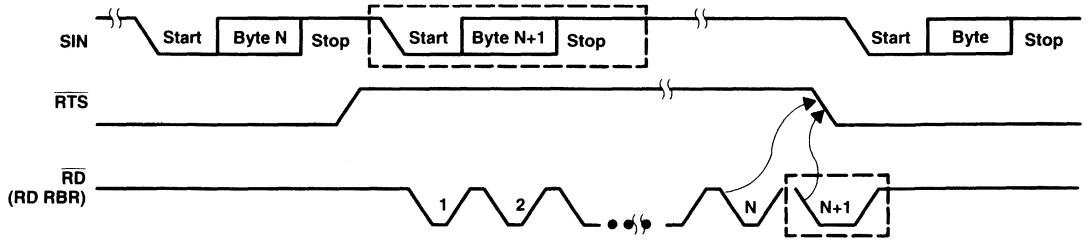


NOTES: A. When $\overline{\text{CTS}}$ is low, the transmitter keeps sending serial data out.
B. When $\overline{\text{CTS}}$ goes high before the middle of the last stop bit of the current byte, the transmitter finishes sending the current byte but it does not send the next byte.
C. When $\overline{\text{CTS}}$ goes from high to low, the transmitter begins sending data again.

Figure 2. $\overline{\text{CTS}}$ Functional Timing

enabling auto-$\overline{RTS}$ and auto-$\overline{CTS}$ (continued)

The receiver FIFO trigger level can be set to 1, 4, 8, or 14 bytes for the 16-byte mode and 1, 16, 32, or 56 bytes for 64-byte mode (see Figure 3).



NOTES: A. N = receiver FIFO trigger level
B. The two blocks in dashed lines cover the case where an additional byte is sent as described in auto-$\overline{RTS}$.

Figure 3. $\overline{RTS}$ Functional Timing, Receiver FIFO Trigger Level

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	−0.5 V to 6 V
Input voltage range, V_I: Standard	−0.5 V to V_{CC} + 0.5 V
Fail safe	−0.5 V to 6.5 V
Output voltage range, V_O: Standard	−0.5 V to V_{CC} + 0.5 V
Fail safe	−0.5 V to 6.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) (see Note 1)	±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) (see Note 2)	±20 mA
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. This applies for external input and bidirectional buffers. V_I > V_{CC} does not apply to fail safe terminals.
2. This applies for external output and bidirectional buffers. V_O > V_{CC} does not apply to fail safe terminals.

recommended operating conditions

low voltage (3.3 V nominal)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
Input voltage, V_I	0		V_{CC}	V
High-level input voltage, V_{IH} (see Note 3)	0.7 V_{CC}			V
Low-level input voltage, V_{IL} (see Note 3)			0.3 V_{CC}	V
Output voltage, V_O (see Note 4)	0		V_{CC}	V
High-level output current, I_{OH} (all outputs)			1.8	mA
Low-level output current, I_{OL} (all outputs)			3.2	mA
Input capacitance, c_i			1	pF
Operating free-air temperature, T_A	0	25	70	°C
Junction temperature range, T_J (see Note 5)	0	25	115	°C
Oscillator/clock speed			14	MHz

NOTES: 3. Meets TTL levels, V_{IHmin} = 2 V and V_{ILmax} = 0.8 V on nonhysteresis inputs
4. Applies for external output buffers
5. These junction temperatures reflect simulated conditions. Absolute maximum junction temperature is 150°C. The customer is responsible for verifying junction temperature.

standard voltage (5 V nominal)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Input voltage, V_I	0		V_{CC}	V
High-level input voltage, V_{IH}	0.7 V_{CC}			V
Low-level input voltage, V_{IL}			0.2 V_{CC}	V
Output voltage, V_O (see Note 4)	0		V_{CC}	V
High-level output current, I_{OH} (all outputs)			4	mA
Low-level output current, I_{OL} (all outputs)			4	mA
Input capacitance, c_i			1	pF
Operating free-air temperature, T_A	0	25	70	°C
Junction temperature range, T_J (see Note 5)	0	25	115	°C
Oscillator/clock speed			16	MHz

NOTES: 4. Applies for external output buffers
5. These junction temperatures reflect simulated conditions. Absolute maximum junction temperature is 150°C. The customer is responsible for verifying junction temperature.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

low voltage (3.3 V nominal)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage†	$I_{OH} = -1.8$ mA	$V_{CC}-0.55$		V
V_{OL}	Low-level output voltage†	$I_{OL} = 3.2$ mA		0.5	V
I_{OZ}	High-impedance 3-state output current (see Note 6)	$V_I = V_{CC}$ or GND		±10	μA
I_{IL}	Low-level input current (see Note 7)	V_I = GND		−1	μA
I_{IH}	High-level input current (see Note 8)	$V_I = V_{CC}$		1	μA

† For all outputs except XOUT

NOTES: 6. The 3-state or open-drain output must be in the high-impedance state.
7. Specifications only apply with pullup termination turned off.
8. Specifications only apply with pulldown termination turned off.

standard voltage (5 V nominal)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage†	$I_{OH} = -4$ mA	$V_{CC}-0.8$		V
V_{OL}	Low-level output voltage†	$I_{OL} = 4$ mA		0.5	V
I_{OZ}	High-impedance 3-state output current (see Note 6)	$V_I = V_{CC}$ or GND		±10	μA
I_{IL}	Low-level input current (see Note 7)	V_I = GND		−1	μA
I_{IH}	High-level input current (see Note 8)	$V_I = V_{CC}$		1	μA

† For all outputs except XOUT

NOTES: 6. The 3-state or open-drain output must be in the high-impedance state.
7. Specifications only apply with pullup termination turned off.
8. Specifications only apply with pulldown termination turned off.

system timing requirements over recommended ranges of supply voltage and operating free-air temperature

	PARAMETER	ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{cR}	Cycle time, read ($t_{w7} + t_{d8} + t_{d9}$)	RC			87		ns
t_{cW}	Cycle time, write ($t_{w6} + t_{d5} + t_{d6}$)	WC			87		ns
t_{w1}	Pulse duration, clock (XIN) high	t_{XH}	4	f = 16 MHz maximum	25		ns
t_{w2}	Pulse duration, clock (XIN) low	t_{XL}	4	f = 16 MHz maximum	25		ns
t_{w5}	Pulse duration, $\overline{ADS}$ low	t_{ADS}	5, 6		9		ns
t_{w6}	Pulse duration, write strobe	t_{WR}	5		40		ns
t_{w7}	Pulse duration, read strobe	t_{RD}	6		40		ns
t_{w8}	Pulse duration, MR	t_{MR}			1		µs
t_{su1}	Setup time, address valid before $\overline{ADS}\uparrow$	t_{AS}	5, 6		8		ns
t_{su2}	Setup time, CS valid before $\overline{ADS}\uparrow$	t_{CS}	5, 6		8		ns
t_{su3}	Setup time, data valid before $\overline{WR1}\downarrow$ or WR2$\uparrow$	t_{DS}	5		15		ns
t_{su4}†	Setup time, $\overline{CTS}\uparrow$ before midpoint of stop bit		16			10	ns
t_{h1}	Hold time, address low after $\overline{ADS}\uparrow$	t_{AH}	5, 6		0		ns
t_{h2}	Hold time, CS valid after $\overline{ADS}\uparrow$	t_{CH}	5, 6		0		ns
t_{h3}	Hold time, CS valid after $\overline{WR1}\uparrow$ or WR2$\downarrow$	t_{WCS}	5		10		ns
t_{h4}†	Hold time, address valid after $\overline{WR1}\uparrow$ or WR2$\downarrow$	t_{WA}	5		10		ns
t_{h5}	Hold time, data valid after $\overline{WR1}\uparrow$ or WR2$\downarrow$	t_{DH}	5		5		ns
t_{h6}	Hold time, CS valid after $\overline{RD1}\uparrow$ or RD2$\downarrow$	t_{RCS}	6		10		ns
t_{h7}†	Hold time, address valid after $\overline{RD1}\uparrow$ or RD2$\downarrow$	t_{RA}	6		20		ns
t_{d4}†	Delay time, CS valid before $\overline{WR1}\downarrow$ or WR2$\uparrow$	t_{CSW}	5		7		ns
t_{d5}	Delay time, address valid before $\overline{WR1}\downarrow$ or WR2$\uparrow$	t_{AW}	5		7		ns
t_{d6}†	Delay time, write cycle, $\overline{WR1}\uparrow$ or WR2$\downarrow$ to $\overline{ADS}\downarrow$	t_{WC}	5		40		ns
t_{d7}†	Delay time, CS valid to $\overline{RD1}\downarrow$ or RD2$\uparrow$	t_{CSR}	6		7		ns
t_{d8}†	Delay time, address valid to $\overline{RD1}\downarrow$ or RD2$\uparrow$	t_{AR}	6		7		ns
t_{d9}	Delay time, read cycle, $\overline{RD1}\uparrow$ or RD2$\downarrow$ to $\overline{ADS}\downarrow$	tRC	6		40		ns
t_{d10}	Delay time, $\overline{RD1}\downarrow$ or RD2$\uparrow$ to data valid	t_{RVD}	6	C_L = 75 pF	45		ns
t_{d11}	Delay time, $\overline{RD1}\uparrow$ or RD2$\downarrow$ to floating data	t_{HZ}	6	C_L = 75 pF	20		ns

† Only applies when $\overline{ADS}$ is low

system switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 9)

	PARAMETER	ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$t_{dis(R)}$	Disable time, $\overline{RD1}\downarrow\uparrow$ or RD2$\uparrow\downarrow$ to DDIS$\uparrow\downarrow$	t_{RDD}	6	C_L = 75 pF	20		ns

NOTE 9: Charge and discharge times are determined by V_{OL}, V_{OH}, and external loading.

baud generator switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 75 pF

	PARAMETER	ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{w3}	Pulse duration, $\overline{BAUDOUT}$ low	t_{LW}	4	f = 16 MHz, CLK ÷ 2	50		ns
t_{w4}	Pulse duration, $\overline{BAUDOUT}$ high	t_{HW}	4	f = 16 MHz, CLK ÷ 2	50		ns
t_{d1}	Delay time, XIN$\uparrow$ to $\overline{BAUDOUT}\uparrow$	t_{BLD}	4			45	ns
t_{d2}	Delay time, XIN$\uparrow\downarrow$ to $\overline{BAUDOUT}\downarrow$	t_{BHD}	4			45	ns

commercial maximum switching characteristics, V_{CC} = 4.75 V, T_J = 115°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	INTRINSIC DELAY (ns)	DELTA DELAY (ns/pF)	DELAY (ns)			
					C_L = 15 pF	C_L = 50 pF	C_L = 85 pF	C_L = 100 pF
t_{PLH}	XIN	XO	−0.92	0.571	7.65	27.66	47.66	56.23
t_{PHL}			−0.79	0.312	3.89	14.83	25.76	30.45
t_r	Output rise time, XO				10.86	40.42	69.98	82.65
t_f	Output fall time, XO				5.47	20.90	36.34	42.95

commercial maximum switching characteristics, V_{CC} = 3 V, T_J = 115°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	INTRINSIC DELAY (ns)	DELTA DELAY (ns/pF)	DELAY (ns)			
					C_L = 15 pF	C_L = 50 pF	C_L = 85 pF	C_L = 100 pF
t_{PLH}	XIN	XO	−4.69	1.017	10.57	46.16	81.75	97.00
t_{PHL}			−3.05	0.442	3.58	19.04	34.51	41.13
t_r	Output rise time, XO				14.39	64.87	115.35	136.98
t_f	Output fall time, XO				5.06	26.53	48.01	57.21

receiver switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 10)

	PARAMETER	ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d12}	Delay time, RCLK to sample clock	t_{SCD}	7			10	ns
t_{d13}	Delay time, stop to set receiver error interrupt or read RBR to LSI interrupt or stop to $\overline{RXRDY}\downarrow$	t_{SINT}	7, 8, 9, 10, 11			2	RCLK cycle
t_{d14}	Delay time, read RBR/LSR low to reset interrupt low	t_{RINT}	7, 8, 9, 10, 11	C_L = 75 pF		120	ns

NOTE 10: In the FIFO mode, the read cycle (RC) = 425 ns (minimum) between reads of the receive FIFO and the status registers (interrupt identification register or line status register).

transmitter switching characteristics over recommended ranges of supply voltage and operating free-air temperature

	PARAMETER†	ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d15}	Delay time, INTRPT to transmit start	t_{IRS}	12		8	24	baudout cycles
t_{d16}	Delay time, start to interrupt	t_{STI}	12		8	10	baudout cycles
t_{d17}	Delay time, WR THR to reset interrupt	t_{HR}	12	C_L = 75 pF		50	ns
t_{d18}	Delay time, initial write to interrupt (THRE)	t_{SI}	12		16	34	baudout cycles
t_{d19}	Delay time, read IIR to reset interrupt (THRE)	t_{IR}	12	C_L = 75 pF		70	ns
t_{d20}	Delay time, write to $\overline{TXRDY}$ inactive	t_{WXI}	13, 14	C_L = 75 pF		75	ns
t_{d21}	Delay time, start to $\overline{TXRDY}$ active	t_{SXA}	13, 14	C_L = 75 pF		9	baudout cycles

† THRE = transmitter holding register empty, IIR = interrupt identification register.

modem control switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 75 pF

	PARAMETER	ALT. SYMBOL	FIGURE	MIN	MAX	UNIT
t_{d22}	Delay time, WR MCR to output	t_{MDO}	15		60	ns
t_{d23}	Delay time, modem interrupt to set interrupt	t_{SIM}	15		35	ns
t_{d24}	Delay time, RD MSR to reset interrupt	t_{RIM}	15		45	ns
t_{d25}	Delay time, $\overline{CTS}$ low to SOUT↓		16		24	baudout cycles
t_{d26}	Delay time, $\overline{receiver}$ threshold byte to $\overline{RTS}$↑		17		2	baudout cycles
t_{d27}	Delay time, read of last byte in receive FIFO to $\overline{RTS}$↓		17		3	baudout cycles

PARAMETER MEASUREMENT INFORMATION

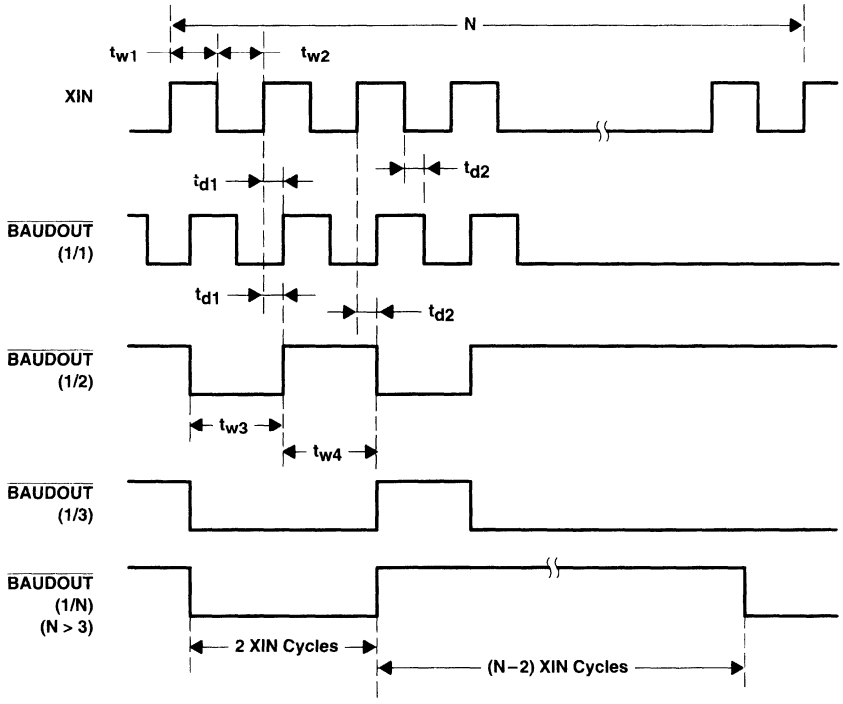
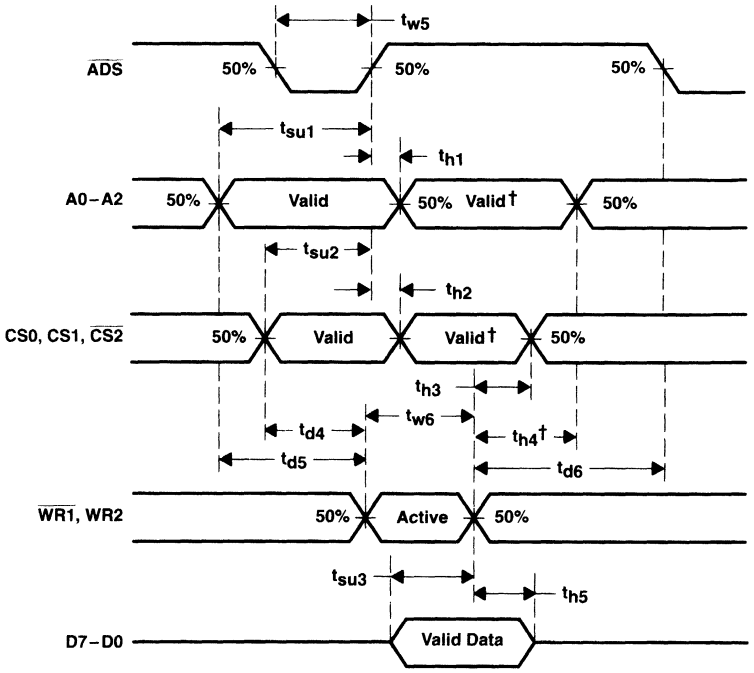


Figure 4. Baud Generator Timing Waveforms

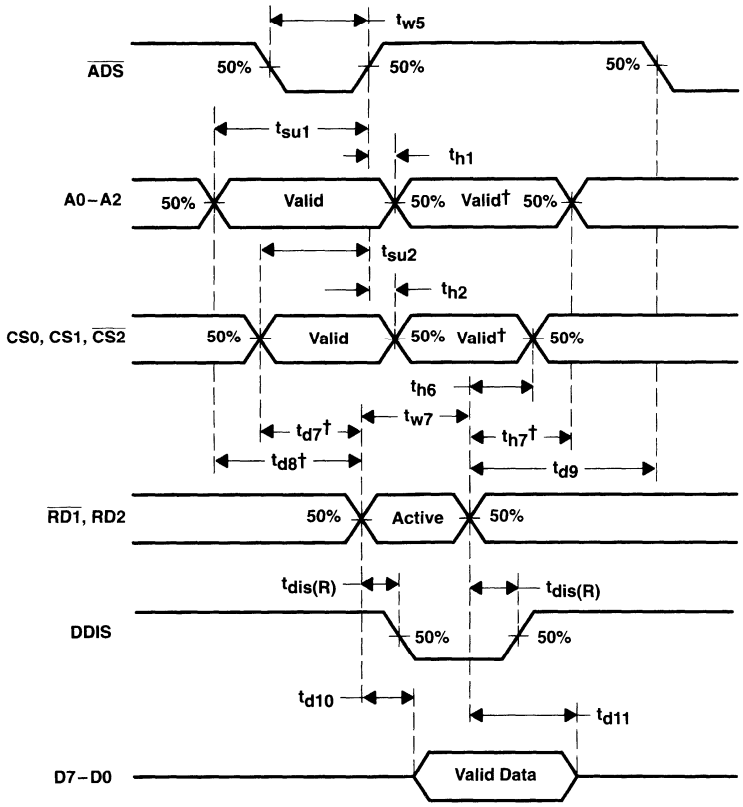
PARAMETER MEASUREMENT INFORMATION



† Applicable only when ADS is low

Figure 5. Write Cycle Timing Waveforms

PARAMETER MEASUREMENT INFORMATION



† Applicable only when $\overline{ADS}$ is low

Figure 6. Read Cycle Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

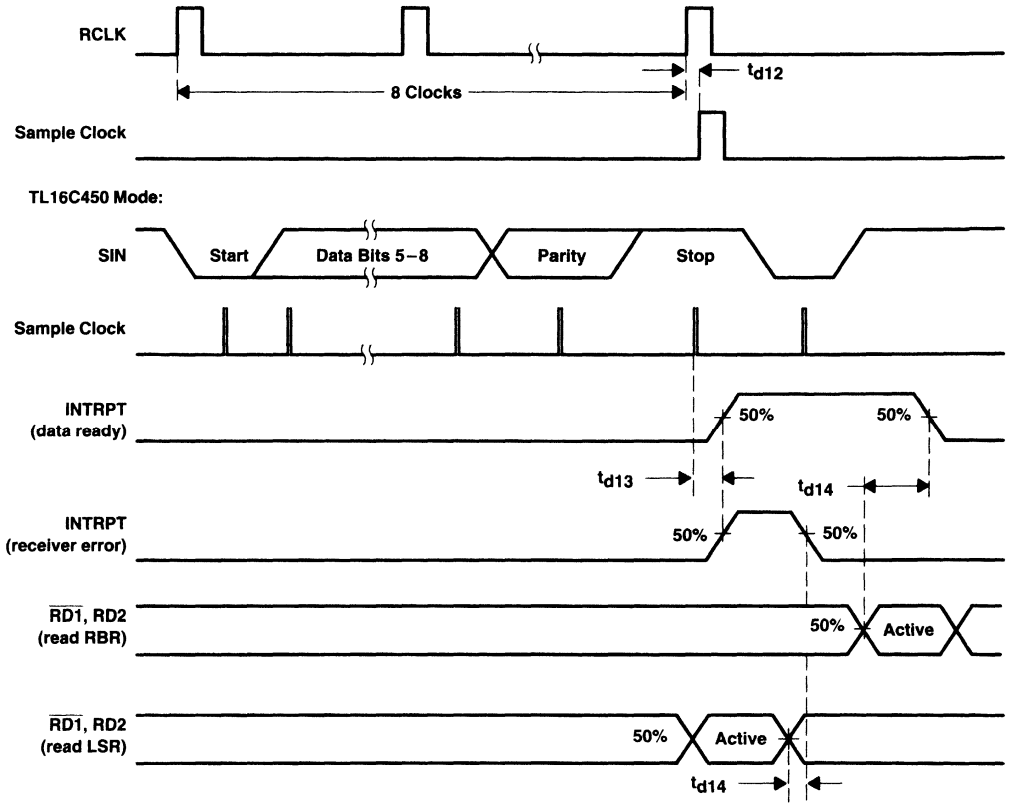
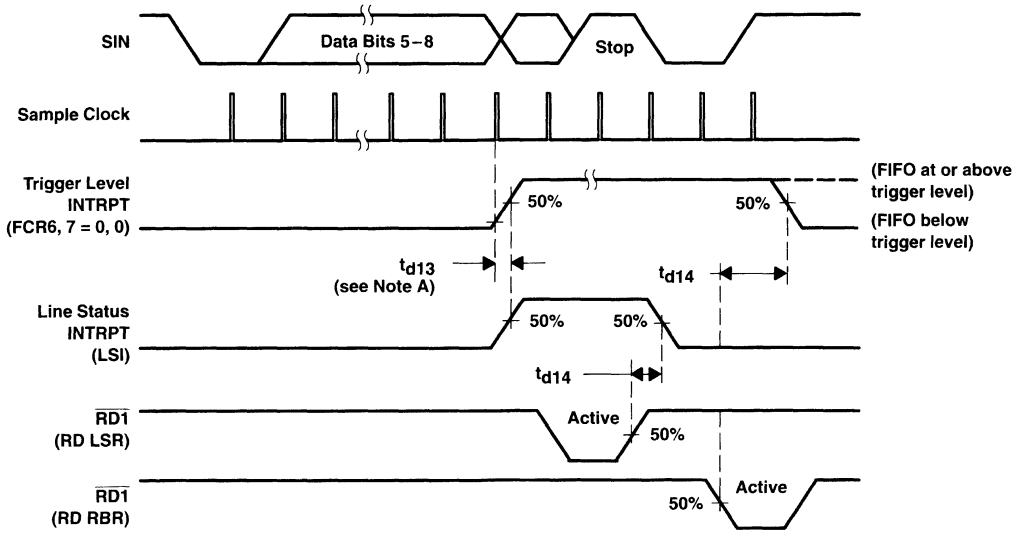


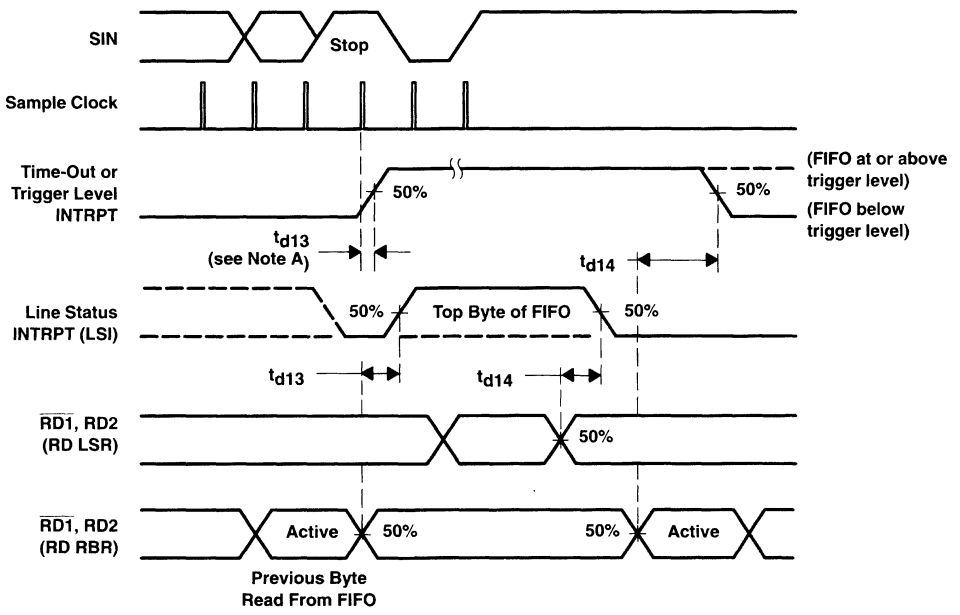
Figure 7. Receiver Timing Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: For a time-out interrupt, t_{d13} = 9 RCLKs.

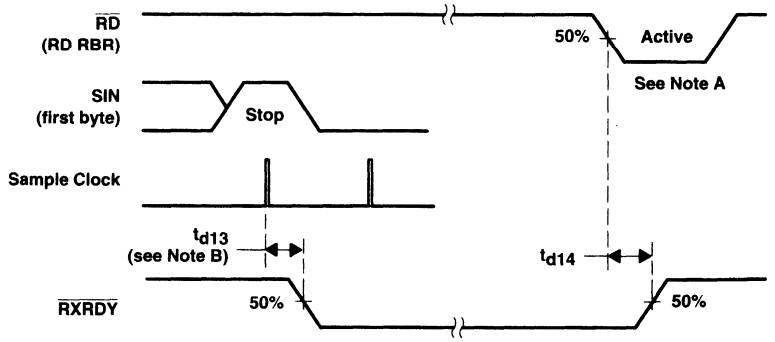
Figure 8. Receive FIFO First Byte (Sets DR Bit) Waveforms



NOTE A: For a time-out interrupt, t_{d13} = 9 RCLKs.

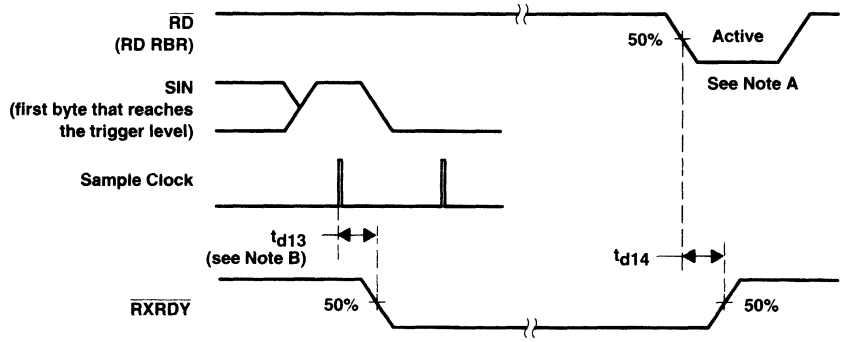
Figure 9. Receive FIFO Bytes Other Than the First Byte (DR Internal Bit Already Set) Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. This is the reading of the last byte in the FIFO.
B. For a time-out interrupt, t_{d13} = 9 RCLKs.

Figure 10. Receiver Ready ($\overline{RXRDY}$) Waveforms, FCR0 = 0 or FCR0 = 1 and FCR3 = 0 (Mode 0)



NOTES: A. This is the reading of the last byte in the FIFO.
B. For a time-out interrupt, t_{d13} = 9 RCLKs.

Figure 11. Receiver Ready ($\overline{RXRDY}$) Waveforms, FCR0 = 1 and FCR3 = 1 (Mode 1)

PARAMETER MEASUREMENT INFORMATION

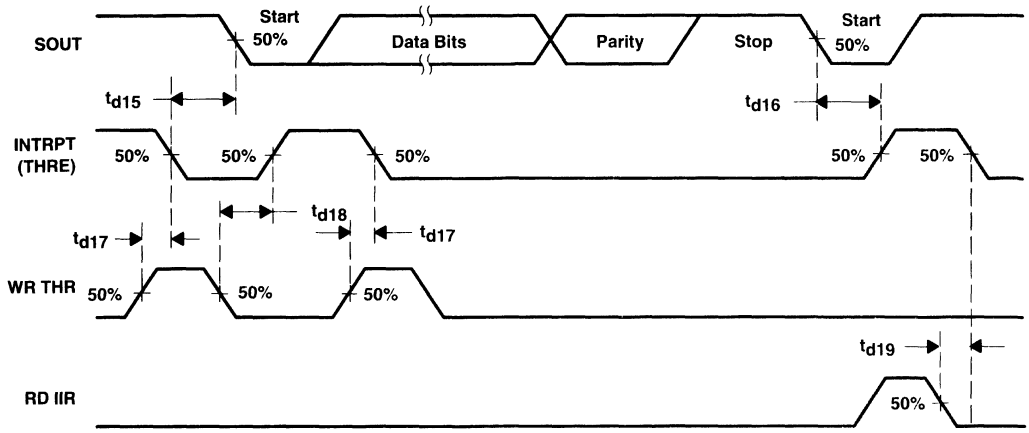


Figure 12. Transmitter Timing Waveforms

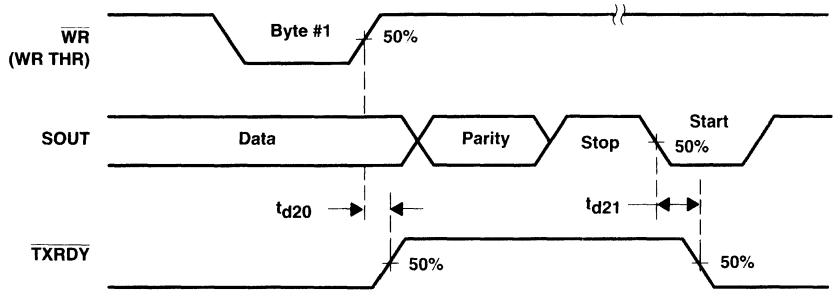


Figure 13. Transmitter Ready ($\overline{\text{TXRDY}}$) Waveforms, FCR0 = 0 or FCR0 = 1 and FCR3 = 0 (Mode 0)

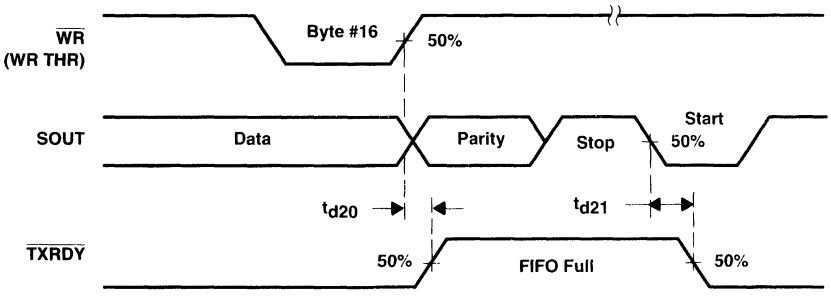


Figure 14. Transmitter Ready ($\overline{\text{TXRDY}}$) Waveforms, FCR0 = 1 and FCR3 = 1 (Mode 1)

PARAMETER MEASUREMENT INFORMATION

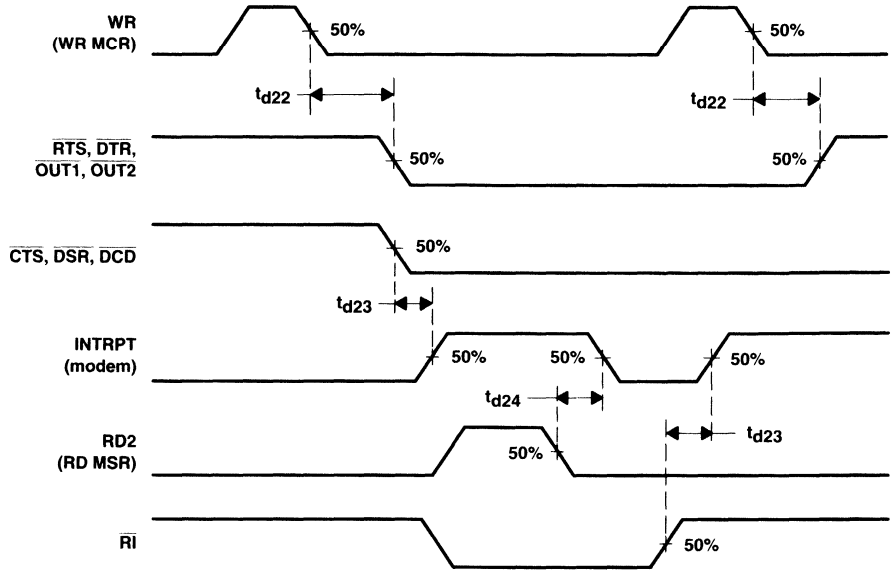


Figure 15. Modem Control Timing Waveforms

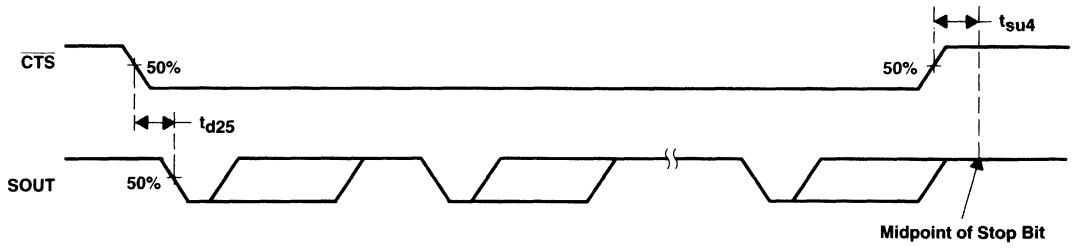


Figure 16. CTS and SOUT Autoflow Control Timing (Start and Stop) Waveforms

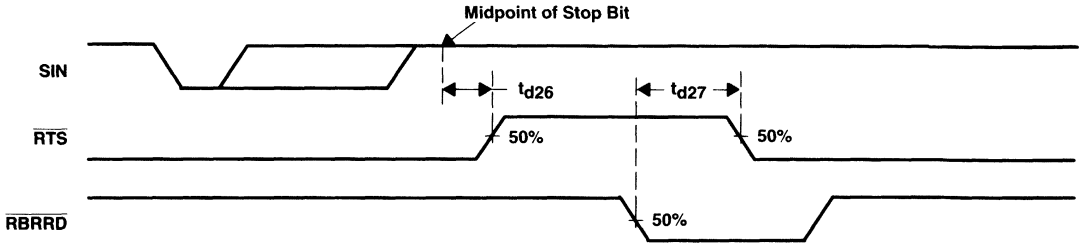


Figure 17. Auto-RTS Timing for Receiver Threshold at All Trigger Levels Waveforms

PARAMETER MEASUREMENT INFORMATION

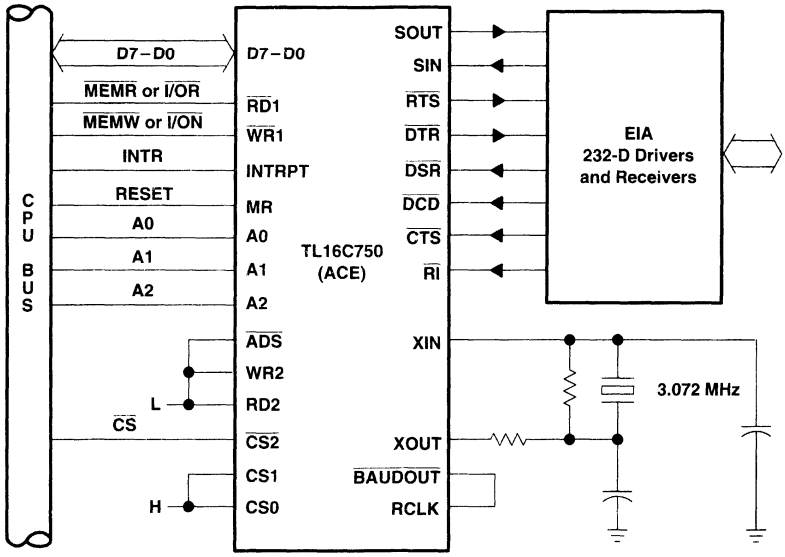


Figure 18. Basic TL16C750 Configuration

APPLICATION INFORMATION

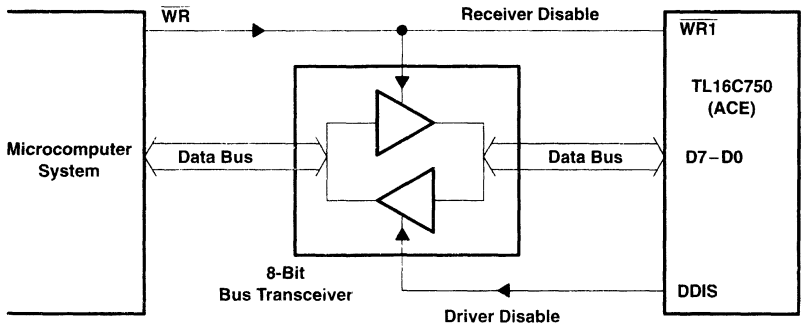
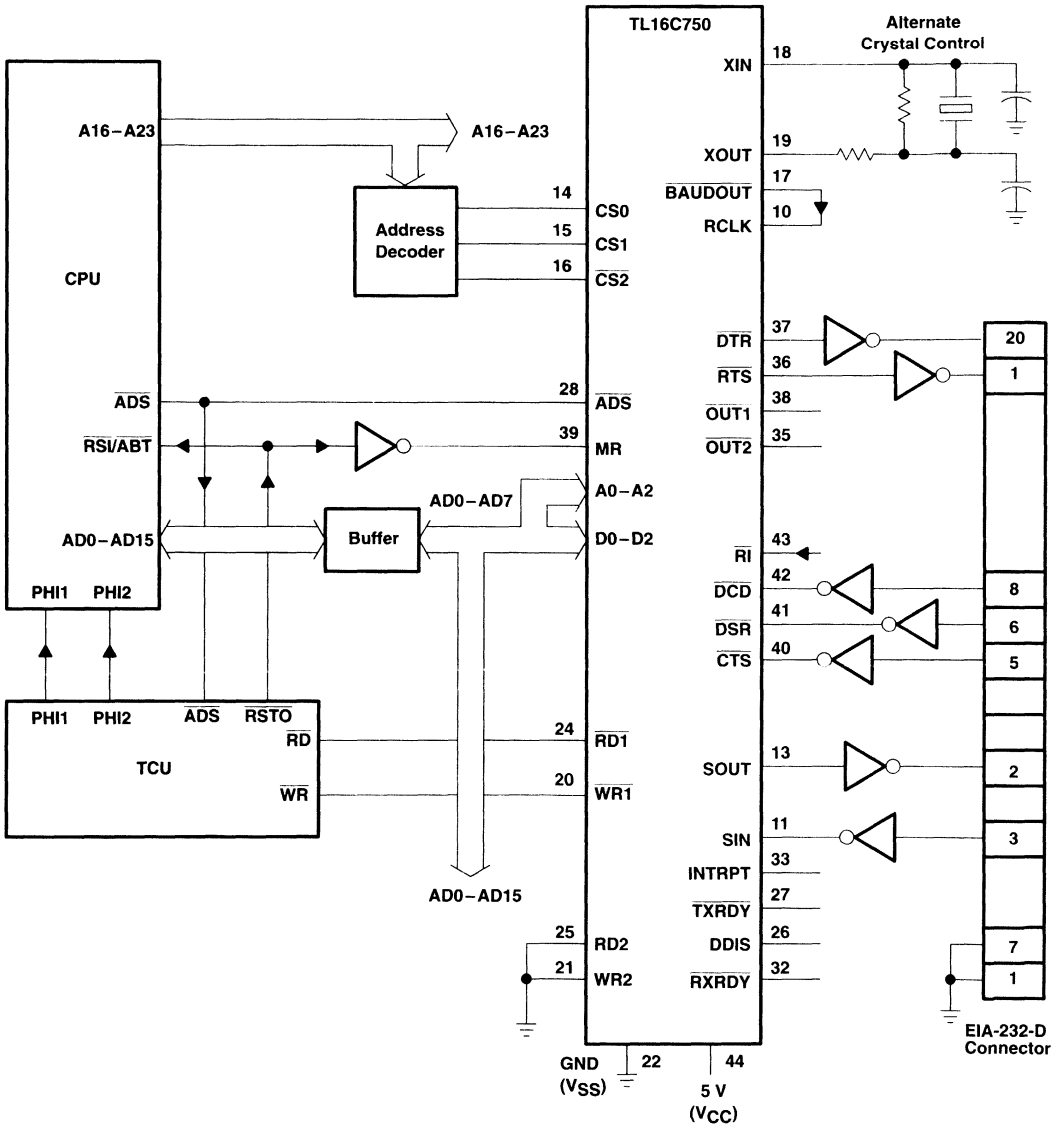


Figure 19. Typical Interface for a High-Capacity Data Bus

APPLICATION INFORMATION



NOTE A: Terminal numbers shown are for the FN package.

Figure 20. Typical TL16C750 Connection to a CPU

PRINCIPLES OF OPERATION

Table 1. Register Selection

DLAB†	A2	A1	A0	REGISTER
0	L	L	L	Receiver buffer (read), transmitter holding register (write)
0	L	L	H	Interrupt enable register
X	L	H	L	Interrupt identification register (read only)
X	L	H	L	FIFO control register (write)
X	L	H	H	Line control register
X	H	L	L	Modem control register
X	H	L	H	Line status register
X	H	H	L	Modem status register
X	H	H	H	Scratch register
1	L	L	L	Divisor latch (LSB)
1	L	L	H	Divisor latch (MSB)

† The divisor latch access bit (DLAB) is the most significant bit of the line control register. The DLAB signal is controlled by writing to this bit location (see Table 3).

Table 2. ACE Reset Functions

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	Master Reset	All bits cleared (0–5 forced and 6–7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is set, bits 1–4 are cleared, and bits 5–7 are cleared
FIFO Control Register	Master Reset	All bits cleared
Line Control Register	Master Reset	All bits cleared
Modem Control Register	Master Reset	All bits cleared (6–7 permanent)
Line Status Register	Master Reset	Bits 5 and 6 are set, all other bits are cleared
Modem Status Register	Master Reset	Bits 0–3 are cleared, bits 4–7 are input signals
SOUT	Master Reset	High
INTRPT (receiver error flag)	Read LSR/MR	Low
INTRPT (received data available)	Read RBR/MR	Low
INTRPT (transmitter holding register empty)	Read IR/Write THR/MR	Low
INTRPT (modem status changes)	Read MSR/MR	Low
$\overline{OUT2}$	Master Reset	High
$\overline{RTS}$	Master Reset	High
$\overline{DTR}$	Master Reset	High
$\overline{OUT1}$	Master Reset	High
Scratch Register	Master Reset	No effect
Divisor Latch (LSB and MSB) Registers	Master Reset	No effect
Receiver Buffer Registers	Master Reset	No effect
Transmitter Holding Registers	Master Reset	No effect
Receiver FIFO	MR/FCR1–FCR0/ ΔFCR0	All bits cleared
XMIT FIFO	MR/FCR2–FCR0/ ΔFCR0	All bits cleared

PRINCIPLES OF OPERATION

accessible registers

The system programmer, through the CPU, has access to and control over any of the ACE registers. These registers control ACE operations, receive data, and transmit data. Descriptions of these registers follow in Table 3.

Table 3. Summary of Accessible Registers

Bit No.	REGISTER ADDRESS											
	0 DLAB = 0	0 DLAB = 0	1 DLAB = 0	2	2	3	4	5	6	7	0 DLAB = 1	1 DLAB = 1
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident. Register (Read Only)	FIFO Control Register (Write Only)	Line Control Register	Modem Control Register	Line Status Register	Modem Status Register	Scratch Register	Divisor Latch (LSB)	Latch (MSB)
	RBR	THR	IER	IIR	FCR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Data Bit 0†	Data Bit 0	Enable Received Data Available Interrupt (ERBI)	0 when interrupt Pending	FIFO Enable	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (ΔCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit 1	Receiver FIFO Reset	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (ΔDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit 2	Transmitter FIFO Reset	Number of Stop Bits (STB)	OUT1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable Modem Status Interrupt (EDSSI)	Interrupt ID Bit 2 (see Note 4)	DMA Mode Select	Parity Enable (PEN)	OUT2	Framing Error (FE)	Delta Data Carrier Detect (ΔDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	Sleep Mode Enable	0	Reserved	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	Low Power Mode Enable	64 Byte FIFO Enabled	64 Byte FIFO Enable‡	Stick Parity	Flow Control Enable (AFE)	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	FIFOs Enabled (see Note 11)	Receiver Trigger (LSB)	Break Control	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	FIFOs Enabled (see Note 11)	Receiver Trigger (MSB)	Divisor Latch Access Bit (DLAB)‡	0	Error in Receiver FIFO (see Note 12)	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

† Bit 0 is the least significant bit. It is the first bit serially transmitted or received.
‡ Access to DLAB LSB, MSB, and FCR bit 5 require LCR bit 7 = 1
NOTE 11: These bits are always 0 in the TL16C450 mode.

PRINCIPLES OF OPERATION

FIFO control register (FCR)

The FCR is a write-only register at the same location as the IIR, which is a read-only register. The FCR enables the FIFOs, clears the FIFOs, sets the receiver FIFO trigger level, and selects the type of DMA signaling.

- Bit 0: FCR0 when set enables the transmit and receive FIFOs. This bit must be set when other FCR bits are written to or they are not programmed. Changing this bit clears the FIFOs.
- Bit 1: FCR1 when set clears all bytes in the receiver FIFO and resets its counter. The RSR is not cleared. The logic 1 that is written to this bit position is self clearing.
- Bit 2: FCR2 when set clears all bytes in the transmit FIFO and resets its counter to 0. The TSR is not cleared. The logic 1 that is written to this bit position is self clearing.
- Bit 3: When FCR0 is set, setting FCR3 causes the $\overline{\text{RXRDY}}$ and $\overline{\text{TXRDY}}$ to change from mode 0 to mode 1.
- Bit 4: Reserved for future use.
- Bit 5: When this bit is set 64-byte mode of operation is selected. When cleared, the 16-byte mode is selected. A write to FCR bit 5 is protected by setting the line control register (LCR) bit 7 = 1. LCR bit 7 needs to cleared for normal operation.
- Bits 6 and 7: FCR6 and FCR7 set the trigger level for the receiver FIFO interrupt (see Table 4).

Table 4. Receiver FIFO Trigger Level

BIT 7	BIT 6	16-BYTE RECEIVER FIFO TRIGGER LEVEL (BYTES)	64-BYTE RECEIVER FIFO TRIGGER LEVEL (BYTES)
0	0	01	01
0	1	04	16
1	0	08	32
1	1	14	56

FIFO interrupt mode operation

When the receiver FIFO and receiver interrupts are enabled (FCR0 = 1, IER0 = 1, IER2 = 1), a receiver interrupt occurs as follows:

1. The received data available interrupt is issued to the microprocessor when the FIFO has reached its programmed trigger level. It is cleared when the FIFO drops below its programmed trigger level.
2. The IIR receive data available indication also occurs when the FIFO trigger level is reached, and as the interrupt, is cleared when the FIFO drops below the trigger level.
3. The receiver line status interrupt (IIR = 06 or 0110h) has higher priority than the received data available (IIR = 04) interrupt.
4. The data ready bit (LSR0) is set when a character is transferred from the shift register to the receiver FIFO. It is cleared when the FIFO is empty.

When the receiver FIFO and receiver interrupts are enabled:

PRINCIPLES OF OPERATION

FIFO interrupt mode operation (continued)

1. FIFO time-out interrupt occurs when the following conditions exist:
   a. At least one character is in the FIFO.
   b. The most recent serial character was received more than four continuous character times ago (if two stop bits are programmed, the second one is included in this time delay).
   c. The most recent microprocessor read of the FIFO occurred more than four continuous character times ago. This causes a maximum character received to interrupt an issued delay of 160 ms at 300 baud with a 12-bit character.
2. Character times are calculated by using RCLK for a clock signal (makes the delay proportional to the baud rate).
3. When a time-out interrupt has occurred, the FIFO interrupt is cleared. The timer is reset when the microprocessor reads one character from the receiver FIFO. When a time-out interrupt has not occurred, the time-out timer is reset after a new character is received or after the microprocessor reads the receiver FIFO.

When the transmitter FIFO and THRE interrupt are enabled (FCR0 = 1, IER1 = 1), transmit interrupts occur as follows:

1. The transmitter holding register interrupt [IIR (3–0) = 2] occurs when the transmit FIFO is empty. The transmit FIFO is cleared [IIR (3–0) = 1] when the THR is written to (1 to 16 characters may be written to the transmit FIFO while servicing this interrupt) or the IIR is read.
2. The transmit FIFO empty indicator (LSR5 (THRE) = 1) is delayed one character time minus the last stop bit time when there have not been at least two bytes in the transmit FIFO at the same time since the last time that THRE = 1. The first transmitter interrupt after changing FCR0 is immediate when it is enabled.

Character time-out and receiver FIFO trigger level interrupts have the same priority as the current received data available interrupt; transmit FIFO empty has the same priority as the current THRE interrupt.

FIFO polled mode operation

With FCR0 = 1 (transmitter and receiver FIFOs enabled), clearing IER0, IER1, IER2, IER3, or all four to 0 puts the ACE in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately, either one or both can be in the polled mode of operation.

In this mode, the user program checks receiver and transmitter status using the LSR. As stated previously:

- LSR0 is set when there is at least one byte in the receiver FIFO.
- LSR (1–4) specify which error(s) have occurred. Character error status is handled the same way as when in the interrupt mode; the IIR is not affected since IER2 = 0.
- LSR5 indicates when the THR is empty.
- LSR6 indicates that both the THR and TSR are empty.
- LSR7 indicates whether there are any errors in the receiver FIFO.

There is no trigger level reached or time-out condition indicated in the FIFO polled mode. However, the receiver and transmitter FIFOs are still fully capable of holding characters.

PRINCIPLES OF OPERATION

interrupt enable register (IER)

The IER enables each of the five types of interrupts (refer to Table 5) and the INTRPT signal in response to an interrupt generation. The IER can also disable the interrupt system by clearing bits 0 through 3. The contents of this register are summarized in Table3 and are described in the following bulleted list.

- Bit 0: When set, this bit enables the received data available interrupt.
- Bit 1: When set, this bit enables the THRE interrupt.
- Bit 2: When set, this bit enables the receiver line status interrupt.
- Bit 3: When set, this bit enables the modem status interrupt.
- Bit 4: When set, this bit enables sleep mode. The ACE is always awake when there is a byte in the transmitter, activity on the SIN, or when the device is in the loopback mode. The ACE is also awake when either ΔCTS, ΔDSR, ΔDCD, or TERI = 1. Bit 4 must be set to enable sleep mode.
- Bit 5: When set, this bit enables low-power mode. Low-power mode functions similar to sleep mode. However, this feature powers down the clock to the ACE only, while keeping the oscillator running. Bit 5 must be set to enable low-power mode.
- Bits 6 and 7: Not used (always cleared)

interrupt identification register (IIR)

The ACE has an on-chip interrupt generation and prioritization capability that permits a flexible interface with most popular microprocessors.

The ACE provides four prioritized levels of interrupts:

- Priority 1 – Receiver line status (highest priority)
- Priority 2 – Receiver data ready or receiver character timeout
- Priority 3 – Transmitter holding register empty
- Priority 4 – Modem status (lowest priority)

When an interrupt is generated, the IIR indicates that an interrupt is pending and provides the type of interrupt in its three least significant bits (bits 0, 1, and 2). The contents of this register are summarized in Table 3 and described in Table 5. Details on each bit are as follows:

- Bit 0: This bit can be used either in a hardwire prioritized, or polled interrupt system. When this bit is cleared, an interrupt is pending. When bit 0 is set, no interrupt is pending.
- Bits 1 and 2: Used to identify the highest priority interrupt pending as indicated in Table 3.
- Bit 3: This bit is always cleared in the TL16C450 mode. In FIFO mode, this bit is set with bit 2 to indicate that a time-out interrupt is pending.
- Bit 4: Not used (always cleared)
- Bits 5, 6, and 7: These bits are to verify the FIFO operation. When all 3 bits are cleared, TL16C450 mode is chosen. When bits 6 and 7 are set and bit 5 is cleared, 16-byte mode is chosen. When bits 5, 6, and 7 are set, 64-byte mode is chosen.

PRINCIPLES OF OPERATION

interrupt identification register (IIR) (continued)

Table 5. Interrupt Control Functions

INTERRUPT IDENTIFICATION REGISTER				PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET METHOD
BIT 3	BIT 2	BIT 1	BIT 0				
0	0	0	1	None	None	None	None
0	1	1	0	1	Receiver line status	Overrun error, parity error, framing error or break interrupt	Reading the line status register
0	1	0	0	2	Received data available	Receiver data available in the TL16C450 mode or trigger level reached in the FIFO mode.	Reading the receiver buffer register
1	1	0	0	2	Character time-out indication	No characters have been removed from or input to the receiver FIFO during the last four character times, and there is at least one character in it during this time	Reading the receiver buffer register
0	0	1	0	3	Transmitter holding register empty	Transmitter holding register empty	Reading the interrupt identification register (if source of interrupt) or writing into the transmitter holding register
0	0	0	0	4	Modem status	Clear to send, data set ready, ring indicator, or data carrier detect	Reading the modem status register

line control register (LCR)

The system programmer controls the format of the asynchronous data communication exchange through the LCR. In addition, the programmer is able to retrieve, inspect, and modify the contents of the LCR; this eliminates the need for separate storage of the line characteristics in system memory. The contents of this register are summarized in Table 3 and described in the following bulleted list.

- Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. These bits are encoded as shown in Table 6.

Table 6. Serial Character Word Length

BIT 1	BIT 0	WORD LENGTH
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

- Bit 2: This bit specifies either one, one and one-half, or two stop bits in each transmitted character. When bit 2 is cleared, one stop bit is generated in the data. When bit 2 is set, the number of stop bits generated is dependent on the word length selected with bits 0 and 1. The receiver clocks only the first stop bit, regardless of the number of stop bits selected. The number of stop bits generated, in relation to word length and bit 2, is shown in Table 7.

PRINCIPLES OF OPERATION

line control register (LCR) (continued)

Table 7. Number of Stop Bits Generated

BIT 2	WORD LENGTH SELECTED BY BITS 1 AND 2	NUMBER OF STOP BITS GENERATED
0	Any word length	1
1	5 bits	1 1/2
1	6 bits	2
1	7 bits	2
1	8 bits	2

- Bit 3: This bit is the parity enable bit. When bit 3 is set, a parity bit is generated in data transmitted between the last data word bit and the first stop bit. In received data, when bit 3 is set, parity is checked. When bit 3 is cleared, no parity is generated or checked.
- Bit 4: This bit is the even parity select bit. When parity is enabled (bit 3 is set) and bit 4 is set, even parity (an even number of logic 1s in the data and parity bits) is selected. When parity is enabled and bit 4 is cleared, odd parity (an odd number of logic 1s) is selected.
- Bit 5: This is the stick parity bit. When bits 3, 4, and 5 are set, the parity bit is transmitted and checked as cleared. When bits 3 and 5 are set and bit 4 is cleared, the parity bit is transmitted and checked as set. When bit 5 is cleared, stick parity is disabled.
- Bit 6: This bit is the break control bit. Bit 6 is set to force a break condition; i.e., a condition where SOUT is forced to the spacing (low) state. When bit 6 is cleared, the break condition is disabled and has no affect on the transmitter logic; it only affects the serial output.
- Bit 7: This bit is the divisor latch access bit (DLAB). Bit 7 must be set to access the divisor latches of the baud generator during a read or write or access bit 5 of the FCR. Bit 7 must be cleared during a read or write to access the receiver buffer, the THR, or the IER.

line status register (LSR)†

The LSR provides information to the CPU concerning the status of data transfers. The contents of this register are described in the following bulleted list and summarized in Table 3.

- Bit 0: This bit is the data ready (DR) indicator for the receiver. DR is set when a complete incoming character is received and transferred into the RBR or the FIFO. DR is cleared by reading all of the data in the RBR or the FIFO.
- Bit 1‡: This bit is the overrun error (OE) indicator. When OE is set, it indicates that before the character in the RBR was read, it was overwritten by the next character transferred into the register. OE is cleared every time the CPU reads the contents of the LSR. When the FIFO mode data continues to fill the FIFO beyond the trigger level, an OE occurs only after the FIFO is full and the next character has been completely received in the shift register. An OE is indicated to the CPU as soon as it happens. The character in the shift register is overwritten, but it is not transferred to the FIFO.
- Bit 2‡: This bit is the parity error (PE) indicator. When PE is set, it indicates that the parity of the received data character does not match the parity selected in the LCR (bit 4). PE is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, PE is associated with the particular character in the FIFO to which it applies. PE is revealed to the CPU when its associated character is at the top of the FIFO.

† The line status register is intended for read operations only; writing to this register is not recommended outside of a factory testing environment.
‡ Bits 1 through 4 are the error conditions that produce a receiver line status interrupt.

PRINCIPLES OF OPERATION

line status register (LSR)† (continued)

- Bit 3‡: This bit is the framing error (FE) indicator. When FE is set, it indicates that the received character does not have a valid (set) stop bit. FE is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. FE is revealed to the CPU when its associated character is at the top of the FIFO. The ACE tries to resynchronize after a FE. To accomplish this, it is assumed that the FE is due to the next start bit. The ACE samples this start bit twice and then accepts the input data.
- Bit 4: This bit is the break interrupt (BI) indicator. When BI is set, it indicates that the received data input was held in the low state for longer than a full-word transmission time. A full-word transmission time is defined as the total time to transmit the start, data, parity, and stop bits. BI is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, BI is associated with the particular character in the FIFO to which it applies. BI is revealed to the CPU when its associated character is at the top of the FIFO. When a break occurs, only one 0 character is loaded into the FIFO. The next character transfer is enabled after SIN goes to the marking state for at least two RCLK samples and then receives the next valid start bit.
- Bit 5: This bit is the transmitter holding register empty (THRE) indicator. THRE is set when the THR is empty, indicating that the ACE is ready to accept a new character. If the THRE interrupt is enabled when THRE is set, an interrupt is generated. THRE is set when the contents of the THR are transferred to the TSR. THRE is cleared concurrent with the loading of the THR by the CPU. In the FIFO mode, THRE is set when the transmit FIFO is empty; it is cleared when at least one byte is written to the transmit FIFO.
- Bit 6: This bit is the transmitter empty (TEMT) indicator. TEMT bit is set when the THR and the TSR are both empty. When either the THR or the TSR contains a data character, TEMT is cleared. In the FIFO mode, TEMT is set when the transmitter FIFO and TSR are both empty.
- Bit 7: In TL16C750 mode and in TL16C450 mode, this bit is always cleared. In the FIFO mode, LSR7 is set when there is at least one parity, framing, or break error in the FIFO. It is cleared when the microprocessor reads the LSR and there are no subsequent errors in the FIFO.

modem control register (MCR)

The MCR is an 8-bit register that controls an interface with a modem, data set, or peripheral device that is emulating a modem. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bit 0: This bit (DTR) controls the $\overline{\text{DTR}}$ output.
- Bit 1: This bit (RTS) controls $\overline{\text{RTS}}$ output.
- Bit 2: This bit (OUT1) controls $\overline{\text{OUT1}}$ signal.
- Bit 3: This bit (OUT2) controls the $\overline{\text{OUT2}}$ signal.

When any of bits 0 through 3 is set, the associated output is forced low; a cleared bit forces the associated output high.

† The line status register is intended for read operations only; writing to this register is not recommended outside of a factory testing environment.
‡ Bits 1 through 4 are the error conditions that produce a receiver line status interrupt.

PRINCIPLES OF OPERATION

modem control register (MCR) (continued)

- Bit 4: This bit (LOOP) provides a local loop back feature for diagnostic testing of the ACE. When LOOP is set, the following occurs:
  - SOUT is asserted high.
  - SIN is disconnected.
  - The output of the TSR is looped back into the RSR input.
  - The four modem control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$) are disconnected.
  - The four modem control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT1}$, and $\overline{OUT2}$) are internally connected to the four modem control inputs.
  - The four modem control outputs are forced to their inactive (high) states.
- Bit 5: This bit (AFE) is the autoflow control enable. When bit 5 is set, the autoflow control, as described in the detailed description, is enabled.

  In the diagnostic mode, data that is transmitted is immediately received. This allows the processor to verify the transmit and receive data paths to the ACE. The receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational, but the modem control interrupt sources are now the lower four bits of the MCR instead of the four modem control inputs. All interrupts are still controlled by the IER.

  The ACE flow can be configured by programming bits 1 and 5 of the MCR as shown in Table 8.

Table 8. ACE Flow Configuration

MCR BIT 5 (AFE)	MCR BIT 1 (RTS)	ACE FLOW CONFIGURATION
1	1	Auto-$\overline{RTS}$ and auto-$\overline{CTS}$ enabled (autoflow control enabled)
1	0	Auto-$\overline{CTS}$ only enabled
0	X	Auto-$\overline{RTS}$ and auto-$\overline{CTS}$ disabled

When bit 5 of the FCR is cleared, there is a 16-byte AFC. When bit 5 of the FCR is set, there is a 64-byte AFC.

modem status register (MSR)

The MSR is an 8-bit register that provides information about the current state of the control lines from the modem, data set, or peripheral device to the CPU. Additionally, four bits of this register provide change information. When a control input from the modem changes state, the appropriate bit is set. All four bits are cleared when the CPU reads the MSR. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bit 0: This bit is the change in clear-to-send (ΔCTS) indicator. ΔCTS indicates that $\overline{CTS}$ has changed states since the last time it was read by the CPU. When ΔCTS is set (autoflow control is not enabled and the modem status interrupt is enabled), a modem status interrupt is generated. When autoflow control is enabled, no interrupt is generated. When ΔCTS is set, sleep or low-power modes are avoided.
- Bit 1: This bit is the change in data set ready (ΔDSR) indicator. ΔDSR indicates that $\overline{DSR}$ has changed states since the last time it was read by the CPU. When ΔDSR is set and the modem status interrupt is enabled, a modem status interrupt is generated. When ΔDSR is set, the sleep or low-power modes are avoided.

PRINCIPLES OF OPERATION

modem status register (MSR) (continued)

- Bit 2: This bit is the trailing edge of the ring indicator (TERI) detector. TERI indicates that $\overline{RI}$ to the chip has changed from a low to a high level. When TERI is set and the modem status interrupt is enabled, a modem status interrupt is generated. When TERI is set, sleep or low-power modes are avoided.
- Bit 3: This bit is the change in data carrier detect (ΔDCD) indicator. ΔDCD indicates that $\overline{DCD}$ to the chip has changed states since the last time it was read by the CPU. When ΔDCD is set and the modem status interrupt is enabled, a modem status interrupt is generated. When ΔDCD is set, sleep or low-power modes are avoided.
- Bit 4: This bit is the complement of $\overline{CTS}$. When the ACE is in the diagnostic test mode (LOOP [MCR4] = 1), this bit is equal to the MCR bit 1 (RTS).
- Bit 5: This bit is the complement of $\overline{DSR}$ input. When the ACE is in the diagnostic test mode (LOOP [MCR4] = 1), this bit is equal to the MCR bit 0 (DTR).
- Bit 6: This bit is the complement of $\overline{RI}$. When the ACE is in the diagnostic test mode (LOOP [MCR4] = 1), this bit is equal to the MCR bit 2 (OUT1).
- Bit 7: This bit is the complement of $\overline{DCD}$. When the ACE is in the diagnostic test mode (LOOP [MCR4] = 1), this bit is equal to the MCR bit 3 (OUT2).

programmable baud generator

The ACE contains a programmable baud generator that takes a clock input in the range between dc and 16 MHz and divides it by a divisor in the range between 1 and ($2^{16}-1$). The output frequency of the baud generator is 16× the baud rate. The formula for the divisor is:

divisor = XIN frequency input ÷ (desired baud rate × 16)

Two 8-bit registers, called divisor latches, store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization of the ACE to ensure desired operation of the baud generator. When either of the divisor latches is loaded, a 16-bit baud counter is also loaded to prevent long counts on initial load.

Tables 9 and 10 illustrate the use of the baud generator with crystal frequencies of 1.8432 MHz and 3.072 MHz respectively. For baud rates of 38.4 kbits/s and below, the error obtained is very small. The accuracy of the selected baud rate is dependent on the selected crystal frequency (see Figure 21).

PRINCIPLES OF OPERATION

programmable baud generator (continued)

Table 9. Baud Rates Using a 1.8432-MHz Crystal

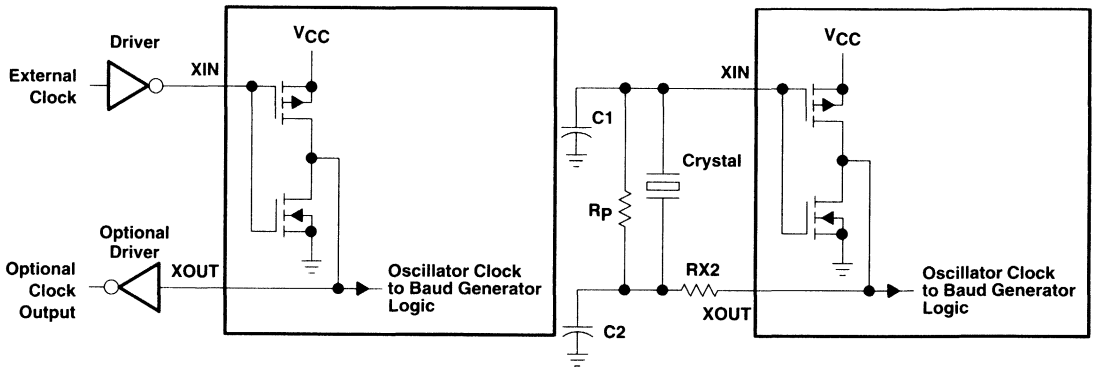
DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16× CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
1800	64	
2000	58	0.69
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19200	6	
38400	3	
56000	2	2.86

Table 10. Baud Rates Using a 3.072-MHz Crystal

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16× CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	
75	2560	
110	1745	0.026
134.5	1428	0.034
150	1280	
300	640	
600	320	
1200	160	
1800	107	0.312
2000	96	
2400	80	
3600	53	0.628
4800	40	
7200	27	1.23
9600	20	
19200	10	
38400	5	

PRINCIPLES OF OPERATION

programmable baud generator (continued)



TYPICAL CRYSTAL/OSCILLATOR NETWORK

CRYSTAL	Rp	RX2	C1	C2
3.072 MHz	1 MΩ	1.5 kΩ	10–30 pF	40–60 pF
1.8432 MHz	1 MΩ	1.5 kΩ	10–30 pF	40–60 pF

Figure 21. Typical Clock Circuits

receiver buffer register (RBR)

The ACE receiver section consists of a RSR and a RBR. The RBR is actually a 64-byte FIFO. Timing is supplied by the 16× receiver clock (RCLK). Receiver section control is a function of the ACE line control register.

The ACE RSR receives serial data from the SIN terminal. The RSR then deserializes the data and moves it into the RBR FIFO. In the TL16C450 mode, when a character is placed in the RBR and the received data available interrupt is enabled, an interrupt is generated. This interrupt is cleared when the data is read out of the RBR. In the FIFO mode, the interrupts are generated based on the control setup in the FIFO control register.

scratch register

The scratch register is an 8-bit register used by the programmer as a scratchpad that temporarily holds the programmer data without affecting any other ACE operation.

transmitter holding register (THR)

The ACE transmitter section consists of a THR and a transmitter shift register (TSR). The THR is actually a 64-byte FIFO. Timing is supplied by the baud out ($\overline{\text{BAUDOUT}}$) clock signal. Transmitter section control is a function of the ACE line control register.

The ACE THR receives data off the internal data bus and when the shift register is idle, moves it into the TSR. The TSR serializes the data and outputs it at the SOUT terminal. In the TL16C450 mode, when the THR is empty and the transmitter holding register empty (THRE) interrupt is enabled (IER1 = 1), an interrupt is generated. This interrupt is cleared when a character is loaded into the register. In the FIFO mode, the interrupts are generated based on the control setup in the FIFO control register.

SLLS172B – MAY 1994 – REVISED MARCH 1996

- **Integrated Asynchronous Communications Element Compatible With PCMCIA PC Card Standard Release 2.01**
- **Consists of a Single TL16C550 ACE Plus PCMCIA Interface Logic**
- **Provides Common I Bus/Z Bus Microcontroller Inputs for Most Intel™ and Zilog™ Subsystems**
- **Fully Programmable 256-Byte Card Information Structure and 8-Byte Card Configuration Register**
- **Adds or Deletes Standard Asynchronous Communication Bits (Start, Stop and Parity) to or From Serial Data Stream**
- **Transmit, Receive, Line Status, and Data Set Interrupts Independently Controlled**
- **Selectable Serial Bypass Mode Provides Subsystem With Direct Parallel Access to the FIFOs**
- **Fully Programmable Serial Interface Characteristics:**
  - **5-, 6-, 7-, or 8-Bit Characters**
  - **Even-, Odd-, or No-Parity Bit Generation and Detection**
  - **1-, 1 1/2-, or 2-Stop Bit Generation**
  - **Baud Rate Generation**
- **Fully Prioritized Interrupt System Controls**
- **Modem Control Functions**
- **Provides TL16C450 Mode at Reset Plus Selectable Normal TL16C550 Operation or Extended 64-Byte FIFO Mode**
- **Selectable Auto-$\overline{\text{RTS}}$ Mode Deactivates $\overline{\text{RTS}}$ at 14 Bytes in 550 Mode and at 56 Bytes in Extended 550 Mode**
- **Selectable Auto-$\overline{\text{CTS}}$ Mode Deactivates Serial Transfers When $\overline{\text{CTS}}$ is Inactive**

description

The TL16PC564A† is designed to provide all the functions necessary for a Personal Computer Memory Card International Association (PCMCIA) universal asynchronous receiver transmitter (UART) subsystem interface. This interface provides a serial-to-parallel conversion for data to and from a modem coder decoder/digital signal processor (CODEC/DSP) function to a PCMCIA parallel data port format. A computer central processing unit (CPU), through a PCMCIA host controller, can read the status of the asynchronous communications element (ACE) interface at any point in the operation. Reported status information includes the type of transfer operation in process, the status of the operation, and any error conditions encountered.

Attribute memory consists of a 256-byte card information structure (CIS) and eight 8-byte card configuration registers (CCR). The CIS, implemented with a dual port random access memory (DPRAM), is available to both the host CPU and subsystem (modem), as are the CCRs. This DPRAM is used in place of the electrically erasable programmable read-only memory (EEPROM) normally used for the CIS. At power up, attribute memory is initialized by the subsystem.

The TL16PC564A uses a TL16C550 ACE-type core with an expanded 64 × 11 receiver first-in-first-out (FIFO) memory and a 64 × 8 transmitter FIFO memory. The receiver trigger logic flags have been adjusted in order to take full advantage of the increased capacity when in the extended mode. In addition, eight of the UART registers have been mapped into the subsystem (modem) memory space as read-only registers. This allows the subsystem to read UART status information.

A subsystem selectable serial bypass mode has been implemented to allow the subsystem to bypass the serial portion of the UART and write directly to the receiver FIFO and read directly from the transmitter FIFO. The interrupt operation is not affected in this mode.

The TL16PC564A is packaged in a 100-pin thin quad flat package (PZ).

† Patent pending

Intel is a trademark of Intel Corporation.
Zilog is a trademark of Zilog Corporation.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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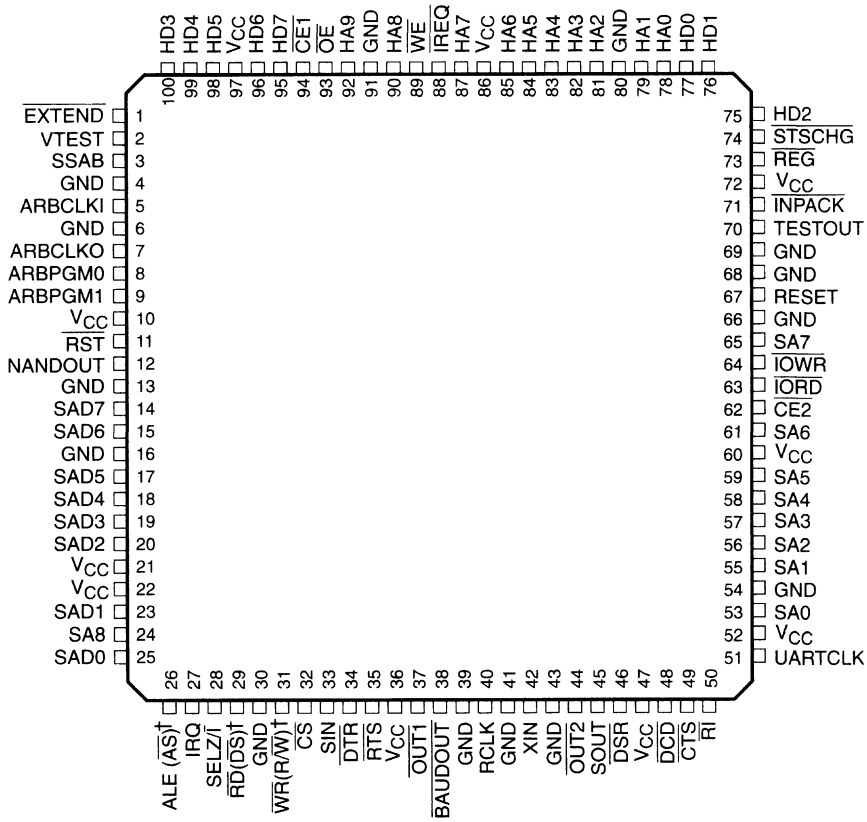
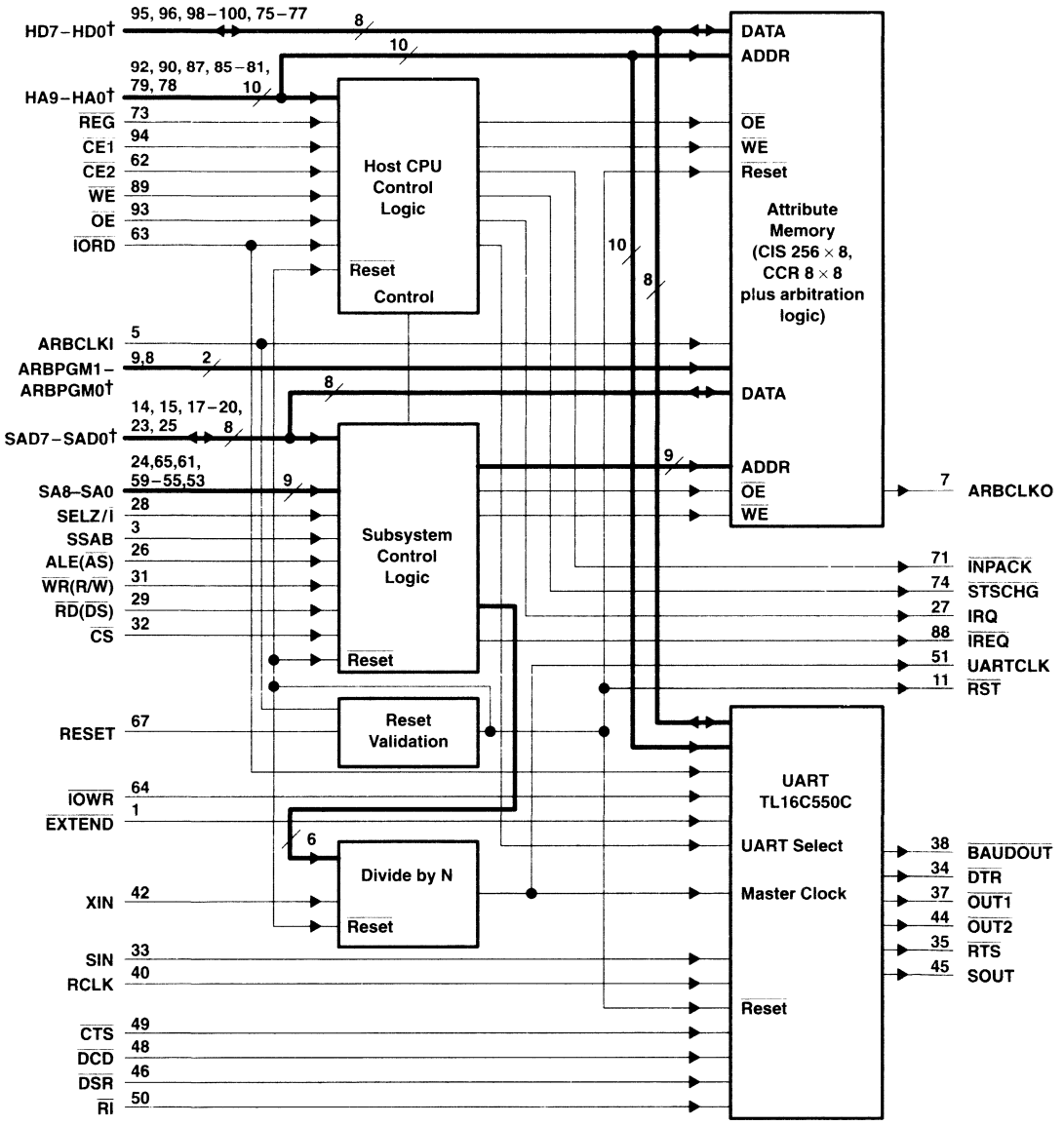
PZ PACKAGE
(TOP VIEW)



† The terminal names not enclosed in parentheses correspond to an Intel microcontroller signal, and the terminal names enclosed in parentheses correspond to a Zilog microcontroller signal.

block diagram



† Bit 0 is the least significant bit (LSB).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	INTERFACE†	I/O	DESCRIPTION
ALE ($\overline{AS}$)	26	S	I	Address latch enable/address strobe. ALE($\overline{AS}$) is an address latch enable in the Intel mode and an address strobe in the Zilog mode. ALE ($\overline{AS}$) is active high for an Intel subsystem and active low for a Zilog subsystem.
ARBCLKO	7	M	O	Arbitration clock output. ARBCLKO is equal to the input on ARBCLKI divided by the binary coded divisor input on ARBPGM (1–0).
ARBCLKI	5	M	I	Arbitration clock input. ARBCLKI is the base clock used in arbitration for the attribute memory DRAM and the reset validation circuitry.
ARBPGM0 ARBPGM1	8 9	M	I	Arbitration clock divisor program. These two bits set the divisor for ARBCLKI. Clock divisors 1, 2, 4, and 8 are available.
$\overline{BAUDOUT}$	38	U	O	Baud output. $\overline{BAUDOUT}$ is an active-low 16× signal for the transmitter section of the UART. The clock rate is established by the reference clock (UARTCLK) frequency divided by a divisor specified by the baud rate generator divisor latches. $\overline{BAUDOUT}$ may also be used for the receiver section by tying this output to the RCLK input.
$\overline{CE1}$ $\overline{CE2}$	94 62	H	I	Card enable 1 and card enable 2 are active-low signals. $\overline{CE1}$ enables even numbered address bytes, and $\overline{CE2}$ enables odd numbered address bytes. A multiplexing scheme based on HA0, $\overline{CE1}$, and $\overline{CE2}$ allows an 8-bit host to access all data on HD0 through HD7 if desired. These signals have internal pullup resistors.
$\overline{CS}$	32	S	I	Chip select. $\overline{CS}$ is the active-low chip select from the Zilog or Intel microcontroller.
$\overline{CTS}$	49	U	I	Clear to send. $\overline{CTS}$ is an active-low modem status signal. Its condition can be checked by reading bit 4 (CTS) of the modem status register (MSR). Bit 0 (delta clear to send) of the MSR indicates that the signal has changed states since the last read from the MSR. If the modem status interrupt is enabled when $\overline{CTS}$ changes states, an interrupt is generated.
DCD	48	U	I	Data carrier detect. $\overline{DCD}$ is an active-low modem status signal. Its condition can be checked by reading bit 7 (DCD) of the MSR. Bit 3 (delta data carrier detect) of the MSR indicates that the signal has changed states since the last read from the MSR. If the modem status interrupt is enabled when $\overline{DCD}$ changes states, an interrupt is generated.
$\overline{DSR}$	46	U	I	Data set ready. $\overline{DSR}$ is an active-low modem status signal. Its condition can be checked by reading bit 5 (DSR) of the MSR. Bit 1 (delta data set ready) of the MSR indicates that the signal has changed states since the last read from the MSR. If the modem status interrupt is enabled when $\overline{DSR}$ changes states, an interrupt is generated.
$\overline{DTR}$	34	U	O	Data terminal ready. $\overline{DSD}$ is an active-low signal. When active, $\overline{DTR}$ informs the modem or data set that the UART is ready to establish communication. $\overline{DTR}$ is placed in the active state by setting the DTR bit 0 of the modem control register (MCR) to a high level. $\overline{DTR}$ is placed in the inactive state either as a result of a reset, doing a loop mode operation, or clearing bit 0 (DTR) of the MCR.
$\overline{EXTEND}$	1	U	I	FIFO extend. When $\overline{EXTEND}$ is high, the UART is configured as a standard TL16C550 with 16-byte transmit and receive FIFOs. When $\overline{EXTEND}$ is low and FIFO control register (FCR) bit 5 is set, the FIFOs are extended to 64 bytes and the receiver interrupt trigger levels adjust accordingly. $\overline{EXTEND}$ low in conjunction with FCR bit 4 set high enables the auto-$\overline{RTS}$.
GND	4, 6, 13, 16, 30, 39, 41, 43, 54, 66, 68, 69, 80, 91	M		Common ground
HA0 HA1 HA2 HA3 HA4 HA5 HA6 HA7 HA8 HA9	78 79 81 82 83 84 85 87 90 92	H	I	H address bus. The 10-bit address bus addresses the attribute memory (bits 1–8) and addresses the internal UART as either PCMCIA I/O (bits 0–2) or as a standard COM port (bits 0–9).

† Host = H, Subsystem = S, UART = U, Miscellaneous = M

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	INTERFACE†	I/O	DESCRIPTION
HD0 HD1 HD2 HD3 HD4 HD5 HD6 HD7	77 76 75 100 99 98 96 95	H	I/O	H data bus. The 8-bit bidirectional data bus transfers data to and from the attribute memory and the internal UART.
$\overline{\text{INPACK}}$	71	H	O	Input port acknowledge. $\overline{\text{INPACK}}$ is an active-low output signal that is asserted when the card responds to an I/O read cycle at the address on the HA bus.
$\overline{\text{IORD}}$	63	H	I	I/O read strobe. $\overline{\text{IORD}}$ is an active-low input signal activated to read data from the card I/O space. The $\overline{\text{REG}}$ signal and at least one of the card enable inputs ($\overline{\text{CE1}}$, $\overline{\text{CE2}}$) must also be active for the I/O transfer to take place. This signal has an internal pullup resistor.
$\overline{\text{IOWR}}$	64	H	I	I/O write strobe. $\overline{\text{IORW}}$ is an active-low input signal activated to write data to the card I/O space. The $\overline{\text{REG}}$ signal and at least one of the card enable inputs ($\overline{\text{CE1}}$, $\overline{\text{CE2}}$) must also be active for the I/O transfer to take place. This signal has an internal pullup resistor.
$\overline{\text{IREQ}}$	88	H	O	Interrupt request. $\overline{\text{IREQ}}$ is an active-low output signal asserted by the card to indicate to the host CPU that a card device requires host software service. This signal doubles as the READY/BUSY signal during power-up initialization.
IRQ	27	S	O	Interrupt request. An active-high IRQ to the subsystem indicates a host CPU write to attribute memory has occurred.
NANDOUT	12	M	O	This is a production test output.
$\overline{\text{OE}}$	93	H	I	Output enable. $\overline{\text{OE}}$ is an active-low input signal that gates memory read data from the card. This signal has an internal pullup resistor.
$\overline{\text{OUT1}}$ $\overline{\text{OUT2}}$	37 44	U	O	Output 1 and output 2 are active-low signals. $\overline{\text{OUT1}}$ and $\overline{\text{OUT2}}$ are user-defined output terminals that are set to their active state by setting the respective MCR bits (OUT1 and OUT2). $\overline{\text{OUT1}}$ and $\overline{\text{OUT2}}$ are set to their inactive (high) state as a result of a reset, by doing loop mode operation, or by clearing bit 2 (OUT1) or bit 3 (OUT2) of the MCR. These signals have open-drain outputs.
RCLK	40	U	I	Receiver clock. RCLK is the 16×-baud rate clock input for the receiver section of the UART.
$\overline{\text{RD}}(\overline{\text{DS}})$	29	S	I	Read enable or data strobe input. $\overline{\text{RD}}(\overline{\text{DS}})$ is the active-low read enable in the Intel mode and the active-low data strobe in the Zilog mode.
$\overline{\text{REG}}$	73	H	I	Attribute memory select. This active-low input signal is generated by the host CPU and accesses attribute memory ($\overline{\text{OE}}$ and $\overline{\text{WE}}$ active) and I/O space ($\overline{\text{IORD}}$ or $\overline{\text{IOWR}}$ active). PCMCIA common memory access is excluded. This signal has an internal pullup resistor and hysteresis on the input buffer.
RESET	67	H	I	Reset. RESET is an active-high input that serves as the master reset for the device. RESET clears the UART, placing the card in an unconfigured state. This signal has an internal pullup resistor.
$\overline{\text{RI}}$	50	U	I	Ring indicator. $\overline{\text{RI}}$ is an active-low modem status signal. Its condition can be checked by reading bit 6 (RI) of the MSR. The trailing edge of ring indicator (TERI) bit 2 of the MSR indicates that $\overline{\text{RI}}$ has transitioned from a low to a high state since the last read from the MSR. If the modem status interrupt is enabled when this transition occurs, an interrupt is generated.
$\overline{\text{RST}}$	11	M	O	This is the qualified active-low reset signal. $\overline{\text{RST}}$ has a fail safe open-drain output.
$\overline{\text{RTS}}$	35	U	O	Request to send. $\overline{\text{RTS}}$ is an active-low signal. When active, $\overline{\text{RTS}}$ informs the modem of the data set that the UART is ready to receive data. $\overline{\text{RTS}}$ is set to its active state by setting the RTS modem control register bit and is set to its inactive (high) state either as a result of a reset, by doing a loop mode operation, or by clearing bit 1 (RTS) of the MCR.

† Host = H, Subsystem = S, UART = U, Miscellaneous = M

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	INTERFACE†	I/O	DESCRIPTION
SA0 SA1 SA2 SA3 SA4 SA5 SA6 SA7	53 55 56 57 58 59 61 65	S	I	Subsystem address bus. When SSAB is high, this is the subsystem address bus and SAD (7–0) is the subsystem data bus. When SSAB is low, this bus is not used and SAD(7–0) is the subsystem multiplexed address/data bus.
SA8	24	S	I	Address bit 8 is bit 8 of the subsystem address bus.
SAD0 SAD1 SAD2 SAD3 SAD4 SAD5 SAD6 SAD7	25 23 20 19 18 17 15 14	S	I/O	Subsystem address/data bus. This is a multiplexed bidirectional address/data bus to the attribute memory DPRAM and CCRs when SSAB is low. This becomes a bidirectional data bus when SSAB is high.
SELZ/$\overline{I}$	28	S	I	Select Zilog or Intel mode. SELZ/$\overline{I}$ selects between a Zilog-like or Intel-like microcontroller. SELZ/$\overline{I}$ is asserted high to select Zilog. SELZ/$\overline{I}$ is asserted low to select Intel.
SIN	33	U	I	Serial data input. SIN moves information from the communication line or modem to the TL16PC564A UART receiver circuits. Data on the serial bus is disabled when operating in the loop mode.
SOUT	45	U	O	Serial out. SOUT is the composite serial data output to a connected communication device. SOUT is set to the marking (high) state as a result of a reset.
SSAB	3	S	I	Separate subsystem address bus. SSAB selects between a multiplexed address/data bus subsystem interface (SSAB = 0) and a subsystem interface with separate address and data buses (SSAB = 1). This signal has an internal pulldown resistor.
$\overline{\text{STSCHG}}$	74	H	O	Status change. $\overline{\text{STSCHG}}$ is an optional active-low output signal that alerts the host that a subsystem write to attribute memory has occurred. This signal has an open-drain output.
TESTOUT	70	M	O	Test output. This is a production test output.
UARTCLK	51	M	O	UART clock. UARTCLK is a clock output. Its frequency is determined by the frequency on XIN and the divisor value on the programmable clock (PGMCLK) register.
V_{CC}	10,21,22,36, 47,52,60, 72,86,97	M		3.3-V or 5-V supply voltage
VTEST	2	M	I	Voltage test. VTEST is an active-high production test input with an internal pulldown resistor. It can be left open or tied to ground.
$\overline{\text{WE}}$	89	H	I	Write enable. $\overline{\text{WE}}$ is an active-low input signal used for strobing attribute memory write data into the card. This signal has an internal pullup resistor
$\overline{\text{WR}}$(R/$\overline{\text{W}}$)	31	S	I	Write or read/write enable. $\overline{\text{WR}}$(R/$\overline{\text{W}}$) is the active-low write enable in the Intel mode and read/$\overline{\text{write}}$ in the Zilog mode.
XIN	42	M	I	Crystal input. XIN is a clock input divided internally based on the PGMCLK register value, then used as the primary UART clock input.

† Host = H, Subsystem = S, UART = U, Miscellaneous = M

detailed description

reset validation circuit

A reset validation circuit has been implemented to qualify the active-high RESET input. At power up, the level on the $\overline{RST}$ output is unknown. Whenever RESET is stable for at least eight ARBCLKIs, $\overline{RST}$ reflects the inverted state of that stable value of RESET. Any changes on RESET must be valid for eight ARBCLKI clocks before the change is reflected on $\overline{RST}$. This 8-clock filter provides needed hysteresis on the master reset input. $\overline{RST}$ is driven by a low noise, open-drain, fail safe output buffer.

host CPU memory map

The host CPU attribute memory space is mapped as shown in Table 1.

Table 1. Host CPU Attribute Memory Space

Host CPU Address Bits 9–1 (HA0 = 0)	Attribute Memory Space
0 – 255	CIS
256	CCR0
257	CCR1
258	CCR2
259	CCR3
260	CCR4
261	CCR5
262	CCR6
263	CCR7

The host CPU I/O space is mapped as shown in Table 2.

Table 2. Host CPU I/O Memory Space

Normal Mode	Address Mode (hex)				I/O Space
	COM1	COM2	COM3	COM4	
0 (DLAB = 0)†	3F8	2F8	3E8	2E8	UART receiver buffer register (RBR) – read only
0 (DLAB = 0)†	3F8	2F8	3E8	2E8	UART transmitter holding register (THR) – write only
0 (DLAB = 1)†	3F8	2F8	3E8	2E8	UART divisor latch LSB (DLL)
1 (DLAB = 0)†	3F9	2F9	3E9	2E9	UART interrupt enable register (IER)
1 (DLAB = 1)†	3F9	2F9	3E9	2E9	UART divisor latch MSB (DLM)
2	3FA	2FA	3EA	2EA	UART interrupt identification register (IIR) – read only
2	3FA	2FA	3EA	2EA	UART FIFO control register (FCR) – write only
3	3FB	2FB	3EB	2EB	UART line control register (LCR)
4	3FC	2FC	3EC	2EC	UART modem control register (MCR) – bit 5 read only
5	3FD	2FD	3ED	2ED	UART line status register (LSR)
6	3FE	2FE	3EE	2EE	UART modem status register (MSR)
7	3FF	2FF	3EF	2EF	UART scratch register (SCR)

† DLAB is bit 7 of the line control register (LCR).

subsystem memory map

The subsystem attribute memory space is mapped as shown in Table 3.

Table 3. Subsystem Attribute Memory Space

Subsystem Address Bits 8–0	Attribute Memory Space
0 – 255	CIS
256	CCR0
257	CCR1
258	CCR2
259	CCR3
260	CCR4
261	CCR5
262	CCR6
263	CCR7

The subsystem control space is mapped as shown in Table 4.

Table 4. Subsystem Control Memory Space

Subsystem Address Bits 8–0	Control Space
272	Control Register
288	PGMCLK Register (write only)

The subsystem UART space is mapped as shown in Table 5.

Table 5. Subsystem UART Memory Space

Subsystem Address Bits 8–0	UART Space
304	UART MCR bit 5 (write only)
304	UART DLL (read only)
305	UART IER (read only)
306	UART FCR (read only)
307	UART LCR (read only)
308	UART MCR (read only)
309	UART LSR (read only)
310	UART MSR (read only)
311	UART DLM (read only)
320	UART transmitter FIFO (read only)†
320	UART receiver FIFO (write only)†

† Only when serial bypass mode is enabled

host CPU/attribute memory interface

The host CPU/attribute memory interface is comprised of one port of the internal DPRAM, the eight CCRs, and necessary control circuitry. Signals HA0 and $\overline{CE1}$ are gated together internally so that the output of the gate is low when both signals have been asserted by the host CPU. This output is combined with $\overline{REG}$ and the decoded address, HA(9–1), to provide the chip enable for the DPRAM and CCRs. This composite chip enable in combination with $\overline{WE}$ or $\overline{OE}$ allows writes and reads to the DPRAM and CCRs.

subsystem/attribute memory interface

The subsystem/attribute memory interface is comprised of the second port of the internal DPRAM, the eight CCRs, and necessary control circuitry. When in multiplexed mode (SSAB = 0), the combination of signals SELZ/$\overline{I}$ and ALE($\overline{AS}$) allows either a positive pulse Intel or a negative pulse Zilog address latch enable strobe to latch the address on SA8 and SAD(7–0). When in the Zilog mode (SELZ/$\overline{I}$ high), the combination of read/write [$\overline{WR}$(R/$\overline{W}$)], data strobe [$\overline{RD}$($\overline{DS}$)], and decoded address allows ZBUS access. When in the Intel configuration (SELZ/$\overline{I}$ low), the combination of read [$\overline{RD}$($\overline{DS}$)], write [$\overline{WR}$(R/$\overline{W}$)], and decoded address allows IBUS access.

When in nonmultiplexed mode (SSAB = 1), SA(7–0) become the lower-order address bits, SAD(7–0) are strictly the bidirectional data bus, and ALE($\overline{AS}$) is nonfunctional. All other interface signals function the same.

Table 6. Subsystem/Attribute Memory Interface

SSAB	SELZ/$\overline{I}$	$\overline{RD}$($\overline{DS}$)	$\overline{WR}$(R/$\overline{W}$)	Address	Operation
0	0	0	1	SA8, SAD(7–0)	Intel read
0	0	1	0	SA8, SAD(7–0)	Intel write
0	1	0	1	SA8, SAD(7–0)	Zilog read
0	1	0	0	SA8, SAD(7–0)	Zilog write
1	0	0	1	SA(8–0)	Intel read
1	0	1	0	SA(8–0)	Intel write
1	1	0	1	SA(8–0)	Zilog read
1	1	0	0	SA(8–0)	Zilog write

attribute memory arbitration

Arbitration for the attribute memory is necessary whenever there is simultaneous access to the same DPRAM or CCR address for the conditions of:

- Host CPU read and subsystem write
- Host CPU write and subsystem read
- Host CPU write and subsystem write

If arbitration were not provided, attribute memory data would be corrupted and invalid data read due to uncontrolled access to the same DPRAM or CCR address.

The arbitration control circuitry synchronizes the asynchronous accesses of the host CPU and subsystem to the DPRAM and CCR and controls the access based on the pending host CPU and subsystem attribute memory operation. The synchronizing and control circuitry needs a clock called the arbitration clock. The external clock (ARBCLKI) goes through a programmable divider and can be divided by 1, 2, 4, or 8 to generate a clock frequency within an allowed range for the arbitration logic to work correctly. The output of this frequency divider is named ARBCLKO. The programmable divider bits are defined as shown in Table 7.

Table 7. Programmable Divider Bits

ARBPGM1	ARBPGM0	INTERNAL ARBITRATION CLOCK
L	L	ARBCLKI/1
L	H	ARBCLKI/2
H	L	ARBCLKI/4
H	H	ARBCLKI/8

attribute memory arbitration (continued)

The upper period limit of ARBCLKO is N/6, where N (ns) is the shortest of the two attribute memory accesses, to either the host CPU or the subsystem. The lower period limit of ARBCLKO is based on the DPRAM specifications at the supply voltage used:

5 V = 14-ns clock cycle (71 MHz)
3.3 V = 26-ns clock cycle (38.5 MHz)

For any arbitration condition, attribute memory access is controlled to ensure valid data is read for a port that is doing a read operation and valid data is written for a port that is doing a write operation. When both the host CPU and subsystem are performing simultaneous write operations to the same address, the host CPU is allowed to write and the subsystem write is ignored.

host CPU/subsystem handshake

Two signals are provided for handshaking between the host CPU and the subsystem. The active-high IRQ signifies to the subsystem that the host CPU has written data into attribute memory. The subsystem can clear IRQ by setting bit 6 of the subsystem control register. The active-low $\overline{\text{STSCHG}}$ signifies to the host CPU that the subsystem has written data to attribute memory provided bit 2 of the subsystem control register ($\overline{\text{STSCHG}}$ enable) is set. The host CPU clears $\overline{\text{STSCHG}}$ by reading any location in attribute memory. The control of these signals is synchronized to ARBCLKO to ensure there are no false assertions/deassertions.

There is additional arbitration performed for instances of simultaneous assertion/deasseration of IRQ or $\overline{\text{STSCHG}}$. When a subsystem write and host CPU read occur simultaneously, $\overline{\text{STSCHG}}$ may be briefly deasserted prior to being asserted, but the write ultimately wins arbitration. If the host CPU read occurs more than one-half an arbitration clock after the subsystem write, $\overline{\text{STSCHG}}$ is deasserted. IRQ is arbitrated in a similar fashion.

host CPU/UART interface

The UART select is derived from either host CPU address information or logic levels on $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ and $\overline{\text{REG}}$. In the address mode, host CPU address bits HA9, HA7, HA6, HA5, and HA3 are combined with conditional derivatives of HA4 and HA8 to select the UART (HA4 and HA8 select COM ports 1–4 based on settings in the subsystem control register). $\overline{\text{CE1}}$ and $\overline{\text{CE2}}$ are combined such that either of these two signals in combination with $\overline{\text{REG}}$ enable the UART in the event that these signals are present. In the event that $\overline{\text{CE1}}$ or $\overline{\text{CE2}}$ are not present, the UART must be accessed in the address mode previously described. The UART select in conjunction with $\overline{\text{IORD}}$ and $\overline{\text{IOWR}}$ allows host CPU accesses to the UART. Host CPU address bits HA2–HA0 are decoded to select which UART register is to be accessed.

All UART registers remain intact with the exception of the FIFO control register (FCR) and the modem control register (MCR). The FCR (host CPU write-only address 2) bits 4 and 5 in conjunction with $\overline{\text{EXTEND}}$ control $\overline{\text{RTS}}$ operation and FIFO depth are shown in Table 8.

Table 8. FIFO Control Register and $\overline{\text{EXTEND}}$ Signal Control of FIFO Depth and $\overline{\text{RTS}}$ Operation

BIT 5	BIT 4	$\overline{\text{EXTEND}}$	RTS OPERATION	FIFO DEPTH
X	X	H	Normal	16 bytes
0	0	L	Normal	16 bytes
0	1	L	Auto	16 bytes
1	0	L	Normal	64 bytes
1	1	L	Auto	64 bytes

host CPU/UART interface (continued)

FCR bit 5 high and $\overline{\text{EXTEND}}$ low redefine the receiver FIFO trigger levels set by FCR bits 6 and 7 are shown in Table 9.

Table 9. Receiver FIFO Trigger Level

BIT 7	BIT 6	RECEIVER FIFO TRIGGER LEVEL
0	0	1
0	1	16
1	0	32
1	1	56

The MCR bit 5 (host CPU address 4) is read only. This bit is controlled by the subsystem to enable (high) the auto-$\overline{\text{CTS}}$ mode of operation

subsystem/UART interface

The UART provides a serial communications channel to the subsystem with enhanced $\overline{\text{RTS}}$ control (see auto-$\overline{\text{RTS}}$ description). This channel is capable of operating at 115 kbps and is the main communications channel to the subsystem (refer to the TL16C550 specification for the detailed description of the serial communications channel).

Many of the UART registers have been mapped into the subsystems memory space as read only. In addition, MCR bit 5 (subsystem address 130 hex) is controlled by the subsystem to enable (set) auto-$\overline{\text{CTS}}$. The subsystem can read the MCR at address 134 hex. When reading the FCR (subsystem address 132 hex), bits 1 and 2 are always set, and bits 4 and 5 are cleared only when $\overline{\text{EXTEND}}$ is low and the host CPU has set them (64-byte FIFOs and auto-$\overline{\text{RTS}}$ enabled) (refer to the subsystem memory map).

subsystem control register

The subsystem control register is an 8-bit register located at subsystem address 110 (hex). This register is programmed based on host CPU configuration information and has a default selection of COM2 after a valid reset. The bit definitions are as follows (0 = LSB):

- Bits 0 and 1: These bits define which host COM port the UART is connected to when the chip is in the address mode. COM2 is the default (power-up) condition. COM port selection is shown in Table 10.

Table 10. COM Port Selection

BIT 1	BIT 0	COM PORT
0	0	COM1
1	0	COM2
0	1	COM3
1	1	COM4

- Bit 2: This bit is a host CPU interrupt enable bit. When this bit is set, any subsystem attribute memory write cycle causes $\overline{\text{STSCHG}}$ to be asserted. This bit is cleared after a valid reset.
- Bit 3: This bit enables or disables address mode selection as described in the host CPU/UART interface description. This bit is cleared (disabling the address mode) after a valid reset.

subsystem control register (continued)

- Bits 4 and 5: These bits together ensure adherence to PCMCIA power-up requirements. At power up, the card must operate as a memory card and all host CPU I/O operations must be disabled. $\overline{\text{IREQ}}$, which doubles as the host CPU READY/$\overline{\text{BUSY}}$ line, powers up low indicating that the memory card is busy. Once the subsystem initializes attribute memory, the subsystem sets bit 4 to indicate that the memory card is ready. Then bit 5 is cleared, changing the configuration from a memory card to an I/O card, enabling host CPU UART accesses. $\overline{\text{IREQ}}$ now becomes the host CPU interrupt request line. Memory card, I/O, and $\overline{\text{IREQ}}$ selection is shown in Table 11.

Table 11. Memory Card, I/O, and $\overline{\text{IREQ}}$ Selection

BIT 5	BIT 4	CONFIGURATION
1	0	Memory card and I/O operation (UART) are disabled; $\overline{\text{IREQ}}$ is low indicating that the card is busy (power-up and reset condition).
1	1	Memory card and I/O operation (UART) are disabled; $\overline{\text{IREQ}}$ is high indicating that the card is ready.
0	X	I/O card and I/O operation (UART) are enabled; $\overline{\text{IREQ}}$ now functions as the host CPU interrupt request line.

- Bit 6 is a self clearing bit that resets the subsystem IRQ signal. Writing a 1 to this location clears the IRQ interrupt.
- Bit 7 enables or disables serial bypass mode as described in the subsystem serial bypass mode description. This bit is cleared (disabling serial bypass mode) after a valid reset.

subsystem PGMCLK register/divide-by-n circuit

The subsystem PGMCLK register is a 6-bit write-only register located at address 120 hex and selects the divisor of the divide-by-n-and-a-half circuitry. Any write to this register generates a reset to the UART and the divide-by-n circuitry.

The divide-by-n circuitry allows for a divisor from 0 to 31.5 in 0.5 increments (PGMCLK0 is the half bit). The divided clock output drives the UART clock input and can be seen on UARTCLK. The UART requires a clock with a minimum high pulse duration of 50 ns and a minimum low pulse duration of 50 ns (10-MHz maximum operating frequency). A programmed divisor between 2 and 7.5 drives the UART clock low for one XIN clock cycle for integer divisors and 1.5 XIN clock cycles for integer-plus-a-half divisors. A programmed divisor of eight or greater drives the UART clock low for four XIN clock cycles for integer divisors and 4.5 XIN clock cycles for integer-plus-a-half divisors. Based on the above parameters, the acceptable

XIN/divisor combinations can be derived using XIN input clock. The precision of the programmable clock generator for integer-plus-a-half divisors depends on the closeness to a 50% duty cycle for the XIN input clock (see Table 12).

Table 12. Programmable Clock Generator Precision Selection

PGMCLK(0–5) VALUE (HEX)	RESULT
0 (0)	No clock (driven high)
0.5 (1)	Divide-by-1
1 (2)	Divide-by-1
1.5 (3)	Divide-by-1
2 (4) to 31.5 (3F)	Divide-by-2 to divide-by-31.5

subsystem serial bypass mode

The optional serial bypass mode is implemented to allow a high throughput path to/from the host CPU. When this mode is enabled and subsystem control register bit 7 is high, the serial portion of the UART is bypassed and the subsystem has direct parallel access to the receiver FIFO (write address 140 hex) and the transmitter FIFO (read address 140 hex). All host CPU interrupts operate normally except for receiver parity, framing, and breaking interrupts.

auto-$\overline{\text{CTS}}$ operation

The optional auto-$\overline{\text{CTS}}$ operation is implemented so that the host CPU cannot overflow the modem receive buffer. Auto-$\overline{\text{CTS}}$ operation is enabled when the subsystem sets MCR bit 5 (subsystem address 130 hex). When auto-$\overline{\text{CTS}}$ enabled, deactivating $\overline{\text{CTS}}$ (high) halts the transmitter section of the UART after it completes the current transfer. Once $\overline{\text{CTS}}$ is reactivated (low) by the modem, transfers resume. Interrupt operation is not affected by enabling auto-$\overline{\text{CTS}}$.

auto-$\overline{\text{RTS}}$ operation

The optional auto-$\overline{\text{RTS}}$ operation is implemented so that the subsystem cannot overflow the receiver FIFO. Auto-$\overline{\text{RTS}}$ operation is enabled when FCR bit 4 is high and $\overline{\text{EXTEND}}$ is low and operates independently from the trigger level circuitry. In the 16-byte FIFO mode, the RTS bit in the modem control register (bit 1) clears when 14 characters are in the receive FIFO. This action causes $\overline{\text{RTS}}$ to go high (inactive). In the 64-byte FIFO mode, the MCR RTS bit clears when 56 characters are in the receiver FIFO. Interrupt operation is not affected and operates the same way in either auto-$\overline{\text{RTS}}$ or nonauto-$\overline{\text{RTS}}$ mode. When enabled, a receive data available interrupt occurs after the trigger level is reached. The MCR RTS bit must then be set by the host CPU after the receiver FIFO has been read.

power consumption

The TL16PC564A has low power consumption under the following conditions:

- 32-MHz signal on XIN
- Divide-by-n is set to give a 1.8432-MHz UARTCLK signal
- Nominal data
- V_{CC} = 5 V

The current (I_{CC}) and power consumption are 18 mA (typical) and 90 mW (typical), respectively. These current and power figures fluctuate with changes in the above conditions.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC}	−0.5 V to 6 V
Input voltage range, V_I (standard)	−0.5 V to V_{CC} + 0.5 V
Input voltage range, V_I (fail safe)	−0.5 V to 6.5 V
Output voltage range, V_O (standard)	−0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (fail safe)	−0.5 V to 6.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) (see Note 1)	±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) (see Note 2)	±20 mA
Operating free-air operating temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. This applies for external input and bidirectional buffers. $V_I > V_{CC}$ does not apply to fail safe terminals.
2. This applies for external output and bidirectional buffers. $V_O > V_{CC}$ does not apply to fail safe terminals.

recommended operating conditions

low voltage (3.3 V nominal)

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
Input voltage, V_I		0		V_{CC}	V
High-level input voltage (CMOS), V_{IH} (see Note 3)		$0.7V_{CC}$			V
Low-level input voltage (CMOS), V_{IL} (see Note 3)				$0.3V_{CC}$	V
Output voltage, V_O (see Note 4)		0		V_{CC}	V
High-level output current, I_{OH}	All outputs except $\overline{RST}$, $\overline{STSCHG}$, $\overline{OUT1}$, $\overline{OUT2}$ (see Note 5)			1.8	mA
Low-level output current, I_{OL}	All outputs except $\overline{RST}$			3.2	mA
	$\overline{RST}$			6.4	
Input transition time, t_t		0		25	ns
Operating free-air temperature range, T_A		0	25	70	°C
Junction temperature range, T_J (see Note 6)		0	25	115	°C

NOTES: 3. Meets TTL levels, V_{IH}min = 2 V and V_{IL}max = 0.8 V on nonhysteresis inputs.
4. Applies for external output buffers.
5. $\overline{RST}$, $\overline{STSCHG}$, $\overline{OUT1}$, and $\overline{OUT2}$ are open-drain outputs, so I_{OH} does not apply.
6. These junction temperatures reflect simulation conditions. Absolute maximum junction temperature is 150°C. The customer is responsible for verifying junction temperature.

standard voltage (5 V nominal)

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Input voltage, V_I		0		V_{CC}	V
High-level input voltage (CMOS), V_{IH}		$0.7V_{CC}$			V
Low-level input voltage (CMOS), V_{IL}				$0.2V_{CC}$	V
Output voltage, V_O (see Note 4)		0		V_{CC}	V
High-level output current, I_{OH}	All outputs except $\overline{RST}$, $\overline{STSCHG}$, $\overline{OUT1}$, $\overline{OUT2}$ (see Note 5)			4	mA
Low-level output current, I_{OL}	All outputs except $\overline{RST}$			4	mA
	$\overline{RST}$			8	
Input transition time, t_t		0		25	ns
Operating free-air temperature range, T_A		0	25	70	°C
Junction temperature range, T_J (see Note 6)		0	25	115	°C

NOTES: 4. Applies for external output buffers.
5. $\overline{RST}$, $\overline{STSCHG}$, $\overline{OUT1}$, and $\overline{OUT2}$ are open-drain outputs, so I_{OH} does not apply.
6. These junction temperatures reflect simulation conditions. Absolute maximum junction temperature is 150°C. The customer is responsible for verifying junction temperature.

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

low voltage (3.3 V nominal)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = rated	$V_{CC}-0.55$		V
V_{OL}	Low-level output voltage	I_{OL} = rated		0.5	V
V_{IT+}	Positive-going input threshold voltage (see Note 7)			$0.7\ V_{CC}$	V
V_{IT-}	Negative-going input threshold voltage (see Note 7)		$0.3\ V_{CC}$		V
V_{hys}	Hysteresis ($V_{IT+} - V_{IT-}$) (see Note 7)		$0.1\ V_{CC}$	$0.3\ V_{CC}$	V
I_{OZ}	3-state-output high-impedance current (see Note 8)	$V_I = V_{CC}$ or GND		±10	µA
I_{IL}	Low-level input current (see Note 9)	V_I = GND		−1	µA
I_{IH}	High-level input current (see Note 10)	$V_I = V_{CC}$		1	µA

NOTES: 7. Applies for external input and bidirectional buffers with hysteresis.
8. The 3-state or open-drain output must be in the high-impedance state.
9. Specifications only apply with pullup terminator turned off.
10. Specifications only apply with pulldown terminator turned off.

standard voltage (5 V nominal)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = rated	$V_{CC}-0.8$		V
V_{OL}	Low-level output voltage	I_{OL} = rated		0.5	V
V_{IT+}	Positive-going input threshold voltage (see Note 7)			$0.7\ V_{CC}$	V
V_{IT-}	Negative-going input threshold voltage (see Note 7)		$0.2\ V_{CC}$		V
V_{hys}	Hysteresis ($V_{IT+} - V_{IT-}$) (see Note 7)		$0.1\ V_{CC}$	$0.3\ V_{CC}$	V
I_{OZ}	3-state-output high-impedance current (see Note 8)	$V_I = V_{CC}$ or GND		±10	µA
i_{IL}	Low-level input current (see Note 9)	V_I = GND		−1	µA
I_{IH}	High-level input current (see Note 10)	$V_I = V_{CC}$		1	µA

NOTES: 7. Applies for external input and bidirectional buffers with hysteresis.
8. The 3-state or open-drain output must be in the high-impedance state.
9. Specifications only apply with pullup terminator turned off.
10. Specifications only apply with pulldown terminator turned off.

XIN timing requirements over recommended operating free-air temperature range (see Figure 1)

		TEST CONDITIONS	MIN	MAX	UNIT
	Input frequency	V_{CC} = 3.3 V		50	MHz
		V_{CC} = 5 V		60	
t_{c1}	Cycle time, XIN	V_{CC} = 3.3 V	20		ns
		V_{CC} = 5 V	16.7		
t_{w1}	Pulse duration, XIN clock high	V_{CC} = 3.3 V	10		ns
		V_{CC} = 5 V	8		
t_{w2}	Pulse duration, XIN clock low	V_{CC} = 3.3 V	10		ns
		V_{CC} = 5 V	8		

clock switching characteristics over recommended operating free-air temperature range (see Figure 1)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{d1}	Delay time, XIN↑ to UARTCLK↑	V_{CC} = 3.3 V		14	ns
		V_{CC} = 5 V		8	
t_{d2}	Delay time, XIN↓ to UARTCLK↓	V_{CC} = 3.3 V		16	ns
		V_{CC} = 5 V		10	
t_{d3}	Delay time, XIN↑ to UARTCLK↓	V_{CC} = 3.3 V		19.8	ns
		V_{CC} = 5 V		13	
t_{d4}	Delay time, XIN↑ to UARTCLK↑	V_{CC} = 3.3 V		20.6	ns
		V_{CC} = 5 V		13.5	
t_{d5}	Delay time, XIN↓ to UARTCLK↑	V_{CC} = 3.3 V		21	ns
		V_{CC} = 5 V		13.8	

host CPU I/O read cycle timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 2 and Note 11)

		MIN	MAX	UNIT
t_{h1}	Hold time, HA(9–0) valid after $\overline{IORD}$↑	20		ns
t_{h2}	Hold time, $\overline{REG}$↑ valid after $\overline{IORD}$↑	0		ns
t_{w4}	Pulse duration, $\overline{IORD}$ low	165		ns
t_{su1}	Setup time, HA(9–0) valid before $\overline{IORD}$↓	70		ns
t_{su2}	Setup time, $\overline{CE}$x↓ before $\overline{IORD}$↓	5		ns
t_{h3}	Hold time, $\overline{CE}$x↑ after $\overline{IORD}$↑	20		ns
t_{h4}	Hold time, HD(7–0) valid after $\overline{IORD}$↑	0		ns
t_{su3}	Setup time, $\overline{REG}$↓ before $\overline{IORD}$↓	5		ns
t_{d6}	Delay time, HD(7–0) valid after $\overline{IORD}$↓		100	ns

NOTE 11. The maximum load on $\overline{INPACK}$ is one LSTTL with 50-pF total load. All timing is measured in nanoseconds.

host CPU I/O read cycle switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figure 2 and Note 11)

PARAMETER		MIN	MAX	UNIT
t_{d7}	Delay time, $\overline{INPACK}$↓ after $\overline{IORD}$↓		45	ns
t_{d8}	Delay time, $\overline{INPACK}$↑ after $\overline{IORD}$↑		45	ns

NOTE 11. The maximum load on $\overline{INPACK}$ is one LSTTL with 50-pF total load. All timing is measured in nanoseconds.

host CPU I/O write cycle timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 3)

		MIN	MAX	UNIT
t_{su4}	Setup time, HD(7–0) valid before $\overline{IOWR}\downarrow$	60		ns
t_{h5}	Hold time, HA(9–0) valid after $\overline{IOWR}\uparrow$	20		ns
t_{w6}	Pulse duration, $\overline{IOWR}$ low	165		ns
t_{su5}	Setup time, HA(9–0) valid before $\overline{IOWR}\downarrow$	70		ns
t_{h6}	Hold time, $\overline{REG}\uparrow$ after $\overline{IOWR}\uparrow$	0		ns
t_{su6}	Setup time, $\overline{CEx}\downarrow$ before $\overline{IOWR}\downarrow$	5		ns
t_{h7}	Hold time, $\overline{CEx}\uparrow$ after $\overline{IOWR}\uparrow$	20		ns
t_{su7}	Setup time, $\overline{REG}\downarrow$ before $\overline{IOWR}\downarrow$	5		ns
t_{h8}	Hold time, HD(7–0) valid after $\overline{IOWR}\uparrow$	30		ns

transmitter switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figure 4)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{d9}	Delay time, $\overline{SOUT}\downarrow$ after $\overline{IOWR}\uparrow$		8	24	Baud cycles
t_{d10}	Delay time, $\overline{IREQ}\downarrow$ after $\overline{SOUT}\downarrow$		8	8	Baud cycles
t_{d11}	Delay time, $\overline{IREQ}\downarrow$ after $\overline{IOWR}\uparrow$		16	32	Baud cycles
t_{d12}	Delay time, $\overline{IREQ}\uparrow$ after $\overline{IOWR}\uparrow$	C_L = 100 pF		140	ns
t_{d13}	Delay time, $\overline{IREQ}\uparrow$ after $\overline{IORD}\uparrow$	C_L = 100 pF		140	ns

receiver switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figure 5)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{d14}	Delay time, sample CLK↑ after RCLK↑			100	ns
t_{d15}	Delay time, $\overline{IREQ}\downarrow$ after SIN↓			1	RCLK cycles
t_{d16}	Delay time, $\overline{IREQ}\uparrow$ after $\overline{IORD}\uparrow$	C_L = 100 pF		150	ns

modem control switching characteristics over recommended ranges of operating free-air temperature and supply voltage, C_L = 100 pF (see Figure 6)

PARAMETER		MIN	MAX	UNIT
t_{d17}	Delay time, $\overline{RTS}$, $\overline{DTR}$, $\overline{OUT1}$, $\overline{OUT2}$ ↓ or ↑ after $\overline{IOWR}\uparrow$		50	ns
t_{d18}	Delay time, $\overline{IREQ}\downarrow$ after $\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}\downarrow$		30	ns
t_{d19}	Delay time, $\overline{IREQ}\uparrow$ after $\overline{IORD}\uparrow$		35	ns
t_{d20}	Delay time, $\overline{IREQ}\downarrow$ after $\overline{RI}\uparrow$		30	ns

host CPU attribute memory write cycle timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figures 7 and 8)

		MIN	MAX	UNIT
t_{c2}	Write cycle time, HA(9–0)	250		ns
t_{w8}	Pulse duration, $\overline{WE}$ low	150		ns
t_{su8}	Setup time, $\overline{CE}x\downarrow$ before $\overline{WE}\uparrow$	180		ns
t_{su9}	Setup time, HA(9–0) before $\overline{WE}\uparrow$ (see Note 12)	180		ns
t_{su10}	Setup time, HA(9–0) before $\overline{WE}\downarrow$ and $\overline{CE}x\downarrow$(see Note 12)	30		ns
t_{su11}	Setup time, $\overline{OE}\uparrow$ before $\overline{WE}\downarrow$	10		ns
t_{h9}	Hold time, HD(7–0) IN after $\overline{WE}\uparrow$	30		ns
t_{rec1}	Recovery time, HA(9–0) after $\overline{WE}\uparrow$	30		ns
t_{su12}	Setup time, HD(7–0) IN before $\overline{WE}\uparrow$	80		ns
t_{h10}	Hold time, $\overline{OE}\downarrow$ after $\overline{WE}\uparrow$	10		ns
t_{su13}	Setup time, $\overline{CE}x\downarrow$ before $\overline{WE}\downarrow$	0		ns
t_{h11}	Hold time, $\overline{CE}x\uparrow$ after $\overline{WE}\uparrow$	20		ns

NOTE 12. The $\overline{REG}$ signal timing is identical to address signal timing.

host CPU attribute memory write cycle switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figure 7)

	PARAMETER	MIN	MAX	UNIT
t_{dis1}	Disable time, HD(7–0) OUT after $\overline{WE}\downarrow$		100	ns
t_{dis2}	Disable time, HD(7–0) OUT after $\overline{OE}\uparrow$		100	ns
t_{en1}	Enable time, HD(7–0) OUT after $\overline{WE}\uparrow$	5		ns
t_{en2}	Enable time, HD(7–0) OUT after $\overline{OE}\downarrow$	5		ns

host CPU attribute memory read cycle timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 9)

		MIN	MAX	UNIT
t_{c3}	Read cycle time	300		ns
t_{d22}	Delay time, HD(7–0) after HA(9–0)		300	ns
t_{d23}	Delay time, HD(7–0) after $\overline{CE}x\downarrow$		300	ns
t_{d24}	Delay time, HD(7–0) after $\overline{OE}\downarrow$		150	ns
t_{h12}	Hold time, HD(7–0) after HA(9–0)	0		ns
t_{su14}	Setup time, $\overline{CE}x\downarrow$ before $\overline{OE}\downarrow$	0		ns
t_{h13}	Hold time, HA(9–0) after $\overline{OE}\uparrow$	20		ns
t_{su15}	Setup time, HA(9–0) before $\overline{OE}\downarrow$	30		ns
t_{h14}	Hold time, $\overline{CE}x\uparrow$ after $\overline{OE}\uparrow$	20		ns

host CPU attribute memory read cycle switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figure 9)

	PARAMETER	MIN	MAX	UNIT
t_{dis3}	Disable time, HD(7–0) after $\overline{CE}x\uparrow$		100	ns
t_{dis4}	Disable time, HD(7–0) after $\overline{OE}\uparrow$		100	ns
t_{en3}	Enable time, HD(7–0) after $\overline{CE}x\downarrow$	5		ns
t_{en4}	Enable time, HD(7–0) after $\overline{OE}\downarrow$	5		ns

subsystem Intel mode timing requirements (32 MHz) (see Figure 10)

INTEL SYMBOL	JEDEC SYMBOL		MIN	MAX	UNIT
t_{LHLL}	t_{w11}	Pulse duration, ALE high	48		ns
t_{AVLL}	t_{su16}	Setup time, SA8, SAD(7–0) valid to ALE low	21		ns
t_{PLLL}	t_{d25}	Delay time, $\overline{CS}$ low to ALE low	21		ns
t_{LLAX}	t_{h15}	Hold time, SA8, SAD(7–0) valid after ALE↓	21		ns
t_{LLWL}	t_{d26}	Delay time, ALE low to $\overline{WR}$ low	16		ns
t_{LLRL}	t_{d27}	Delay time, ALE low to $\overline{RD}$ low	16		ns
t_{WHLH}	t_{d28}	Delay time, $\overline{WR}$ high to ALE high	21		ns
t_{AFRL}	t_{d29}	Delay time, SA8, SAD(7–0) in high-impedance state to $\overline{RD}$ low	0		ns
t_{RLRH}	t_{w12}	Pulse duration, $\overline{RD}$ low	120		ns
t_{WLWH}	t_{w13}	Pulse duration, $\overline{WR}$ low	120		ns
t_{RHAX}	t_{d30}	Delay time, $\overline{RD}$ high to SA8, SAD(7–0) active	48		ns
t_{WHDX}	t_{h16}	Hold time, SA8, SAD(7–0) valid after $\overline{WR}$ high	48		ns
t_{WHPH}	t_{d31}	Delay time, $\overline{WR}$ high to $\overline{CS}$ high	21		ns
t_{RHPH}	t_{d32}	Delay time, $\overline{RD}$ high to $\overline{CS}$ high	21		ns
t_{PHPL}	t_{w14}	Pulse duration, $\overline{CS}$ high	21		ns

subsystem Zilog mode timing requirements (20 MHz) (see Figure 11)

ZILOG SYMBOL	JEDEC SYMBOL		MIN	MAX	UNIT
$t_{dA(AS)}$	t_{su17}	Setup time, SA8 and SAD(7–0) valid before $\overline{AS}$ high	20		ns
$t_{dAS(A)}$	t_{d33}	Delay time, $\overline{AS}$ high to SA8 and SAD(7–0) invalid	35		ns
$t_{dAS(DR)}$	t_{d34}	Delay time, $\overline{AS}$ high to data in on SAD(7–0)		150	ns
t_{wAS}	t_{w15}	Pulse duration, $\overline{AS}$ low	35		ns
$t_{dA(DS)}$	t_{d35}	Delay time, SA8 and SAD(7–0) invalid to $\overline{DS}$ low	0		ns
$t_{wDS(read)}$	t_{w16}	Pulse duration, $\overline{DS}$ low (read)	125		ns
$t_{wDS(write)}$	t_{w17}	Pulse duration, $\overline{DS}$ low (write)	65		ns
$t_{dDS(DR)}$	t_{d36}	Delay time, $\overline{DS}$ low to data in valid		80	ns
$t_{hDS(DR)}$	t_{h17}	Hold time, $\overline{DS}$ high to data in invalid	0		ns
$t_{dDS(A)}$	t_{h18}	Hold time, $\overline{DS}$ high to data out invalid	20		ns
$t_{dDS(AS)}$	t_{d37}	Delay time, $\overline{DS}$ high to $\overline{AS}$ low	30		ns
$t_{dDO(DS)}$	t_{d38}	Delay time, SAD(7–0) (write data from µP) valid to $\overline{DS}$ low	10		ns
$t_{dRW(AS)}$	t_{d39}	Delay time, R/$\overline{W}$ active to AS high	20		ns

subsystem Intel nonmultiplexed timing requirements (see Figure 12)

		MIN	MAX	UNIT
t_{su18}	Setup time, SA(8–0), $\overline{CS}$ valid to $\overline{RD}$, $\overline{WR}\downarrow$	30		ns
t_{w18}	Pulse duration, $\overline{RD}$ low	120		ns
t_{w19}	Pulse duration, $\overline{WR}$ low	120		ns
t_{su19}	Setup time, SAD(7–0) valid to $\overline{WR}\uparrow$	50		ns
t_{en4}	Enable time, $\overline{RD}\downarrow$ to SAD(7–0) driving	5		ns
t_{d40}	Delay time, $\overline{RD}\downarrow$ to SAD(7–0) valid		105	ns
t_{h19}	Hold time, SA(8–0), $\overline{CS}$ valid after $\overline{RD}$, $\overline{WR}\uparrow$	30		ns
t_{h20}	Hold time, SAD(7–0) valid after $\overline{WR}\uparrow$	30		ns
t_{dis3}	Disable time, $\overline{RD}\uparrow$ to SAD(7–0) high impedance	5	15	ns

subsystem Zilog nonmultiplexed timing requirements (see Figure 13)

		MIN	MAX	UNIT
t_{su20}	Setup time, SA(8–0), $\overline{CS}$, R/$\overline{W}$ valid to $\overline{DS}\downarrow$ (write)	90		ns
t_{su21}	Setup time, SA(8–0), $\overline{CS}$, R/$\overline{W}$ valid to $\overline{DS}\downarrow$ (read)	30		ns
t_{w20}	Pulse duration, $\overline{DS}$ low (write)	65		ns
t_{w21}	Pulse duration, $\overline{DS}$ low (read)	125		ns
t_{su22}	Setup time, SAD(7–0) valid to $\overline{DS}\uparrow$	50		ns
t_{en5}	Enable time, $\overline{DS}\downarrow$ to SAD(7–0) driving	5		ns
t_{d41}	Delay time, $\overline{DS}\downarrow$ to SAD(7–0) valid		105	ns
t_{h21}	Hold time, SA(8–0), $\overline{CS}$, R/$\overline{W}$ valid after $\overline{DS}\uparrow$	30		ns
t_{h22}	Hold time, SAD(7–0), $\overline{CS}$, R/$\overline{W}$ valid after $\overline{DS}\uparrow$	30		ns
t_{dis4}	Hold time, $\overline{DS}\uparrow$ to SAD(7–0) high impedance	5	15	ns

ARBCLK switching characteristics over recommended operating free-air temperature range (see Figure 14)

		TEST CONDITIONS	MIN	MAX	UNIT
t_{c4}	Cycle time, internal arbitration clock (ARBCLKI ÷ ARBPGM)	V_{CC} = 3.3 V	26	Note 13	ns
		V_{CC} = 5 V	14	Note 13	
t_{c5}	Cycle time, arbitration clock	V_{CC} = 3.3 V	26		ns
		V_{CC} = 5 V	14		
t_{d42}	Delay time, ARBCLKI↑ to ARBCLK0↑ (÷1)	V_{CC} = 3.3 V		13	ns
		V_{CC} = 5 V		7.3	
t_{d43}	Delay time, ARBCLKI↓ to ARBCLK0↓ (÷1)	V_{CC} = 3.3 V		15.5	ns
		V_{CC} = 5 V		10	
t_{d44}	Delay time, ARBCLKI↑ to ARBCLK0↑ (÷2)	V_{CC} = 3.3 V		15.3	ns
		V_{CC} = 5 V		8.8	
t_{d45}	Delay time, ARBCLKI↑ to ARBCLK0↓ (÷2)	V_{CC} = 3.3 V		17.5	ns
		V_{CC} = 5 V		11	
t_{d46}	Delay time, ARBCLKI↑ to ARBCLK0↑ (÷4)	V_{CC} = 3.3 V		19.5	ns
		V_{CC} = 5 V		11.5	
t_{d47}	Delay time, ARBCLKI↑ to ARBCLK0↓ (÷4)	V_{CC} = 3.3 V		21.5	ns
		V_{CC} = 5 V		13.5	
t_{d48}	Delay time, ARBCLKI↑ to ARBCLK0↑ (÷8)	V_{CC} = 3.3 V		22.7	ns
		V_{CC} = 5 V		13.5	
t_{d49}	Delay time, ARBCLKI↑ to ARBCLK0↓ (÷8)	V_{CC} = 3.3 V		25	ns
		V_{CC} = 5 V		15.7	

NOTE 13. t_{c4} max = N/6, where N = shortest (in ns) of the two attribute memory accesses, host CPU or subsystem.

reset timing requirements over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted) (see Figure 15)

		TEST CONDITIONS	MIN	MAX	UNIT
t_{w22}	Pulse duration, RESET active		$8 t_{c5}$		ns
t_{w23}	Pulse duration, RESET inactive		$8 t_{c5}$		ns
t_{d50}	Delay time, ARBCLKI↑ to $\overline{RST}$ low	V_{CC} = 3.3 V		10.4	ns
		V_{CC} = 5 V		7.5	
t_{d51}	Delay time, ARBCLKI↑ to $\overline{RST}$ high impedance	V_{CC} = 3.3 V		13.9	ns
		V_{CC} = 5 V		9.7	

subsystem interrupt request timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 16)

		MIN	MAX	UNIT
t_{d52}	Delay time, $\overline{WE}$↑ to IRQ↑ (see Note 14)	$2t_{c5}$	$3t_{c5}$	ARBCLKI cycles
t_{d53}	Delay time, SCR bit 6↑ to IRQ↓ (see Note 15)	t_{c5}	$2t_{c5}$	ARBCLKI cycles

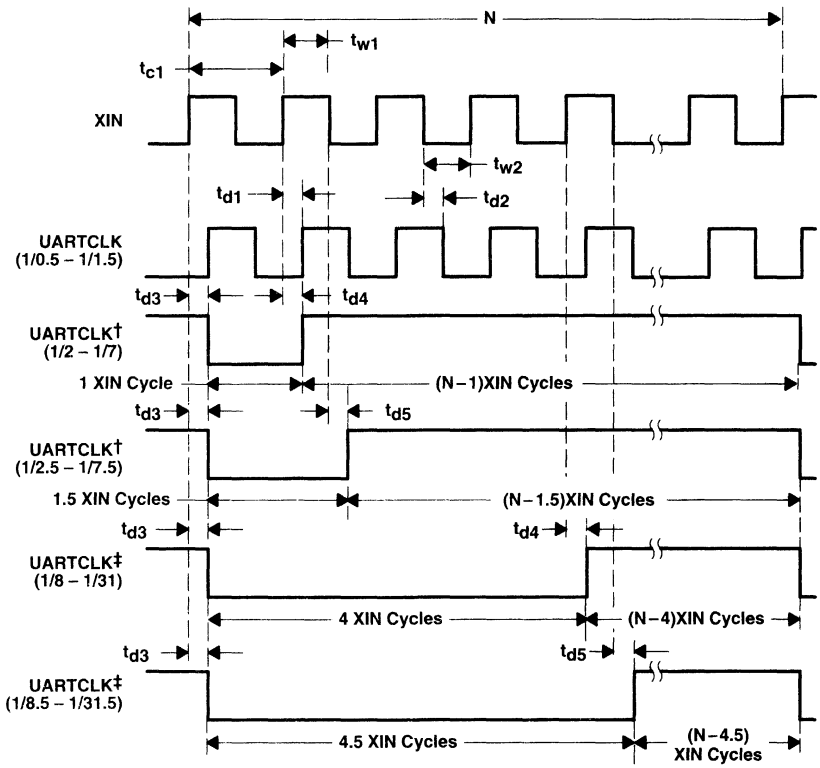
NOTES: 14. Synchronized to rising edge of ARBCLKI
15. Synchronized to falling edge of ARBCLKI

host CPU status change timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 17)

		MIN	MAX	UNIT
t_{d54}	Delay time, subsystem write↑ to $\overline{STSCHG}$↓ (see Note 14)	$2t_{c5}$	$3t_{c5}$	ARBCLKI cycles
t_{d55}	Delay time, $\overline{OE}$↓ to $\overline{STSCHG}$ high impedance (see Note 15)	t_{c5}	$2t_{c5}$	ARBCLKI cycles

NOTES: 14. Synchronized to rising edge of ARBCLKI
15. Synchronized to falling edge of ARBCLKI

PARAMETER MEASUREMENT INFORMATION

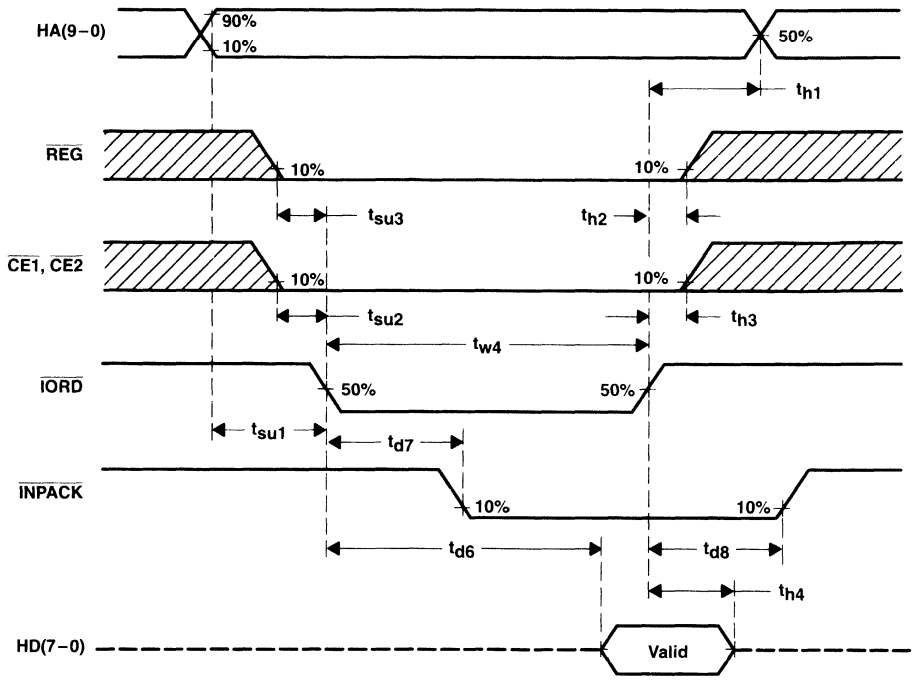


† The low portion of the UARTCLK cycle = 1 XIN cycle for PGMCLK integer values of 2 to 7 and 1.5 XIN cycles for PGMCLK noninteger values 2.5 to 7.5.

‡ The low portion of the UARTCLK cycle = 4 XIN cycles for PGMCLK integer values of 8 to 31 and 4.5 XIN cycles for PGMCLK noninteger values 8.5 to 31.5.

Figure 1. XIN Clock Timing Waveforms

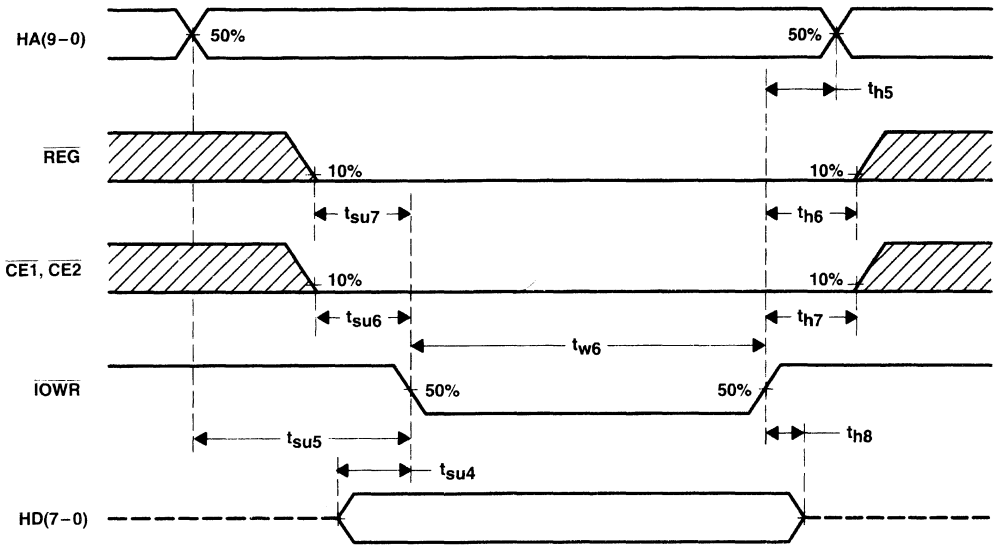
PARAMETER MEASUREMENT INFORMATION



NOTE A: All timings are measured at the card. Skews and delays from the system driver/receiver to the card must be accounted for by the system design.

Figure 2. Host CPU I/O Read Timing Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: All timings are measured at the card. Skews and delays from the system driver/receiver to the card must be accounted for by the system design.

Figure 3. Host CPU I/O Write Timing Waveforms

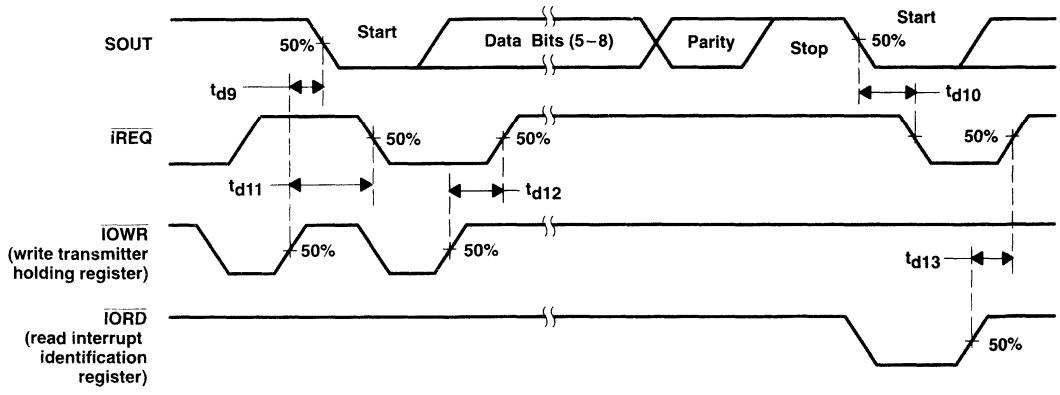


Figure 4. Transmitter Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

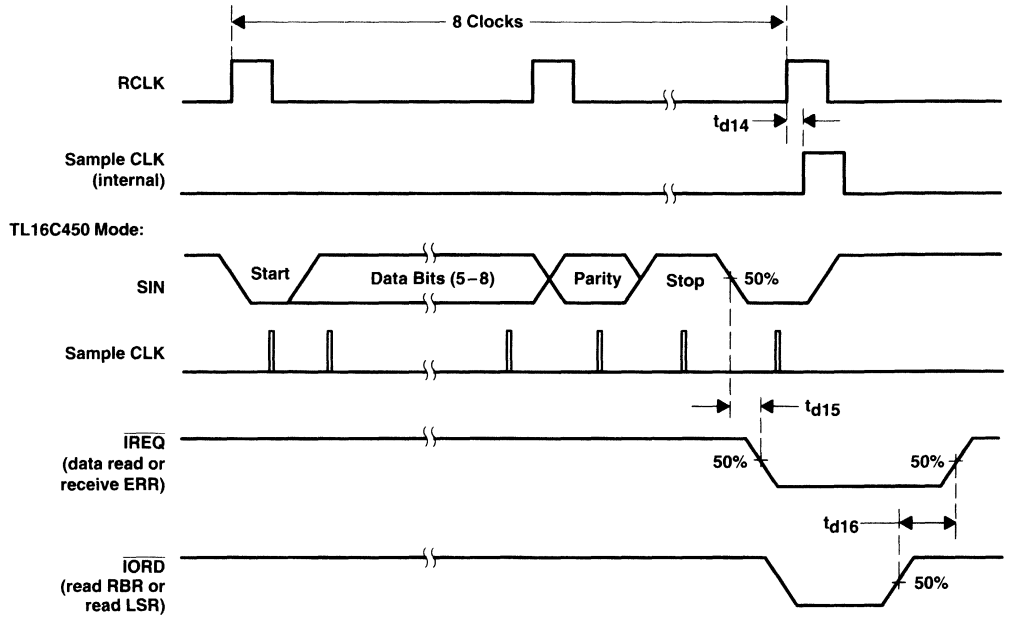


Figure 5. Receiver Timing Waveforms

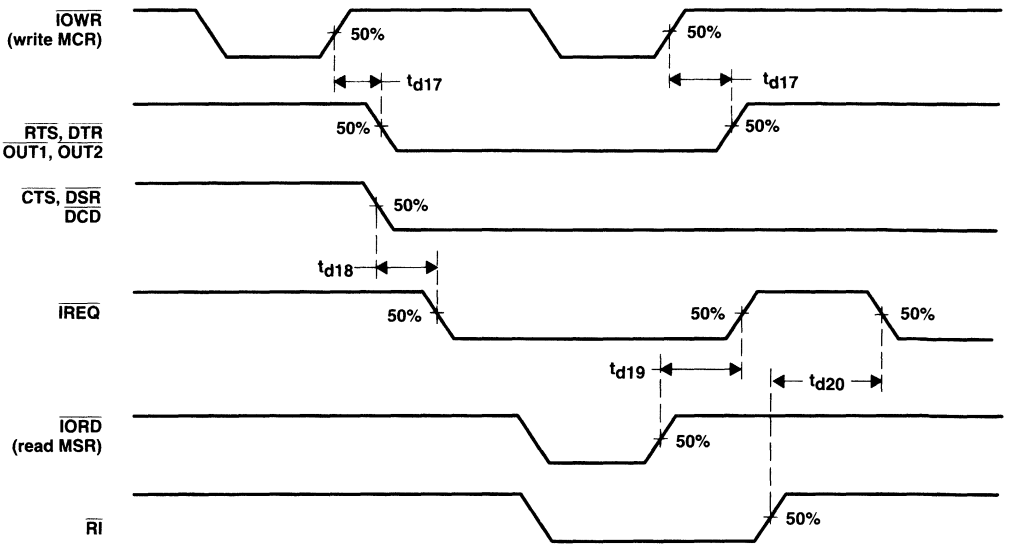
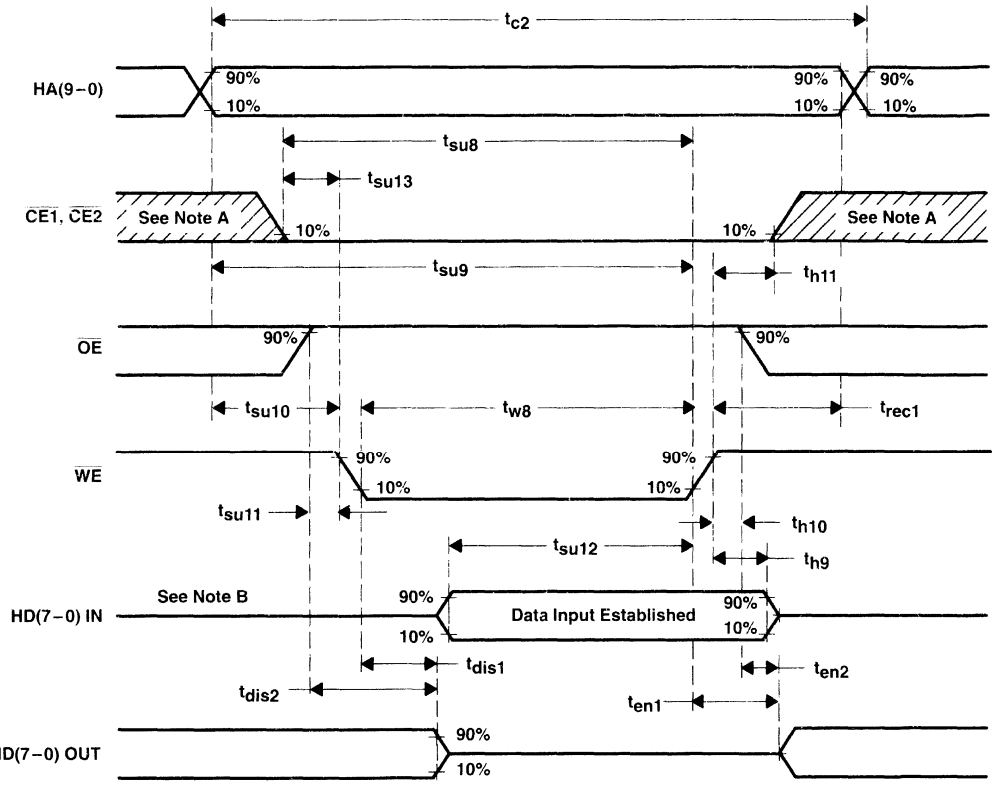


Figure 6. Modem Control Timing Waveforms

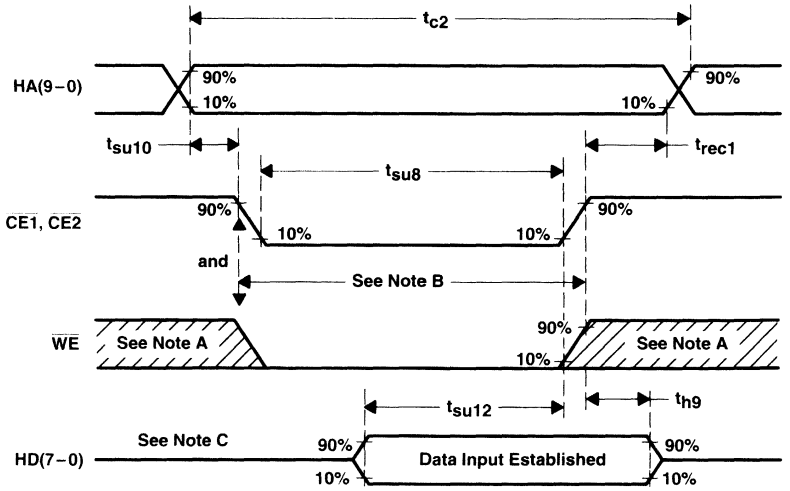
PARAMETER MEASUREMENT INFORMATION



NOTES: A. The hatched portion may be either high or low.
B. When the data I/O terminal is in the output state, no signals shall be applied to HD(7–0) by the system.

Figure 7. Host CPU Attribute Memory Write Timing Waveforms ($\overline{WE}$ Control)

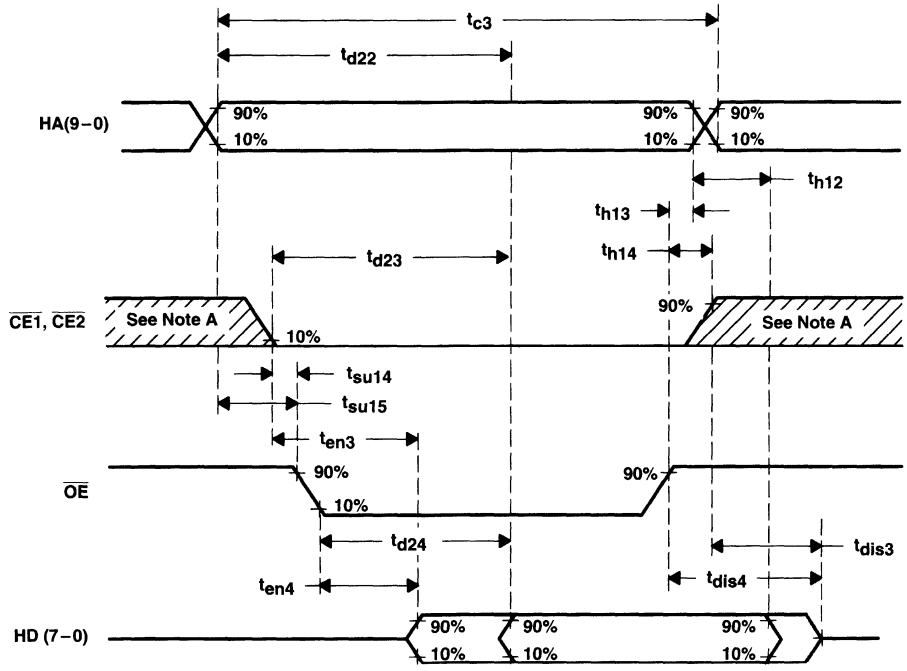
PARAMETER MEASUREMENT INFORMATION



NOTES: A. The hatched portion may be either high (H) or low (L).
B. $\overline{OE}$ must be high (H).
C. When the data I/O terminal is in the output state, no signals shall be applied to HD(7–0) by the system.

Figure 8. Host CPU Attribute Memory Write Timing Waveforms ($\overline{CE}$ Control)

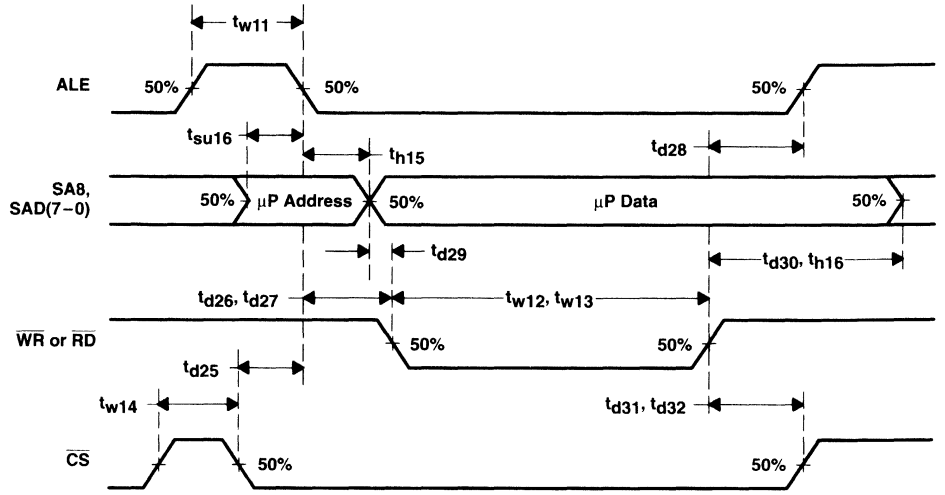
PARAMETER MEASUREMENT INFORMATION



NOTE A: The shaded portion may be either high or low.

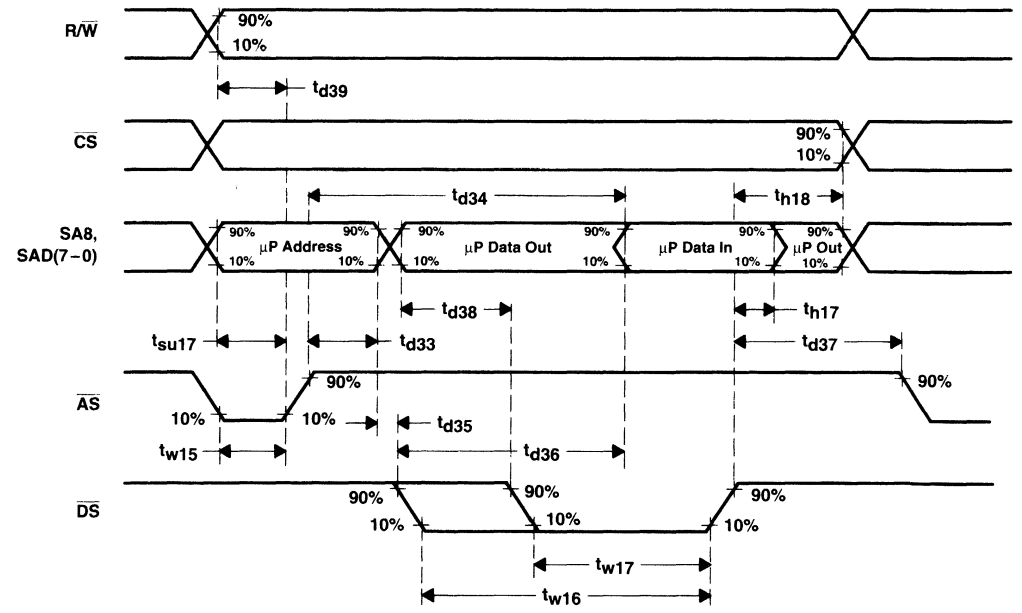
Figure 9. Host CPU Attribute Memory Read Timing Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: This figure is from the microprocessor perspective, not from the UART perspective.

Figure 10. Subsystem Intel Mode Timing Waveforms



NOTE A: This figure is from the microprocessor perspective, not from the UART perspective.

Figure 11. Subsystem Zilog Mode Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

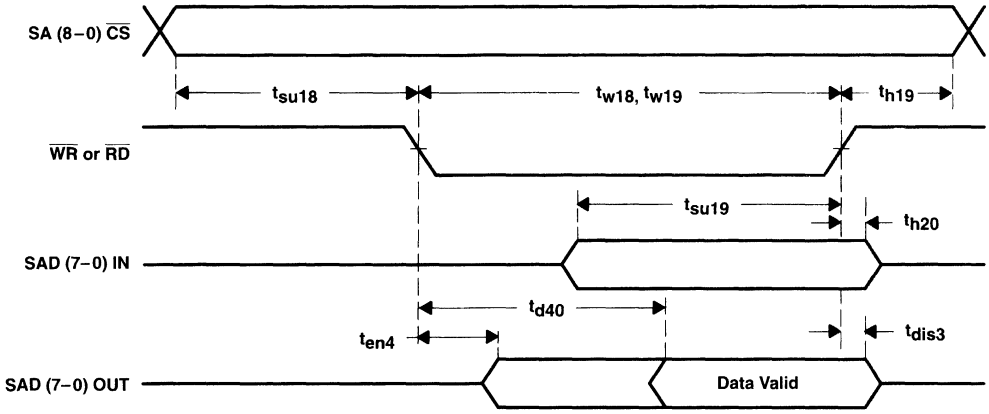


Figure 12. Subsystem Intel Nonmultiplexed Timing Waveforms

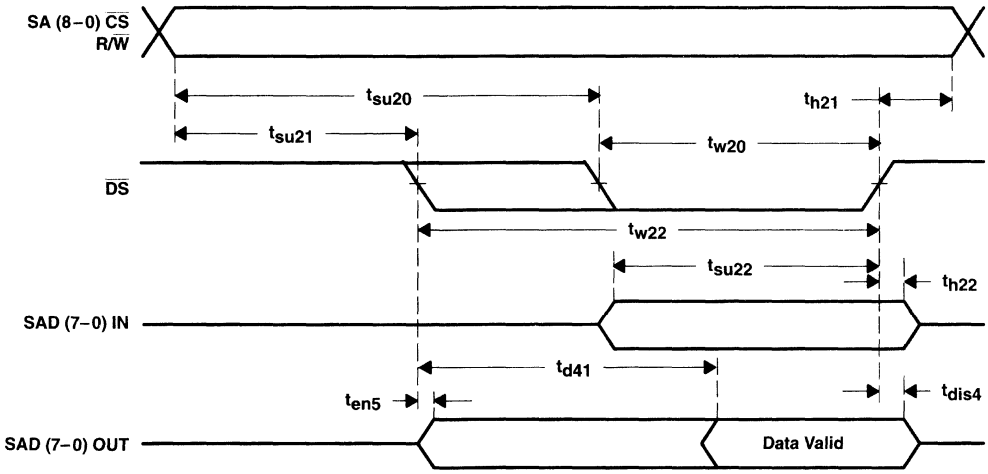


Figure 13. Subsystem Zilog Nonmultiplexed Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

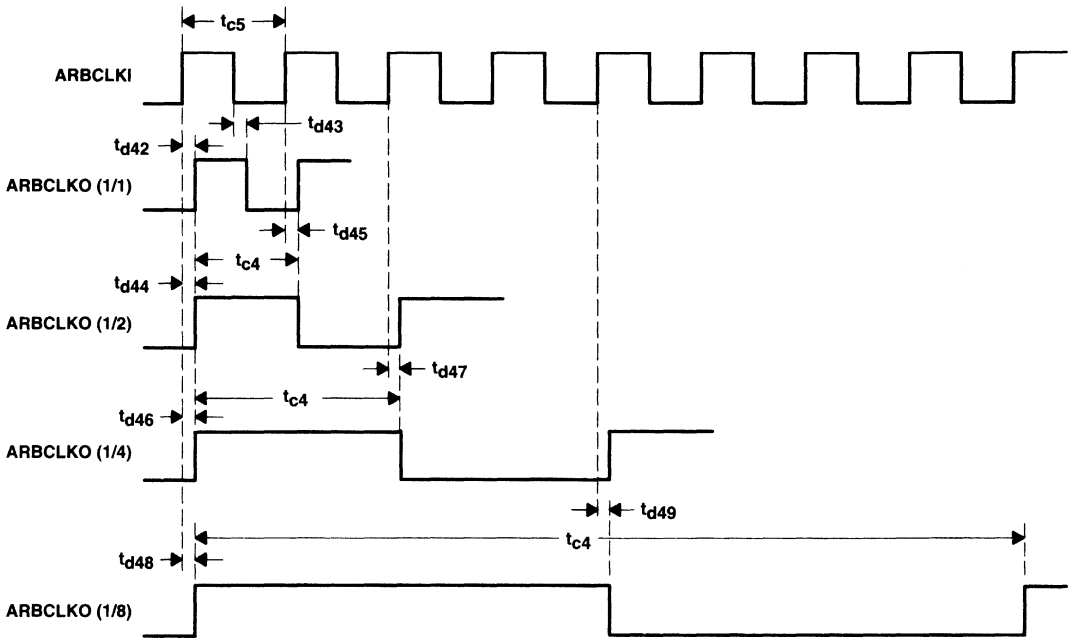


Figure 14. Arbitration Clock Timing Waveforms

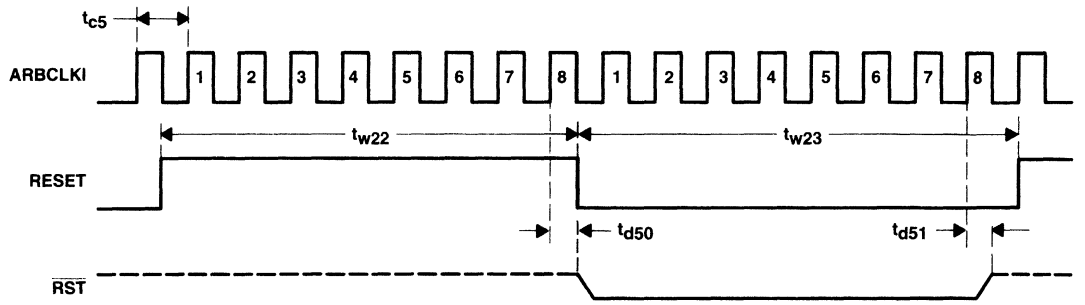


Figure 15. Reset Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

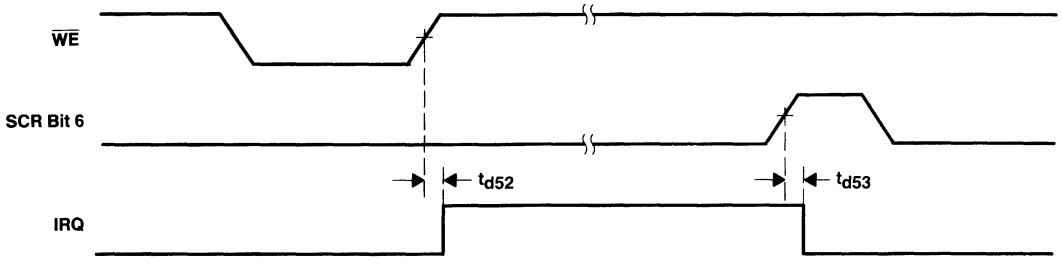


Figure 16. IRQ Timing Waveforms

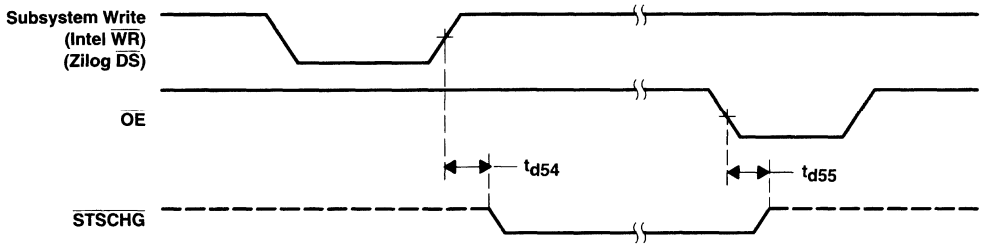
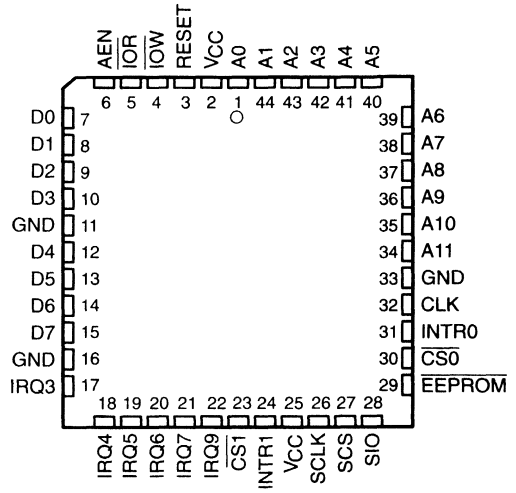


Figure 17. STSCHG Timing Waveforms

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

- **PnP Card Autoconfiguration Sequence Compliant**
- **Supports Two Logical Devices**
- **Decodes 10-Bit I/O Address Location With Programmable 1-, 2-, 4-, 8-, 16-Byte Block Size**
- **Maps Interrupts to Six Interrupt Outputs IRQ3–IRQ7 and IRQ9**
- **Provides Simple 3-Terminal Interface to SGS-Thomson EEPROM 2K/4K ST93C56/66 or Equivalent**
- **3-State Output EEPROM Interface Allows the EEPROM to be Accessed by Another Controller**
- **Provides Direct Connection to ISA/AT Bus**
- **Data and Interrupt Signals Require No Buffer**
- **Available in 44-Pin Plastic Leaded Chip Carrier (PLCC) and 48-Pin TQFP Package**

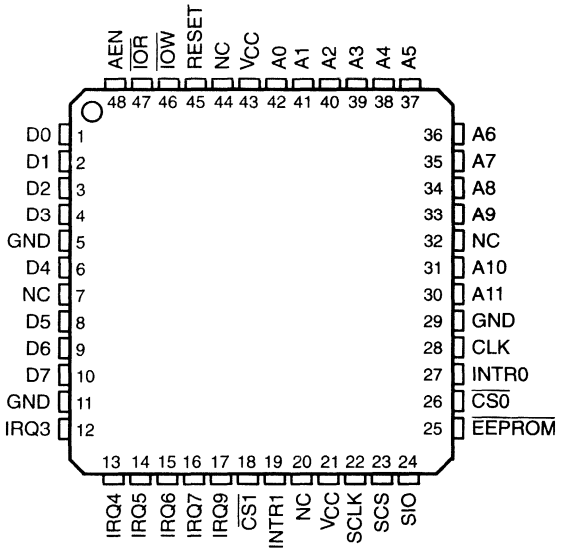
FN PACKAGE
(TOP VIEW)



description

The TL16PNP100A responds to the plug-and-play (PnP) autoconfiguration process. The process puts all PnP cards in a configuration mode, isolates one PnP card at a time, assigns a card-select number (CSN), and reads the card resource-data structure from the ST93C56/66 EEPROM. After the resource requirements and capabilities are determined for all cards, the process uses the CSN to configure the card by writing to the configuration registers. The TL16PNP100A implements configuration registers only for I/O applications with two logical devices, and DMA application support is not provided. Finally, the process activates the TL16PNP100A card and removes it from configuration mode. After the configuration process, the logic function can then start responding to industry standard architecture (ISA) bus cycles. The controller disables the EEPROM interface after the configuration is complete to allow another on-board controller to access the EEPROM.

PT PACKAGE
(TOP VIEW)



NC – No internal connection

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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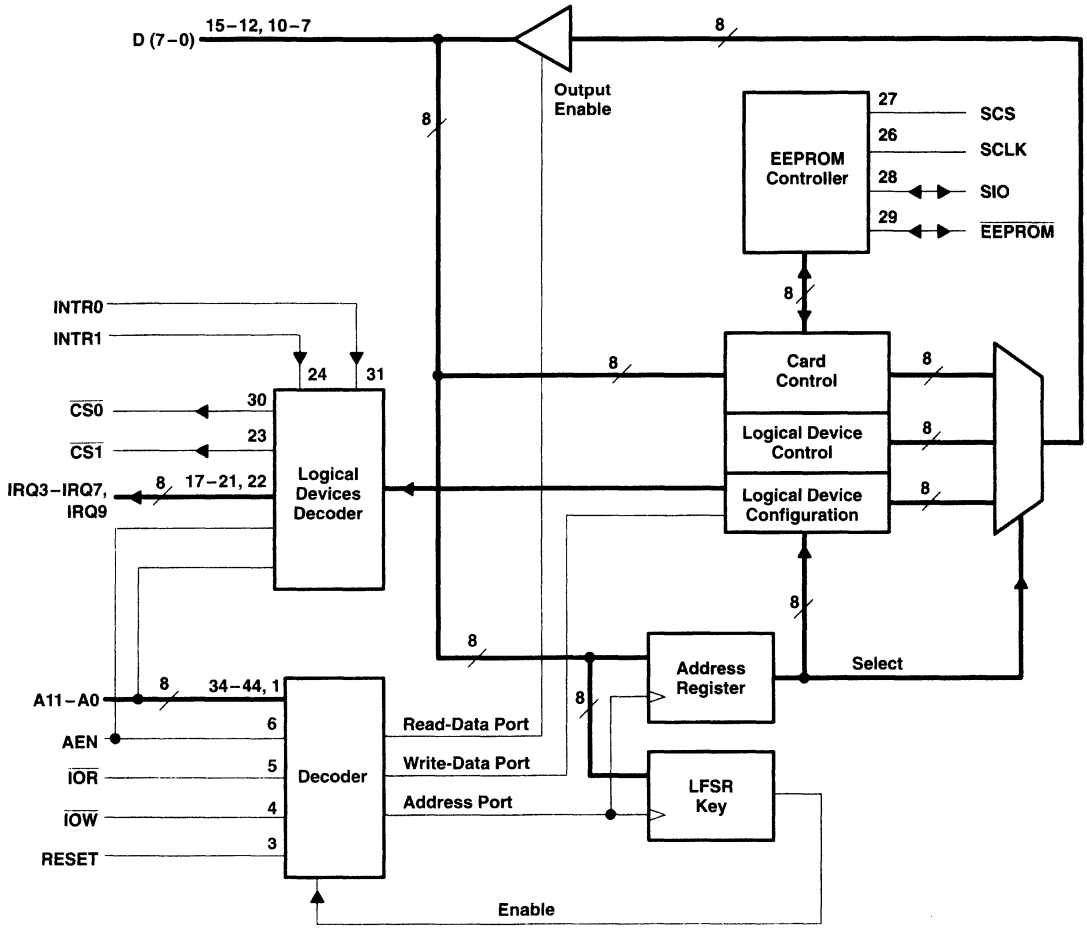
functional block diagram



NOTE A: Terminal numbers shown are for the FN package.

Terminal Functions

TERMINAL NAME	TERMINAL FN NO.	TERMINAL PT NO.	I/O	DESCRIPTION
A0 A11–A1	1 44–34	42 41–33, 31, 30	I	12-bit ISA address terminals. A0 and A1–A11 are all used during the PnP autoconfiguration sequence.
AEN	6	48	I	ISA address enable. During DMA operation, AEN is active and causes the controller to ignore the ISA transaction.
CLK	32	28	I	22-MHz external clock input. CLK synchronizes PnP logic and generates a 0.68-MHz SCLK.
$\overline{CS0}$	30	26	O	Chip select for logical device number 0. The address decoder only decodes a 10-bit address for one I/O location with programmable block size.
$\overline{CS1}$	23	18	O	Chip select for logical device number 1 . The address decoder only decodes a 10-bit address for one I/O location with programmable block size.
D0–D3 D4–D7	7–10 12–15	1–4 6,8 – 10	I/O	Data bus. Eight data lines with 3-state outputs provide a bidirectional path for data, control, and status information between the TL16PNP100A and the CPU. Output drive sinks 24 mA at 0.4 V and sources 12 mA at 2.4 V.
$\overline{EEPROM}$	29	25	I/O	EEPROM interface access enable. A 3-state bidirectional signal. When $\overline{EEPROM}$ is pulled low, the EEPROM interface is being accessed. A release state indicates the EEPROM interface is idle. A 100 μA pullup transistor is connected internally to this terminal.
GND	11, 16, 33	5, 11, 29		Ground (0 V). All terminals must be tied to GND for proper operation.
INTR0	31	27	I	Interrupt request from logical device number 0. INTR0 is an active-high signal.
INTR1	24	19	I	Interrupt request from logical device number 1. INTR1 is an active-high signal.
$\overline{IOR}$	5	47	I	ISA read input
$\overline{IOW}$	4	46	I	ISA write input
IRQ3–IRQ7 IRQ9	17–21 22	12–16 17	O	Interrupt request. INTRn request is mapped to one of the IRQs based on the value of the content of the interrupt request level (0x70) register. Output drive sinks 24 mA at 0.4 V and sources 12 mA at 2.4 V. These terminals are 3-state outputs.
RESET	3	45	I	Reset. When active (high), RESET clears most logical device registers and puts the TL16PNP100A in the wait-for-key state. The CSN is reset to 0x0. All configuration registers are set to their power-up values.
SCLK	26	22	I/O	Serial clock (3-state output path). SCLK controls the serial bus timing for address data. A 100 μA pulldown transistor is connected internally to this terminal.
SCS	27	23	I/O	EEPROM chip select (3-state output). SCS controls the activity of the EEPROM. A 100 μA pulldown transistor is connected internally to this terminal.
SIO	28	24	I/O	Serial input/output. A 3-state bidirectional EEPROM I/O data path. A 100 μA pulldown transistor is connected internally to this terminal.
V_{CC}	2, 25	21, 43		5-V supply voltage

detailed description

block size

This device generates read instructions for the $\overline{\text{EEPROM}}$. Read transactions consist of read opcode, address and data cycles. Data cycles are comprised of 2-byte DATA. After power up resets, this device reads the programmable block size value from address zero in the $\overline{\text{EEPROM}}$. Data [15:13] carries the block size information for logical device 0. Data [11:9] carries the block size information for the logical device 1 (see Table 1).

Table 1. Block Size

DATA [15:13]/[11:9]	BLOCK SIZE (Bytes)	ADDRESS BITS DECODED
000	1	[A9:A0]
001	2	[A9:A1]
010	4	[A9:A2]
100	8	[A9:A3]
111	16 (default)	[A9:A4]

$\overline{\text{EEPROM}}$ signal description

This device interfaces to SGS-Thomson's compatible EEPROM 2-Kbit ST93C56 or 4-Kbit ST93C66. After completion of the configuration sequence, it allows an optional on-board controller to access the EEPROM. During and after reset, TL16PNP100A gains access to the EEPROM by asserting $\overline{\text{EEPROM}}$ low, informing the optional on-board controller that it is accessing the EEPROM. After the configuration is complete, the device leaves the configuration mode, is activated, and is in the wait-for-key state. The $\overline{\text{EEPROM}}$ signal is then released and pulled high, SIO is released and pulled down, and SCS and SCLK are placed in the high-impedance state and pulled down.

NOTE

When the device enters the configuration mode again and leaves the wait-for-key state, it gains direct access to the EEPROM after the $\overline{\text{EEPROM}}$ signal is released. The wake command generates a read transaction from address 0×1, which is the beginning of the resource data of the card.

When the $\overline{\text{EEPROM}}$ signal is released, the interface of the EEPROM is idle. The TL16PNP100A drives the $\overline{\text{EEPROM}}$ signal low when the device enters the configuration mode again.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range at any input, V_I ..... −0.5 V to 7 V
Output voltage range, V_O ..... −0.5 V to 7 V
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Case temperature for 10 seconds: FN package ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2		V_{CC}	V
Low-level input voltage, V_{IL}	−0.5		0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −4 mA (see Note 1)	V_{CC}−0.8			V
		I_{OH} = −12 mA (see Note 2)	V_{CC}−0.8			
V_{OL}	Low-level output voltage	I_{OL} = 4 mA (see Note 1)			0.5	V
		I_{OL} = 24 mA (see Note 2)			0.5	
I_I	Input current	V_{CC} = 5.25 V, V_{SS} = 0, V_I = 0 to 5.25 V, All other pins floating			±1	µA
I_{OZ}	High-impedance-state output current	V_{CC} = 5.25 V, V_{SS} = 0, V_O = 0 to 5.25 V, Pullup transistors and pulldown transistors are off			±10	µA
I_{CC}	Supply current	V_{CC} = 5.25 V, T_A = 25°C, All inputs at 0.8 V, CLK at 4 MHz, No load on outputs			0.7	mA
$C_{i(CLK)}$	Clock input capacitance			15	20	pF
f_{CLK}	Clock frequency		10		22	MHz

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

NOTES: 1. These parameters apply for all outputs except D7–D0, IRQ3–IRQ7 and IRQ9.
2. These parameters only apply for D7–D0 and IRQ3–IRQ7 and IRQ9 outputs.

clock timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		ALTERNATE SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(SCLKH)}$	Pulse duration, SCLK high to low (see Note 3)	t_{CHCL}	See Figure 8	250		ns
$t_{w(SCLKL)}$	Pulse duration, SCLK low to high (see Note 3)	t_{CLCH}		250		ns
f_{CLK}	SCLK clock frequency (see Note 4)			0.3	0.68	MHz

NOTES: 3. The ST93C56 chip select, S, must be brought low for a minimum of 250 ns (t_{SLSH}) between consecutive instruction cycles according to the ST93C56 specification.
4. The SCLK signal is attained by internally dividing the frequency of the XIN signal by 32.

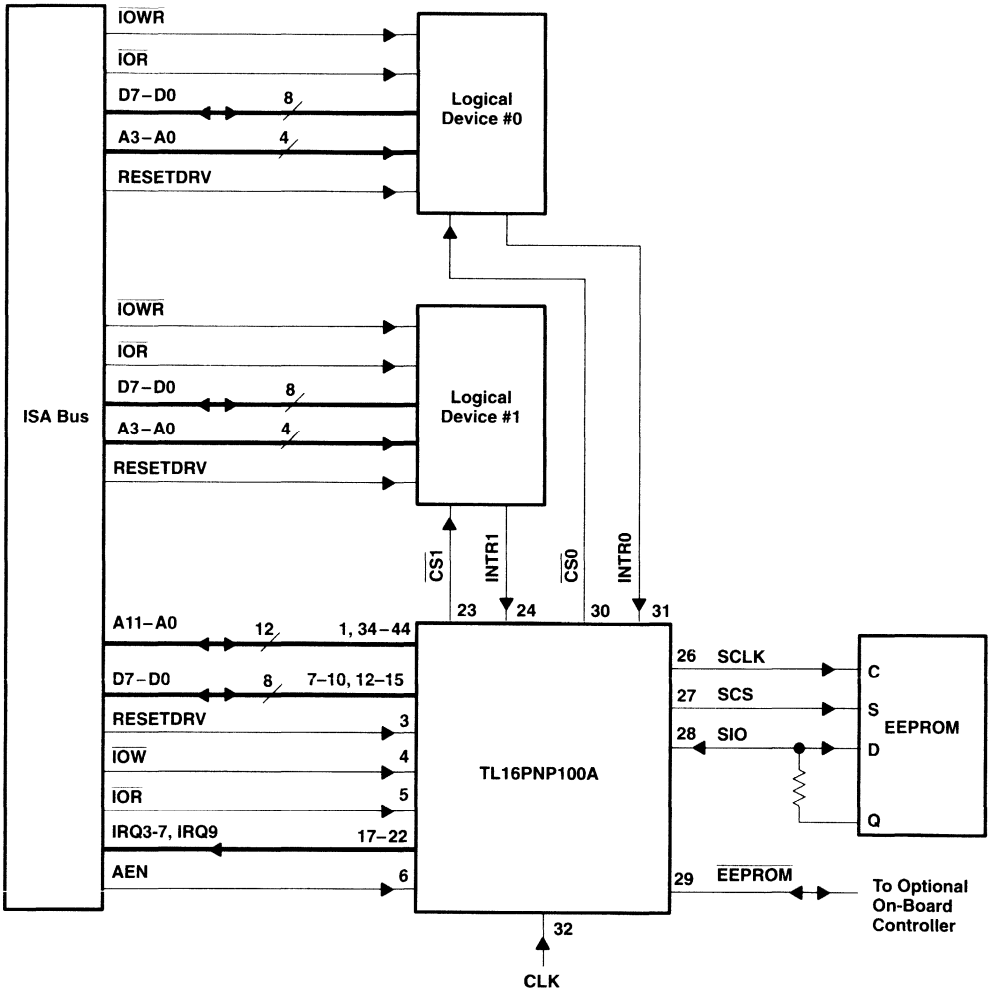
switching characteristics

PARAMETER		ALTERNATE SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
t_{d1}	Delay time, CS high to SCLK high	t_{SHCH}	See Figure 8	50		ns
t_{d2}	Delay time, SIO input valid to SCLK high	t_{DVCH}	See Figure 8 and Figure 9	100		ns
t_{pd1}	Propagation delay time, SCLK high to SIO level transition	t_{CHDX}		100		ns
t_{pd2}	Propagation delay time, SCLK high to output valid	t_{CHQV}	See Figure 9		500	ns
t_{pd3}	Propagation delay time, SCLK low to CS transition	t_{CLSL}			2	clock period
t_{d3}	Delay time, CS low to D/Q output Hi-Z	t_{SLQZ}			100	ns

system timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		ALTERNATE SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
t_{w1}	Pulse duration, write strobe, $\overline{IOW}$ low	t_{WR}	See Figure 5	2		clock periods
t_{w2}	Pulse duration, read strobe, $\overline{IOR}$ low	t_{RD}	See Figure 6	3		clock periods
t_{w3}	Pulse duration, master reset	t_{MR}		1		µs
t_{su1}	Setup time, data D7–D0 valid before $\overline{IOW}\uparrow$	t_{DS}	See Figure 5	15		ns
t_{h1}	Hold time, chip select $\overline{CSx}$ valid after address A0–A11 becomes invalid	t_{CH}	From the first rising edge of XIN after address becomes invalid, See Figure 5 and Figure 6		20	ns
t_{h2}	Hold time, data valid D7–D0 after $\overline{IOW}\uparrow$	t_{DH}	See Figure 5	5		ns
t_{d4}	Delay time, $\overline{CSx}$ valid after address A0–A11 valid	t_{CSRW}	From the first rising edge of XIN after address valid, See Figure 5 and Figure 6		30	ns
t_{h3}	Hold time, address A0–A11 valid after $\overline{IOW}\uparrow$	t_{AW}	See Figure 5	5		ns
t_{d5}	Delay time, $\overline{IOR}$ valid to data D0–D7 valid	t_{CSVD}	C_L = 45 pF after 2 clock periods, See Figure 6		30	ns
t_{d6}	Delay time, $\overline{IOR}\uparrow$ to floating data D0–D7	t_{HZ}	C_L = 45 pF, See Figure 6		20	ns
t_{d7}	Delay time, INTR0↑, INTR1↑, INTR0↓, or INTR1↓ to IRQ↑ or IRQ↓		See Figure 7		15	ns

APPLICATION INFORMATION



NOTE A: A 2-kΩ resistor should be inserted between D and Q. See the SGS-Thomson EEPROM 2K/4K ST93C56/66 application report.

Figure 1. Basic TL16PNP100A Configuration

APPLICATION INFORMATION

on-board EEPROM programming

This section describes a simple approach to programming the resource EEPROM in an expansion board that uses the TL16PNP100A. This approach involves utilizing a readily available standard EEPROM programmer and a ribbon cable in addition to minor additions to the expansion board.

A connector is needed on the expansion board to provide access to the EEPROM signals as shown in the diagram below. Two jumpers are also needed to isolate the EEPROM during programming. Power to the board must be removed before programming. To isolate the V_{CC} of the EEPROM from the board V_{CC}, Jumper 2 should be disconnected. This disables the PnP controller and prevents it from driving the EEPROM inputs. Jumper 1 should also be taken off during programming to isolate the D input and Q output. The PnP controller uses a single pin for the EEPROM data input and output.

The ribbon cable plugs into the on-board connector on one end, and the other end has a DIP connector that plugs into the EEPROM programmer.

Programming the EEPROM is achieved by connecting the unpowered board to the programmer using the ribbon cable, removing the jumper wires, and then using the software supplied with the programmer. After programming is complete, the jumper wires are reattached and the board is now ready for testing.

hardware required for programming an expansion board EEPROM

The hardware required for programming an expansion board EEPROM is listed in the following bulleted list and shown in Figure 2.

- EEPROM programmer
- Ribbon cable with connectors
- On-board connector and two jumper wires

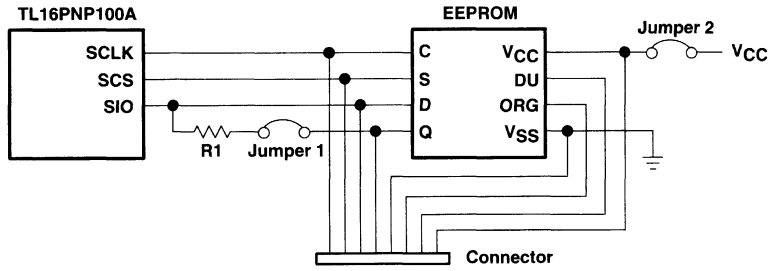


Figure 2. Programming an Expansion Board EEPROM

APPLICATION INFORMATION

32-byte I/O block size

The TL16PNP100A supports I/O block sizes ranging from 1 to 16 bytes. The following is one method to enable this device to support 32-byte I/O block size.

- Use only one logical device, and consequently one CS, either $\overline{CS0}$ or $\overline{CS1}$.
- In the first 2 bytes of the EEPROM select an I/O block size of 16 bytes for the selected logical device.
- In the EEPROM I/O descriptor resources, set the number of ports to 32 and the base address increment to 32.
- Use a NOR gate and an inverter to qualify address line A4 with the signal EEPROM as shown in Figure 3:

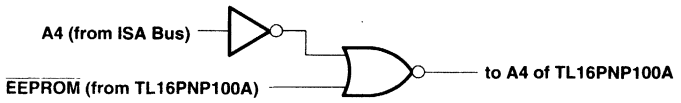


Figure 3. 32-Byte I/O Support

This operation forces A4 to 0 after completing the confirguration process ($\overline{EEPROM}$ signal is pulled up internally and goes high after the configuration process is complete.) When the address on the ISA bus is in the next 16 I/O addresses, only A4 changes from 0 to 1. Since A4 is being forced to 0, the TL16PNP100A thinks that the address is still in the 16-byte range and it asserts CS.

Example:

Using logical device 0:

- Connect $\overline{CS0}$ directly to the CS input of the device.
- Insert the NOR gate as described above.
- In the EEPROM, set the I/O block size to 0x00E0 (Blk_size = 16 bytes)
- The I/O descriptor in the EEPROM resources should be as follows:

```
I/O Port Descriptor 1
db      047h    ; Small item, type I/O port descriptor
db      000h    ; Information, [0] = 0, 10 bit decode
db      020h    ; Minimum base address [7:0]
db      002h    ; Minimum base address [15:8]
db      0e0h    ; Maximum base address [7:0]
db      003h    ; Maximum base address [15:8]
db      020h    ; Base address increment = 32
db      020h    ; Number of ports required = 32
```

APPLICATION INFORMATION

During configuration, assuming the system assigned the device address range 0x220 to 0x23F, $\overline{\text{EEPROM}}$ is low and A4 from the ISA bus passes to A4 on the TL16PNP100A. When configuration is complete $\overline{\text{EEPROM}}$ goes high, and A4 at the input of TL16PNP100A is reset to 0. Since the block size is 16, the TL16PNP100A looks at address bits A9 to A4. When the address on the A9 to A0 is in the range of 0x220 to 0x22F, A9 to A4 is:

A9	A8	A7	A6	A5	A4	A3	A1	A1	A0
1	0	0	0	1	0	X	X	X	X

and $\overline{\text{CS0}}$ is asserted low.

When the address is in the range of 0x230 to 0x23F, A9 to A4 is:

A9	A8	A7	A6	A5	A4	A3	A1	A1	A0
1	0	0	0	1	1	X	X	X	X

However, since A4 at the input of PNP100A is forced to 0, A9 to A4 is the same as in the range of 0x220 to 0x22F and TL16PNP100A asserts $\overline{\text{CS0}}$ low.

obtaining WIN95 logo

To obtain the WIN95 logo, the card should be able to decode 16-bit I/O address. Since the TL15PNP100A uses 10-bit address decoding, an OR gate is needed on-board to decode the upper 6 address bits (SA15-SA10). The customer can use this gate by changing the I/O port descriptors in the EEPROM to reflect the 16-BIT ISA address. However, the customer must make sure that the upper 6 BITS in the I/O port descriptors have the same minimum and maximum base in the address registers.

For example, a logical device requires a base address between 0200h and 0300h with an 8-byte as a base alignment and one I/O port requested. (Notice that the requested base address is such that the upper six bits in the minimum and maximum base address ranges are the same as in this example all are considered to be zeros). To meet the requested resources, the following steps must be done:

1. Modify the gate logic on the board as shown in Figure 4.

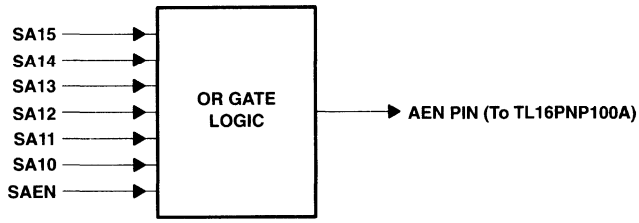


Figure 4. Gate Logic Modification

All the signals on the left side of the OR gate are ISA signals. Output AEN should be zero for valid I/O addresses.

APPLICATION INFORMATION

2. Program the I/O ports descriptors in the EEPROM as follows:

47h	I/O port descriptors with 7 bytes
01h	Information, bit [0] is set. The logical device is decoding full 16-bit ISA addresses
00h	Address bits [7:0] for minimum configuration base I/O address
02h	Address bits [15:8] for minimum configuration base I/O address
00h	Address bits [7:0] for maximum configuration base I/O address
03h	Address bits [15:8] for maximum configuration base I/O address
08h	Base alignment, which has a block size of 8 bytes
01h	One I/O port is needed

Using the above setup, the PnP BIOS maps the logical device to an address so that the upper six bits are always zeros. The logic 0 output from the OR gate occurs when SA15-SA10 and SAEN are low. This forces the logical device to check SA09-SA0 for a possible valid address.

PARAMETER MEASUREMENT INFORMATION

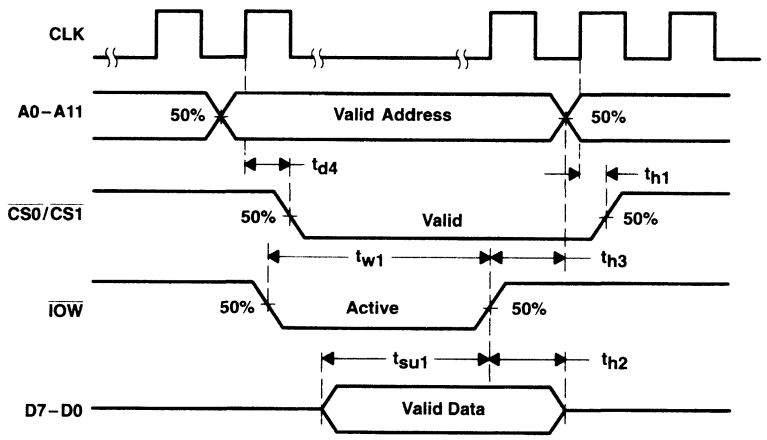


Figure 5. Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

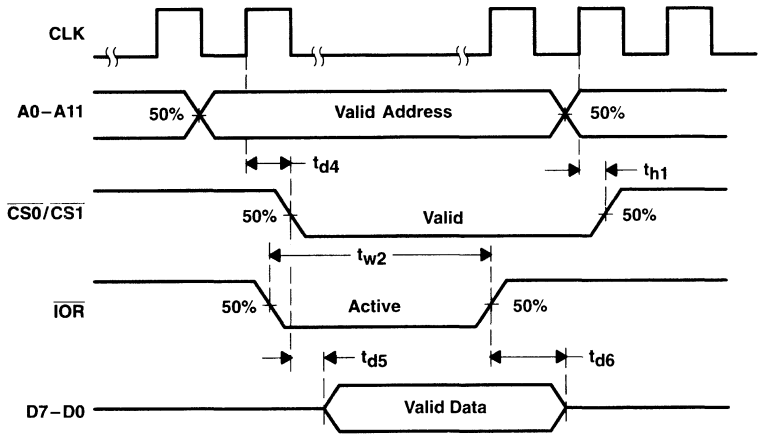


Figure 6. Read-Cycle Timing

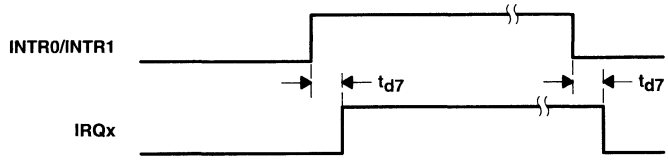


Figure 7. External Interrupt (EXINTR) Timing

PRINCIPLES OF OPERATION

PnP card configuration sequence

The PnP logic is quiescent on power up and must be enabled by software.

1. The initiation key places the PnP logic into configuration mode through a series of predefined writes to the ADDRESS port (see PnP Autoconfiguration Ports section).
2. A serial identifier is accessed in bit-sequence and used to isolate the ISA cards. Seventy-two READ_DATA port reads are required to isolate each card.
3. Once isolated, a card is assigned a CSN that is later used to select the card. This assignment is accomplished by programming the CSN.
4. The PnP software then reads the resource-data structure on each card. When all resource capabilities and demands are known, a process of resource arbitration is invoked to determine resource allocation for each card.
5. All PnP cards are then activated and removed from the configuration mode. This activation is accomplished by programming the ACTIVE register.

PnP autoconfiguration ports

Three 8-bit ports (see Table 2) are used by the software to access the configuration space on each ISA PnP card. These registers are used by the PnP software to issue commands, check status, access the resource data information, and configure the PnP hardware.

The ports have been chosen so as to avoid conflicts in the installed base of ISA functions, while at the same time minimizing the number of ports needed in the ISA I/O space.

Table 2. Autoconfiguration Ports

PORT NAME	LOCATION	TYPE
ADDRESS	0x0279 (printer status port)	Write only
WRITE_DATA	0x0A79 (printer status port + 0x0800)	Write only
READ_DATA	Relocatable in range 0x0203 to 0x03FF	Read only

The PnP registers are accessed by first writing the address of the desired register to the ADDRESS port, followed by a read of data from the READ_DATA port or a write of data to the WRITE_DATA port. Once addressed, the desired register may be accessed through the WRITE_DATA or READ_DATA ports.

The ADDRESS port is also the destination of the initiation key writes (see PnP ISA specification).

The address of the READ_DATA port is set by programming the SET RD_DATA PORT register. When a card cannot be isolated for a given READ_DATA port address, the READ_DATA port address is in conflict. The READ_DATA port address must then be relocated and the isolation process begun again. The entire range between 0x0203 and 0x3FF is available; however, in practice it is expected that only a few address locations are necessary before the software determines that PnP cards are not present.

PRINCIPLES OF OPERATION

PnP registers

PnP card standard registers are divided into three parts: card control, logical device control, and logical device configuration. There is exactly one of each card control register on each ISA card. Card control registers are used for global functions that control the entire card. Logical device control registers and logical device configuration registers are repeated for each logical device. Since the TL16PNP100A has two logical devices and they are intended only for I/O applications, not all the configuration registers are implemented.

PnP card control registers

The PnP card device control registers are listed in the following Table 3.

Table 3. PnP Card Control Registers

ADDRESS PORT VALUE	REGISTER NAME VALUE	READ/WRITE CAPABILITY	POWER UP
0x00	SET RD_DATA PORT	Write only	00 00 00 00
	Writing to this register modifies the address port used for reading from the PnP ISA card. Writing to this register is only allowed when the card is in the isolation state. Bit<7:0> Become I/O port address bits <9:2>.		
0x01	SERIAL ISOLATION	Read only	00 00 00 00
	Reading from this register causes a card in the isolation state to compare one bit of the board ID.		
0x02	CONFIGURATION CONTROL	Write only	0 00
	This 3-bit register consists of three independent commands, which are activated by writing a 1 to their corresponding register bits. These bits are automatically reset to 0 by the hardware after the commands execute. Bit<2> Writing a 1 to bit 1 causes the card to reset its CSN and RD-DATA port to zero. Bit<1> Writing a 1 to bit 2 causes the card to enter the wait-for-key state, but the card CSN is preserved and the logical device is unaffected. Bit<0> Writing a 1 to bit 0 resets the configuration registers of the logical device to their default state, and the CSN is preserved.		
0x03	WAKE[CSN]	Write only	00 00 00 00
	Writing to this register, when the write data [7:0] matches the card CSN, causes the card to go from the sleep state either to the isolation state when the write data for this command is zero, or to the configuration state when the write data is not zero. The pointer to the SERIAL IDENTIFIER is reset. This register is write only.		
0x04	RESOURCE DATA	Read only	00 00 00 00
	Reading from this register reads the next byte of resource information from the EEPROM. The STATUS register must be polled until its bit<0> is reset before this register may be read.		
0x05	STATUS	Read only	0
	Bit<0> A one-bit register that, when set, indicates it is okay to read the next data byte from the RESOURCE DATA register.		
0x06	CARD-SELECT NUMBER	Read/write	00 00 00 00
	Writing to this register sets a card CSN, which is uniquely assigned after the serial identification process. This allows each card to be individually selected during a Wake[CSN] command.		
0x07	LOGICAL DEVICE NUMBER	Read/write	00 00 00 00
	This register specifies which logical device is being configured.		

PRINCIPLES OF OPERATION

PnP logical device control registers

The registers in Table 4 are repeated for each logical device. These registers control device functions, such as enabling the device onto the ISA bus.

Table 4. PnP Logical Device Control Registers

ADDRESS PORT VALUE	REGISTER NAME VALUE	READ/WRITE CAPABILITY	POWER UP
0×30	ACTIVE	Read/write	00 00 00 00
	This register controls whether the logical device is active on the bus. Bit<7:1> This is reserved and must be set to zero. Bit<0> If set, activates the logical device. An inactive device does not respond to nor drive any ISA bus signals. Before a logical device is activated, I/O range check must be disabled.		
0×31	I/O RANGE CHECK	Read/write	00 00 00 00
	This register is used to perform a conflict check on the I/O port range programmed for use by the logical device. Bit<7:2> This is reserved and must be set to zero. Bit<1> If set, I/O range check is enabled. I/O range check is only valid when the logical device is inactive. Bit<0> If set, the logical device responds to I/O reads to its assigned I/O range with a 0×55 when I/O range check is in operation. If clear, the logical device responds with a 0×AA.		

PnP logical device configuration registers

The registers in Table 5 are repeated for each logical device and are used to program the ISA bus resource use of the device.

Table 5. PnP Logical Device Configuration Registers

ADDRESS PORT VALUE	REGISTER NAME VALUE	READ/WRITE CAPABILITY	POWER UP
0×60	I/O PORT BASE ADDRESS [15:8]	Read/write	00
	This register indicates the selected I/O lower limit address bits [15:8] for I/O descriptor 0. When the device is activated, if there is an address match to register 0×61 and an address match to this register, a chip select is generated to the logical device. Bit<7:2> Bits 15–10 are not supported, since the logical device uses 10-bit address decoding. Bit<1:0> Address bits 9 and 8 are indicated here.		
0×61	I/O PORT BASE ADDRESS [7:0]	Read/write	00 00 00 00
	This register indicates the selected I/O lower limit address bits [7:0] for I/O descriptor 0. When the device is activated, if there is an address match to register 0×60 and an address match to this register, a chip select is generated to the logical device. Bit<7:0> Address bits 7–0 are indicated here.		
0×70	INTERRUPT REQUEST LEVEL SELECT	Read/write	00 00
	This register indicates the selected interrupt level. Bit<3:0> Select the interrupt level. This device uses 6 interrupts from IRQ3 to IRQ7 and IRQ9.		
0×71	INTERRUPT REQUEST TYPE	Read/write	00 00
	This register indicates which type of interrupt is used for the selected interrupt level. Bit<7:2> This is reserved. Bit<1> Level, where 1 = high, 0 = low Bit<0> Type, where 1 = level, 0 = edge		
0×74	DMA CHANNEL SELECT 0	Read only	00 00 01 00
	This register has a value of 4 to indicate that DMA is not supported.		
0×75	DMA CHANNEL SELECT 1	Read only	00 00 01 00
	This register has a value of 4 to indicate that DMA is not supported.		

PRINCIPLES OF OPERATION

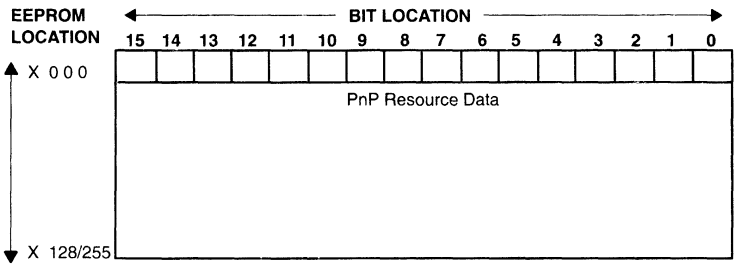
EEPROM

The TL16PNP100A has been designed to interface with the ST93C56/66 EEPROM (SGS-Thomson) or an equivalent. The EEPROM provides the block size for each device and the PnP resource data.

memory organization

The EEPROM should be organized as 128/255 words times 16 bits, so its ORG terminal should be connected to V_{CC} or left unconnected. The EEPROM memory organization is shown in Table 6.

Table 6. EEPROM Memory Organization



EEPROM READ (see Figure 8 and Figure 9)

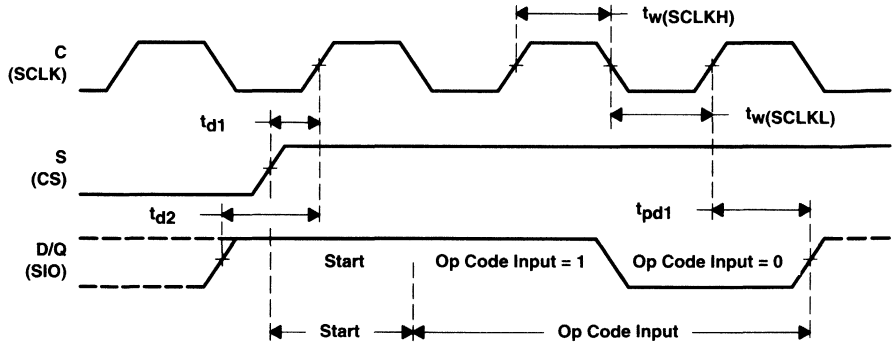
This device only supports read transactions. The READ op code instruction (10) must be sent to the EEPROM. The op code is then followed by an 8-bit-long address for the 16-bit word. The READ op code with accompanying address directs the EEPROM to output serial data on the EEPROM data terminals D and Q, which is connected to the TL16PNP100A bidirectional serial data bus (SIO). Specifically, when a READ op code and address are received, the instruction and address are decoded and the addressed EEPROM data is transferred into an output shift register in the EEPROM. Each read transaction consists of a start bit, 2-bit op code (10), 8-bit address, and 16-bit data. The TL16PNP100A does not accommodate the EEPROM autoaddress next-word feature.

READ op code transfer (see Figure 8)

Initially, the EEPROM chip select signal, S, which connects to the TL16PNP100A EEPROM chip select (CS), is raised. The EEPROM data, D and Q, then sample the TL16PNP100A SIO line on the following rising edges of the TL16PNP100A serial clock, SCLK, until a 1 is sampled and decoded by the EEPROM as a start bit. The TL16PNP100A SCLK signal connects to the EEPROM clock C. The READ op code (10) is then sampled on the next two rising edges of SCLK. TL16PNP100A sources the op code at the falling edges of SCLK.

PRINCIPLES OF OPERATION

READ op code transfer (continued)

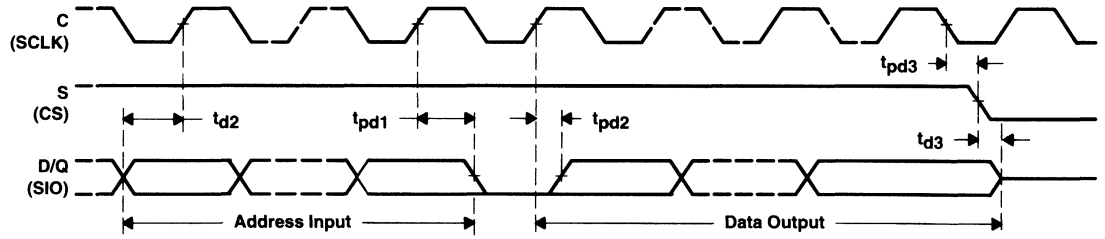


NOTE A: The corresponding TL16PNP100A terminal names are provided in parentheses. D/Q indicates that D and Q terminals in the EEPROMs are tied together through 2-kΩ resistor.

Figure 8. READ Op Code Transfer

READ address and data transfer (see Figure 9)

After receiving the READ op code, the EEPROM samples the READ address on the next eight rising edges of SCLK. The device sources the address at the falling edge of SCLK. The EEPROM then sends out a dummy 0 bit on the D/Q line, which is followed by the 16-bit data word with the MSB first. Output data changes are triggered by the rising edges of SCLK. The data is also read by the TL16PNP100A on the rising edges of SCLK.



NOTE A: The corresponding terminal names are provided in parentheses. D/Q indicates that D and Q terminals in the EEPROMs are tied together through 2-kΩ resistor.

Figure 9. READ Address and Data Transfer

- PnP Card Autoconfiguration Sequence Compliant
- External Terminal-to-Bypass PnP Autoconfiguration Sequence
- In UART Bypass Mode, the Stand-Alone PnP Controller is Configured With One Logical Device
- Provides 10-Interrupts IRQ3–IRQ7, IRQ9–IRQ12, IRQ15
- Simple 3-Pin Interface to SGS-Thomson™ EEPROM 2K/4K ST93C56/66
- High Output Current Drive. No External Buffer Needed for Data and Interrupt Signals
- Programmable Auto-RTS and Auto-CTS
- In Auto-CTS Mode, $\overline{CTS}$ Controls Transmitter
- In Auto-RTS Mode, Receiver FIFO Contents and Threshold Control RTS
- The Serial and Modem Control Outputs Drive a 1-Meter RJ11 Cable Directly if Equipment Is on the Same Power Drop
- Capable of Running With All Existing TL16C450 Software
- After Reset, All Registers Are Identical to the TL16C450 Register Set
- Clock Prescalar Allows 22-MHz Oscillator Clock to be Divided by 12, 6, 3, or 1
- In the TL16C450 Mode, Hold and Shift Registers Eliminate the Need for Precise Synchronization Between the CPU and Serial Data
- Programmable Baud Rate Generator Allows Division of Any Input Reference Clock by 1 to ($2^{16}-1$) and Generates an Internal 16× Clock
- On-Chip I/O Port Address Decoding
- In PnP Bypass Mode, 6 External Terminals Configure the I/O Base Address and Interrupt Mapping
- Adds or Deletes Standard Asynchronous Communication Bits (Start, Stop, and Parity) to or From the Serial Data Stream
- Independent Control of Transmit, Receive, Line Status, and Data Set Interrupts on Each Channel
- Programmable Serial Interface Characteristics:
  - 5-, 6-, 7-, or 8-Bit Characters
  - Even-, Odd-, or No-Parity-Bit Generation and Detection
  - 1-, 1 1/2-, or 2-Stop Bit Generation
  - Baud Generation (DC to 1 Mbit Per Second)
- False Start Bit Detection
- Complete Status Reporting Capabilities
- 3-State Outputs Provide TTL Drive for Bidirectional Data Bus and Interrupt Lines
- Line Break Generation and Detection
- Internal Diagnostic Capabilities:
  - Loopback Controls for Communications Link Fault Isolation
  - Break, Parity, Overrun, and Framing Error Simulation
- Fully Prioritized Interrupt System Controls
- Modem Control Functions (CTS, RTS, DSR, DTR, RI, and DCD)
- Transmitter and Receiver Run at the Same Speed
- Up to 16-MHz Clock Rate for Up to 1-Mbaud Operation for the Internal ACE
- Available in 68-Pin PLCC

description

The TL16PNP550A is a functional upgrade of the TL16C550C asynchronous communications element (ACE), which in turn is a functional upgrade of the TL16C450. Functionally equivalent to the TL16C450 on power up (character or TL16C450 mode), the TL16PNP550A, like the TL16C550C, can be placed in an alternate mode (FIFO mode). This relieves the CPU of excessive software overhead by buffering received and transmitted characters. The receiver and transmitter FIFOs store up to 16 bytes including three additional bits of error status

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description (continued)

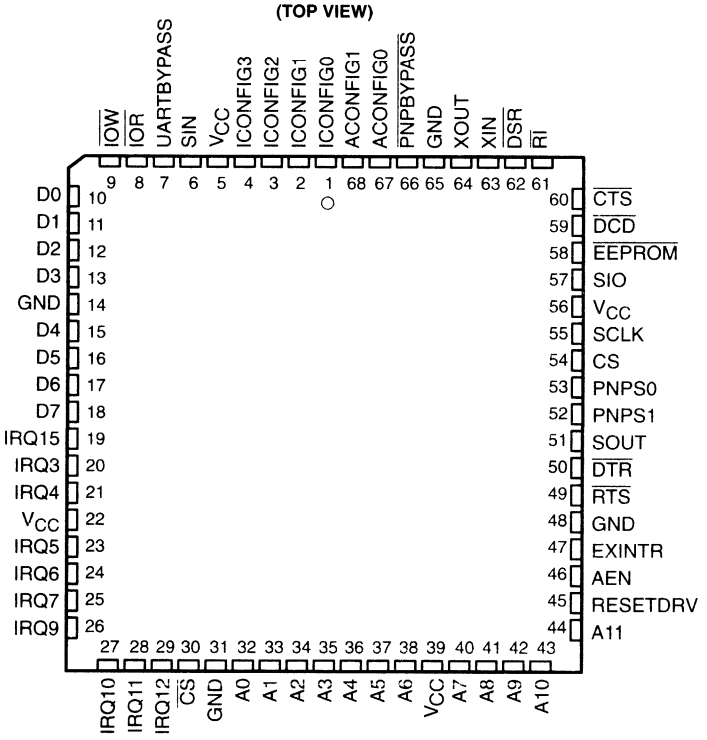
per byte for the receiver FIFO. In the FIFO mode, there is a selectable autoflow control feature that can significantly reduce software overload and increase system efficiency by automatically controlling serial data flow using $\overline{RTS}$ output and $\overline{CTS}$ input signals.

The TL16PNP550A responds to the plug-and-play (PnP) autoconfiguration process. The autoconfiguration process puts all PnP cards in a configuration mode, isolates one PnP card at a time, assigns a card select number (CSN), and reads the card resource data structure from the EEPROM. After the resource requirements and capabilities are determined for all cards, the autoconfiguration process uses the CSN to configure the card by writing to the configuration registers. The TL16PNP550A only implements configuration registers for I/O applications with one logical device and no direct memory access (DMA) support. Finally, the process activates the TL16PNP550A card and removes it from configuration mode. After the configuration process, the ACE starts responding to industry standard architecture (ISA) bus cycles. This device can also be configured to bypass the PnP autoconfiguration sequence. In this mode the TL16PNP500A can be configured to select the COM port address and IRQ level. In the UART bypass mode, the UART is disabled and this device is configured to be a stand-alone PnP controller that supports one logical device and no DMA support.

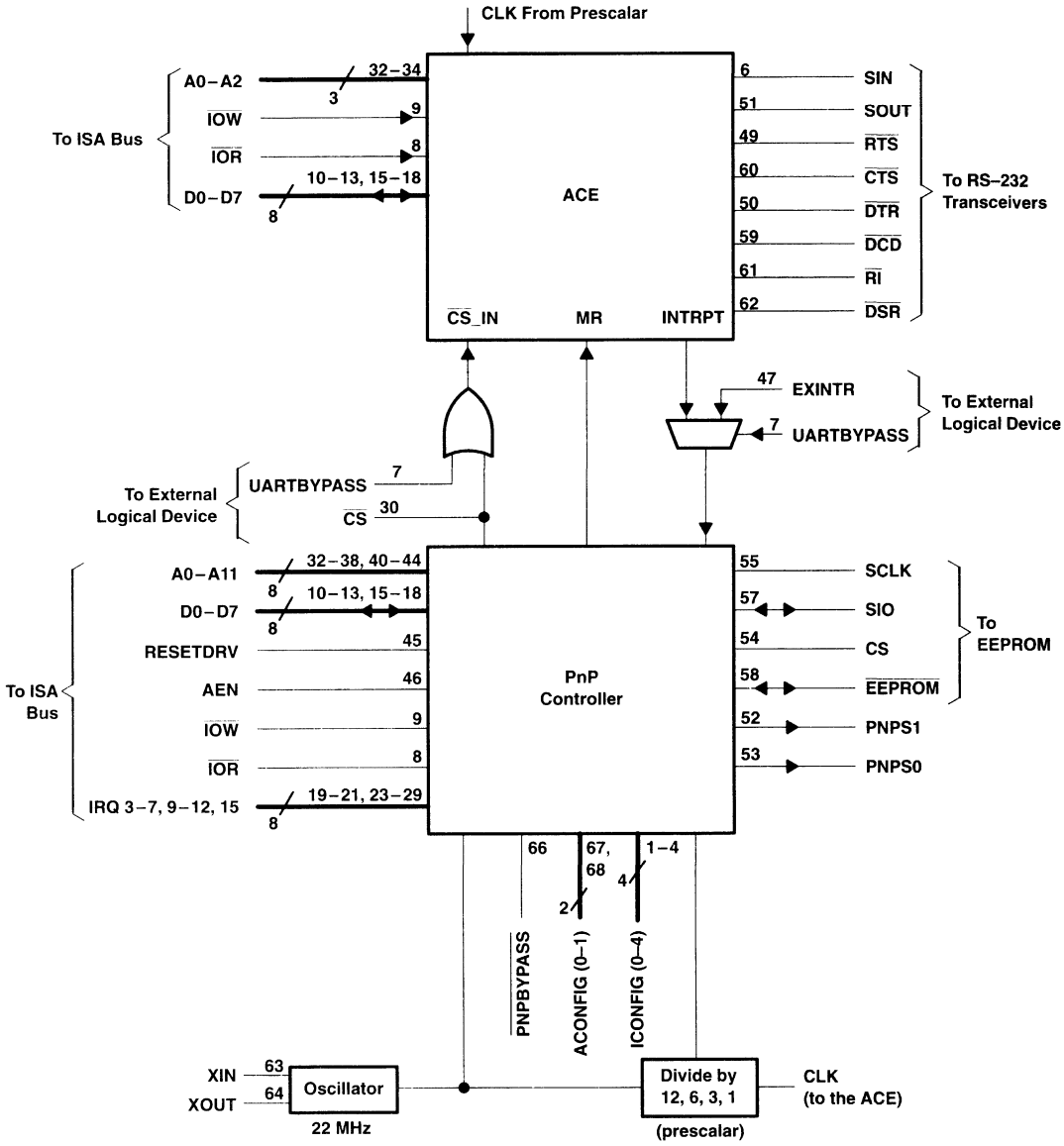
The TL16PNP550A performs serial-to-parallel conversion on data received from a peripheral device or modem and parallel-to-serial conversion on data received from its CPU. The CPU can read and report on the status of the ACE operation. Reported status information includes the type of transfer operation in progress, the status of the operation, and any error conditions encountered.

The TL16PNP550A includes a clock prescalar that divides the 22-MHz input clock by 12, 6, 3, or 1. The prescalar output clock is fed to the programmable baud rate generator, which is capable of dividing this clock by divisors from 1 to $(2^{16} - 1)$.

FN PACKAGE
(TOP VIEW)



functional block diagram



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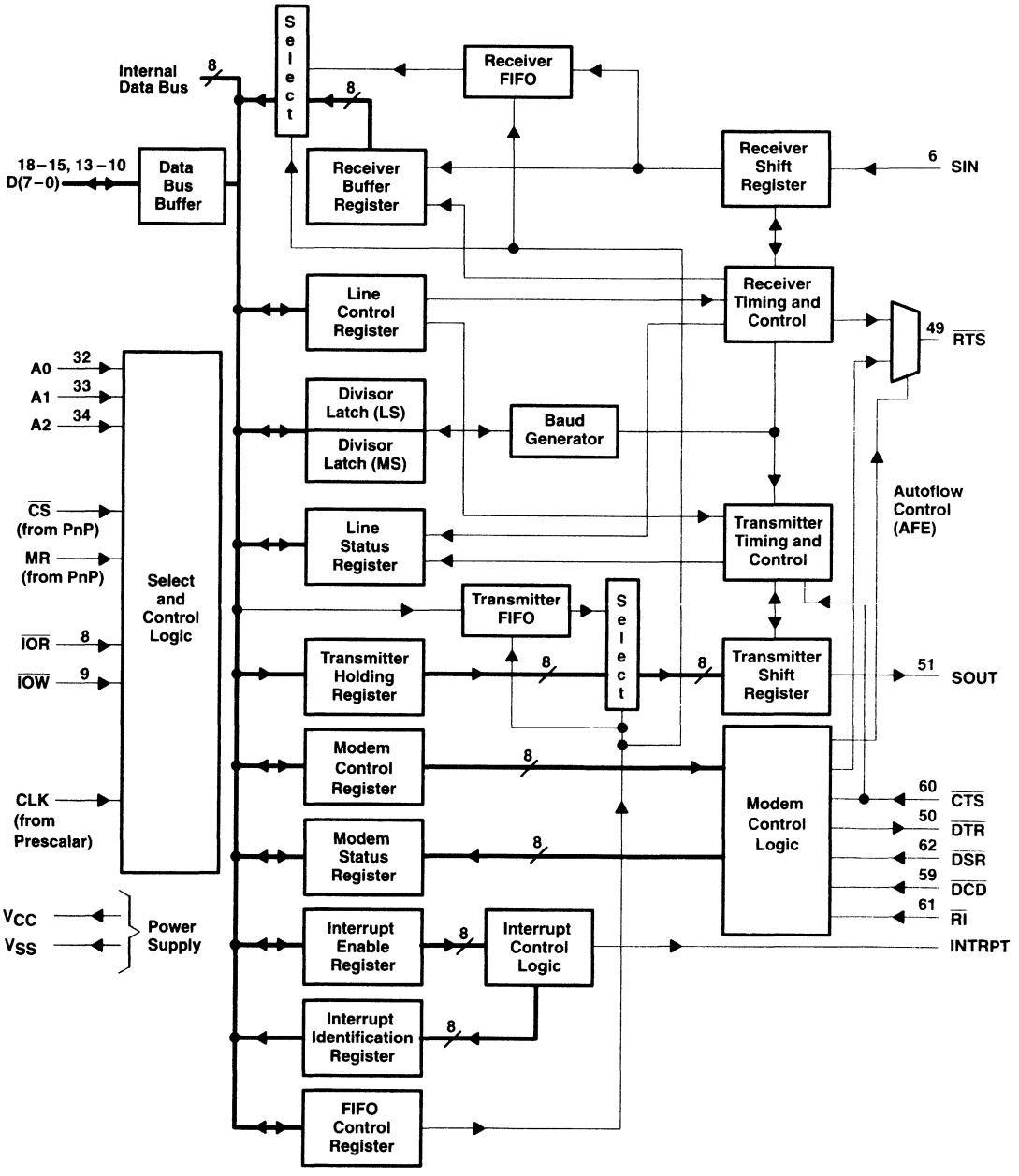
ACE functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO. FN	I/O	DESCRIPTION
A0–A6 A7–A11	32–38 40–44	I	12-bit ISA address terminals. All 12 bits are used during PnP autoconfiguration sequence. After autoconfiguration, bits A0–A2 select the ACE registers and bits A3–A9 are used in the address decoding to generate chip select for the device.
ACONFIG0, ACONFIG1	67, 68	I	Address configure. In PnP bypass mode, both ACONFIG0 and ACONFIG1 configure the COM port base address.
AEN	46	I	Address enable. AEN disables the ACE and PnP controller during DMA.
CS	54	O	Chip select. CS is a 3-state output. It controls the activity of the EEPROM. A 100 µA pulldown circuit is connected to this terminal.
$\overline{CS}$	30	O	Chip select. $\overline{CS}$ is the I/O chip select for the logical device.
$\overline{CTS}$	60	I	Clear to send. $\overline{CTS}$ is a modem status signal. Its condition can be checked by reading bit 4 (CTS) of the modem status register (MSR). Bit 0 (ΔCTS) of the modem status register indicates that this signal has changed states since the last read from the MSR. When the modem status interrupt is enabled when $\overline{CTS}$ changes states and the auto-CTS mode is not enabled, an interrupt is generated. $\overline{CTS}$ is also used in the auto-CTS mode to control the transmitter.
D0–D3 D4–D7	10–13 15–18	I/O	Data bus. D0 – D7 are eight data lines with 3-state outputs that provide a bidirectional path for data, control, and status information between the ACE and the CPU. The output drive sinks 24 mA at 0.4 V and sources 12 mA at 2.4 V.
$\overline{DCD}$	59	I	Data carrier detect. $\overline{DCD}$ is a modem status signal. Its condition can be checked by reading bit 7 (DCD) of the MSR. Bit 3 (ΔDCD) of the MSR indicates that this signal has changed levels since the last read from the MSR. When the modem status interrupt is enabled when $\overline{DCD}$ changes states, an interrupt is generated.
$\overline{DSR}$	62	I	Data set ready. $\overline{DSR}$ is a modem status signal. Its condition can be checked by reading bit 5 (DSR) of the MSR. Bit 1 (ΔDSR) of the MSR indicates this signal has changed states since the last read from the MSR. If the modem status interrupt is enabled when the $\overline{DSR}$ changes states, an interrupt is generated.
$\overline{DTR}$	50	O	Data terminal ready. When active (low), $\overline{DTR}$ informs a modem or data set that the ACE is ready to establish communication. $\overline{DTR}$ is placed in its active level by setting the DTR bit of the MCR. $\overline{DTR}$ is placed in its inactive level either as a result of a master reset, during loop mode operation, or clearing the DTR bit.
$\overline{EEPROM}$	58	I/O	EEPROM access. $\overline{EEPROM}$ is a 3-state bidirectional signal. When it is pulled low, either the TL16PNP550A or controller is accessing the EEPROM. A 100 µA pullup circuit is connected to this terminal.
EXINTR	47	I	External interrupt. During UARTBYPASS mode, the external logical device interrupt (EXINTR) is mapped to the configured IRQs.
GND	14, 31, 48, 65		Ground (0 V). These four GND terminals must be tied to ground for proper operation.
ICONFIG0– ICONFIG3	1–4	I	IRQ configure. In PnP bypass mode, ICONFIG0, ICONFIG2, and ICONFIG3 configure the required IRQ.
$\overline{IOR}$	8	I	Read input. When $\overline{IOR}$ is active while the ACE is selected, the CPU is allowed to read from the ACE.
$\overline{IOW}$	9	I	Write input. When $\overline{IOW}$ is active while the ACE is selected, the CPU is allowed to write to the ACE.
IRQ3–IRQ4 IRQ5–IRQ7 IRQ9–IRQ12 IRQ15	20–21 23–25 26–29 19	O	3-state interrupt requests. When active (high), IRQx informs the CPU that the ACE has an interrupt to be serviced. Four conditions that cause an interrupt to be issued are: a receiver error, received data is available or timed out (FIFO mode only), an empty transmitter holding register, or an enabled modem status interrupt. IRQx is generated when one or all of the above conditions occur and the value of bits 0–3 in the interrupt request level (0×70) is equal to x (of IRQx). The output drive sinks 24 mA at 0.4 V and sources 12 mA at 2.4 V.
$\overline{PNPBYPASS}$	66	I	Bypass PnP configuration sequence. When $\overline{PNPBYPASS}$ is tied to GND, the PnP autoconfiguration sequence is bypassed.
PNPS1– PNPS0	52–53	O	PnP internal states. See the PNPS1 and PNPS0 truth table in the PnP states section of this document.
RESETDRV	45	I	Reset. When active (high), RESETDRV clears most ACE registers and puts the ACE in wait for key state. The CSN is reset to 0×00. All configuration registers are set to their power-up values.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO. FN	I/O	DESCRIPTION
$\overline{RI}$	61	I	Ring indicator. $\overline{RI}$ is modem status signal. Its condition can be checked by reading bit 6 (RI) of the MSR. Bit 2 (TERI) of the MSR indicates that $\overline{RI}$ has transitioned from a low to a high level since the last read from the MSR. If the modem status interrupt is enabled when this transition occurs, an interrupt is generated.
$\overline{RTS}$	49	O	Request to send. When active, $\overline{RTS}$ informs the modem or data set that the ACE is ready to receive data. $\overline{RTS}$ is set to its active level low by setting the RTS modem control register bit and is set to its inactive (high) level either as a result of a master reset or during loop mode operations or by clearing bit 1 (RTS) of the MCR. In auto-RTS mode, $\overline{RTS}$ is set to its inactive level by the receiver threshold control logic.
SCLK	55	O	3-state EEPROM clock. SCLK is a 3-state EEPROM clock output that controls address and data transfer. A 100 μA pulldown circuit is connected to this terminal.
SIN	6	I	Serial data. SIN is input from a connected communications device.
SIO	57	I/O	3-State bidirectional EEPROM serial data bus. During output mode, SIO provides only read opcode and address which are sourced at the falling edge of SCLK. During input mode it provides the data which is captured at the rising edge of SCLK. A 100 μA pulldown circuit is connected to this terminal.
SOUT	51	O	Composite serial data output to a connected communication device. SOUT is set to the marking (high) level as a result of master reset.
UARTBYPASS	7	I	UART bypass. When it is active, UARTBYPASS disables the UART and the TL16PNP550A acts as a PnP stand-alone controller.
V_{CC}	5, 22, 39, 56		5-V supply voltage.
XIN, XOUT	63, 64	I/O	External clock. XIN and XOUT connect the TL16PNP550A to the main timing reference, a 22-MHz clock or crystal.

detailed description

autoflow control

Autoflow control is comprised of auto-CTS and auto-RTS. With auto-CTS, the input must be active before the transmitter FIFO can emit data (see Figure 1). Auto-RTS becomes active when the receiver needs more data and notifies the sending serial device (see Figure 1). When $\overline{RTS}$ is connected to $\overline{CTS}$, data transmission does not occur unless the receiver FIFO has space for the data; thus, overrun errors are eliminated if ACE1 and ACE2 are TL16PNP550As with enabled autoflow control. If autoflow control is not enabled, overrun errors occur when the transmit data rate exceeds the receiver FIFO read latency.

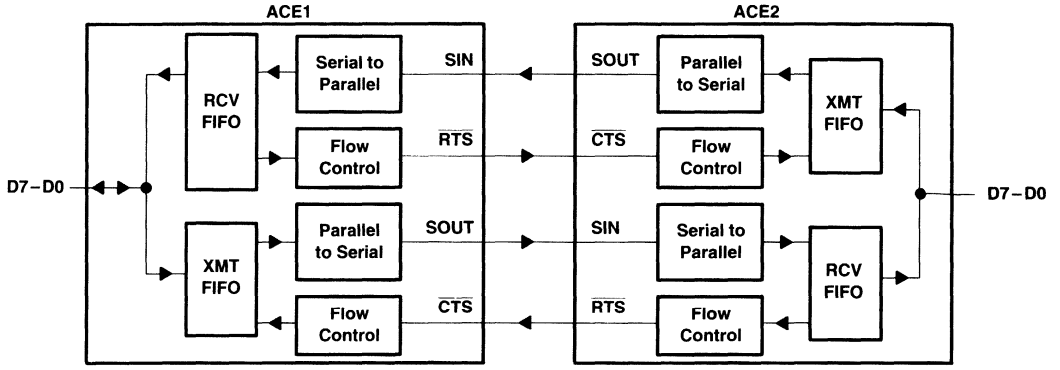


Figure 1. Autoflow Control Example (Auto-RTS and Auto-CTS)

auto-RTS (see Figure 1)

Auto-RTS data flow control originates in the receiver timing and control block (see functional block diagram) and is linked to the programmed receiver FIFO trigger level. When the receiver FIFO level reaches a trigger level of 1, 4, or 8, (see Figure 3), $\overline{RTS}$ is deasserted. With trigger levels of 1, 4, and 8, the sending ACE may send an additional byte after the trigger level is reached (assuming the sending ACE has another byte to send) because it may not recognize the deassertion of $\overline{RTS}$ until after it has begun sending the additional byte. $\overline{RTS}$ is automatically reasserted once the receiver FIFO is emptied by reading the receiver buffer register.

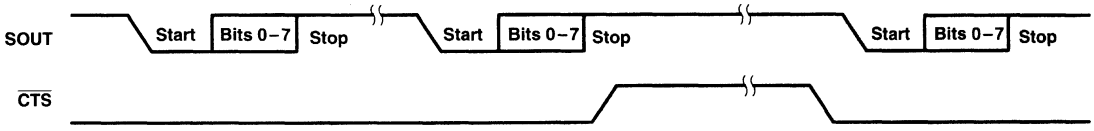
When the trigger level is 14 (see Figure 4), $\overline{RTS}$ is deasserted after the first data bit of the sixteenth character is present on the SIN line. $\overline{RTS}$ is reasserted when the receiver FIFO has at least one available byte space.

auto-CTS (see Figure 1)

The transmitter circuitry checks $\overline{CTS}$ before sending the next data byte. When $\overline{CTS}$ is active, it sends the next byte. To stop the transmitter from sending the following byte, $\overline{CTS}$ must be released before the middle of the last stop bit that is currently being sent (see Figure 2). The auto-CTS function reduces interrupts to the host system. When flow control is enabled, changes of $\overline{CTS}$ level do not trigger host interrupts because the device automatically controls its own transmitter. Without auto-CTS, the transmitter sends any data present in the transmit FIFO and a receiver overrun error may result.

enabling autoflow control and auto-CTS

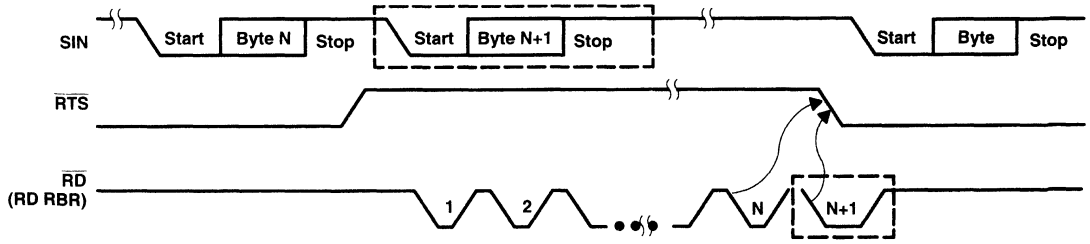
Autoflow control is enabled by setting modem control register bits 5 (autoflow enable or AFE) and 1 (RTS) to 1. Autoflow incorporates both auto-RTS and auto-CTS. If only auto-CTS is desired, bit 1 in the MCR should be cleared (this assumes a control signal is driving $\overline{CTS}$).



NOTE A: When $\overline{CTS}$ is low, the transmitter keeps sending serial data out. If $\overline{CTS}$ goes high before the middle of the last stop bit of the current byte, the transmitter finishes sending the current byte but it does not send the next byte. When $\overline{CTS}$ goes from high to low, the transmitter begins sending data again.

Figure 2. $\overline{CTS}$ Functional Timing Waveforms

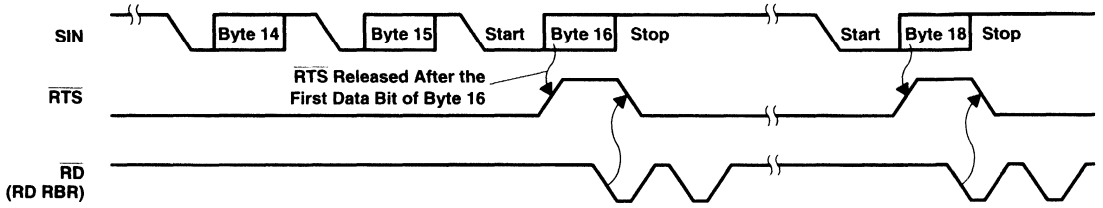
The receiver FIFO trigger level can be set to 1, 4, 8, or 14 bytes. These are described in Figures 3 and 4.



NOTES: A. N = receiver FIFO trigger level (1, 4, or 8 bytes)
B. The two blocks in dashed lines cover the case where an additional byte is sent as described in the preceding auto-RTS section.

Figure 3. $\overline{RTS}$ Functional Timing Waveforms, Receiver FIFO Trigger Level = 1, 4, or 8 Bytes

enabling autoflow control and auto-CTS (continued)



NOTES: A. $\overline{RTS}$ is deasserted when the receiver receives the first data bit of the sixteenth byte. The receiver FIFO is full after finishing the sixteenth byte.
B. $\overline{RTS}$ is asserted again when there is at least one byte of space available and no incoming byte is in processing or there is more than one byte of space available.
C. When the receiver FIFO is full, the first receiver buffer register read reasserts $\overline{RTS}$.

Figure 4. $\overline{RTS}$ Functional Timing Waveforms, Receiver FIFO Trigger Level = 14 Bytes

flow control and interrupt

When flow control is enabled, bit 0 (ΔCTS) of the modem status register does not cause a modem status interrupt. The ACE accommodates a 1-Mbaud serial rate (16-MHz input clock) so that a bit time is 1 μs, and a typical character time is 10 μs (start bit, 8 data bits, and a stop bit).

The TL16PNP550A ACE includes a programmable, on-board, baud rate generator that divides a reference clock input by 1 to $(2^{16}-1)$ for producing a 16 × clock to drive the internal transmitter logic. Provisions are included to use this 16 × clock to drive the receiver logic. The ACE includes complete modem control capability and a processor interrupt system that may be software tailored to minimize the system overhead for handling the communications link.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.5 V to 7 V
Input voltage range at any input, V_I . . . . . −0.5 V to 7 V
Output voltage range, V_O . . . . . −0.5 V to 7 V
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Case temperature for 10 seconds, T_C: FN package . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2		V_{CC}	V
Low-level input voltage, V_{IL}	−0.5		0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}‡	High-level output voltage	I_{OH} = –12 mA	V_{CC}–0.8			V
V_{OL}‡	Low-level output voltage	I_{OL} = 24 mA			0.5	V
V_{OH}	High-level output voltage	I_{OH} = –4 mA (see Note 2), V_{CC} = 0.8 V	V_{CC}–0.8			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA (see Note 2)			0.5	V
I_I	Input current	V_{CC} = 5.25 V, V_{SS} = 0, V_I = 0 to 5.25 V, All other terminals floating			±1	µA
I_{OZ}	High-impedance-state output current	V_{CC} = 5.25 V, V_{SS} = 0, V_O = 0 to 5.25 V, Pullup and pulldown circuits are off			±10	µA
I_{CC}	Supply current	V_{CC} = 5.25 V, T_A = 25°C, SIN, $\overline{DSR}$, $\overline{DCD}$, $\overline{CTS}$, and $\overline{RI}$ at 2 V, All other inputs at 0.8 V, Clock at 4 MHz (no crystal used), No load on outputs, Baud rate = 50 kbit/s			5	mA
$C_{i(CLK)}$	Clock input capacitance	V_{CC} = 0, V_{SS} = 0, f = 1 MHz, T_A = 25°C, All other terminals grounded		15	20	pF
$C_{o(CLK)}$	Clock output capacitance			20	30	pF
C_i	Input capacitance			6	10	pF
C_o	Output capacitance			10	20	pF
$f_{(XIN-XOUT)}$	Oscillator speed (XIN and XOUT)		16		22	MHz

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ These parameters apply only for IRQx and D7–D0.
NOTE 2: These parameters apply for all outputs except XOUT, IRQx, and D7–D0.

clock timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		ALTERNATE SYMBOLS	TEST CONDITIONS	MIN	MAX	UNIT
t_{d1}	Delay time, chip select (CS) high to clock (SCLK) high	t_{SHCH}	See Figure 18 and Figure 19	50		ns
t_{d2}	Input valid to clock (SCLK) high	t_{DVCH}		100		ns
t_{pd1}	Propagation delay time, clock (SCLK) high to input transition (SIO)	t_{CHDX}		100		ns
t_{pd2}	Propagation delay time, clock (SCLK) high to output valid (SIO)	t_{CHQV}			500	ns
t_{pd3}	Propagation delay time, clock (SCLK) low to chip select transition (CS)	t_{CLSL}			2	clock periods
t_{d3}	Delay time, chip select (CS) low to output Hi-Z (SIO)	t_{SLQZ}			100	ns
$t_{w(SCLKH)}$	Pulse duration, clock (SCLK) high to clock (SCLK) low (see Note 3)	t_{CHCL}		250		ns
$t_{w(SCLKL)}$	Pulse duration, clock (SCLK) low to clock (SCLK) high (see Note 3)	t_{CLCH}		250		ns
f_{clock}	Clock frequency (SCLK) (see Note 4)	F_{CLK}		0.5	0.68	MHz

NOTES: 3. The ST93C56 chip select, S, must be brought low for a minimum of 250 ns (t_{SLSH}) between consecutive instruction cycles according to the ST93C56 specification.
4. The SCLK signal is attained by internally frequency dividing the XIN signal by 32.

system timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		ALTERNATE SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{cR}	Cycle time, read ($t_{w7} + t_{d8} + t_{d9}$)	RC			87		ns
t_{cW}	Cycle time, write ($t_{w6} + t_{d5} + t_{d6}$)	WC			87		ns
t_{w1}†	Pulse duration, XIN high	t_{XH}	Figure 5	f = 16 MHz maximum	25		ns
t_{w2}†	Pulse duration, XIN low	t_{XL}	Figure 5	f = 16 MHz maximum	25		ns
t_{w6}	Pulse duration, write strobe ($\overline{IOW}$)	t_{WR}	Figure 6		75		ns
t_{w7}	Pulse duration, read strobe ($\overline{IOR}$)	t_{RD}	Figure 7		75		ns
t_{w8}	Pulse duration, master reset	t_{MR}			1		µs
t_{su3}	Setup time, data valid before $\overline{IOW}$↑	t_{DS}	Figure 6		15		ns
t_{h1}	Hold time, chip select (CS) valid after address (A0 – A2) becomes invalid	t_{CH}	Figure 6, Figure 7	From the first rising edge of XIN after address invalid		20	ns
t_{h2}	Hold time, data valid after $\overline{IOW}$↑	t_{DH}	Figure 6		5		ns
t_{d4}	Delay time, chip select ($\overline{CS}$) valid after address valid (A0 – A2)	t_{CSRW}	Figure 6, Figure 7	From the first rising edge of XIN after address valid		30	ns
t_{d5}	Delay time, address valid (A0 – A2) before $\overline{IOW}$↓	t_{AW}	Figure 6		7		ns
t_{d6}	Delay time, address valid (A0 – A2) before $\overline{IOR}$↓	t_{AR}	Figure 7		7		ns
t_{d7}	Delay time, chip select ($\overline{CS}$) valid to data valid (D7 – D0)	t_{CSVD}	Figure 7	C_L = 75 pF		30	ns
t_{d8}	Delay time, $\overline{IOR}$↑ to floating data (D7 – D0)	t_{HZ}	Figure 7	C_L = 75 pF		20	ns
t_{d9}	Delay time, EXINTR↑ or EXINTR↓ to IRQx↑ or IRQx↓		Figure 8			15	ns

† This only applies when $\overline{PNPBYPASS}$ is low.

oscillator cell maximum switching characteristics, V_{CC} = 4.75 V, T_J = 115°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	INTRINSIC DELAY (ns)	DELTA DELAY (ns/pF)	DELAY (ns)			
					C_L = 15 pF	C_L = 50 pF	C_L = 85 pF	C_L = 100 pF
t_{PLH}	XIN	XOUT	−0.25	0.300	4.26	14.76	25.26	29.77
t_{PHL}			−0.24	0.206	2.85	10.06	17.27	20.36
t_r	Output rise time, XOUT				5.83	21.15	36.47	43.04
t_f	Output fall time, XOUT				3.76	13.50	23.24	27.41

baud generator switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 75 pF (see Figure 5)

PARAMETER		ALTERNATE SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
t_{w3}†	Pulse duration, PNPS1 low	t_{LW}	f = 16 MHz, CLK ÷ 2	50		ns
t_{w4}†	Pulse duration, PNPS1 high	t_{HW}	f = 16 MHz, CLK ÷ 2	50		ns
t_{d1}†	Delay time, XIN↑ to PNPS1↑	t_{BLD}			45	ns
t_{d2}†	Delay time, XIN↑↓ to PNPS1↓	t_{BHD}			45	ns

† This only applies when $\overline{PNPBYPASS}$ is low.

receiver switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 5)

	PARAMETER	ALTERNATE SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d10}	Delay time, stop (SIN) to set INTRPT or read RBR to LSI interrupt (IRQx)	t_{SINT}	Figure 9, Figure 10, Figure 11			1	RCLK cycle
t_{d11}	Delay time, read RBR/LSR ($\overline{IOR}$) to reset INTRPT (IRQx)	t_{RINT}	Figure 9, Figure 10, Figure 11	C_L = 75 pF		70	ns

NOTE 5: In the FIFO mode, the read cycle (RC) = 425 ns (min) between reads of the receiver FIFO and the status registers (interrupt identification register or line status register).

transmitter switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 12)

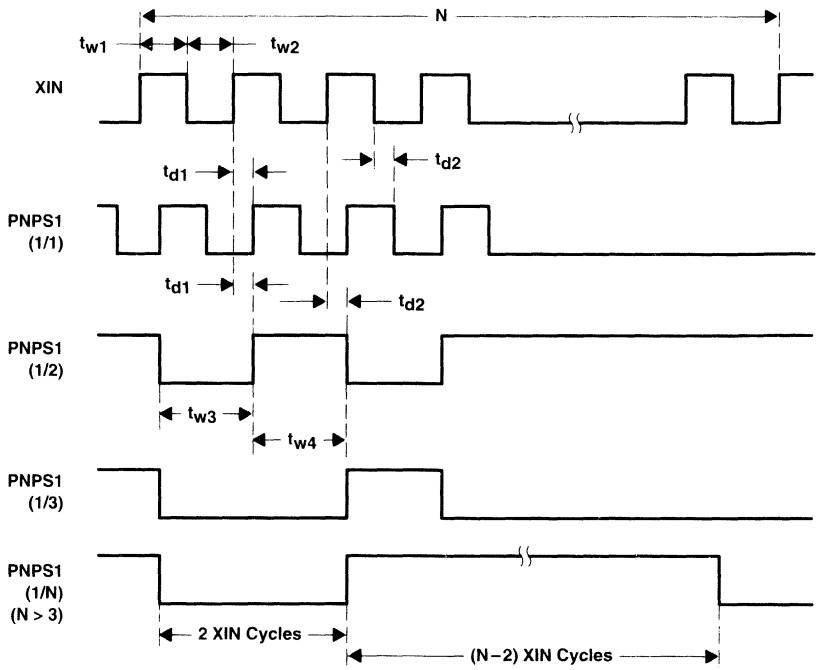
	PARAMETER	ALTERNATE SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
t_{d12}	Delay time, initial write (IRQx) to transmit start (SOUT)	t_{IRS}		8	26	baudout cycles
t_{d13}	Delay time, start (SOUT) to INTRPT (IRQx)	t_{STI}		8	10	baudout cycles
t_{d14}	Delay time, $\overline{IOW}$ (WR THR) to reset INTRPT (IRQx)	t_{HR}	C_L = 75 pF		50	ns
t_{d15}	Delay time, initial write ($\overline{IOW}$) to INTRPT (THRE†) (IRQx)	t_{SI}		16	34	baudout cycles
t_{d16}	Delay time, read IIR† ($\overline{IOR}$) to reset INTRPT (THRE†) (IRQx)	t_{IR}	C_L = 75 pF		35	ns

† THRE = transmitter holding register empty; IIR = interrupt identification register.

modem control switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 75 pF

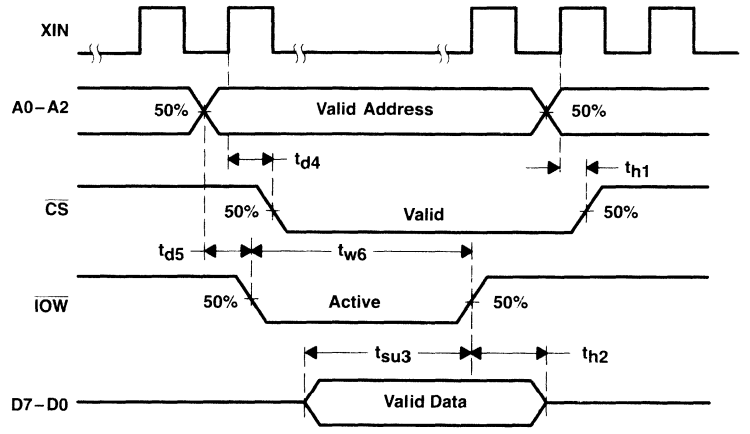
	PARAMETER	ALTERNATE SYMBOL	FIGURE	MIN	MAX	UNIT
t_{d17}	Delay time, WR MCR ($\overline{IOW}$) to output ($\overline{RTS}$, $\overline{DTS}$)	t_{MDO}	Figure 13		50	ns
t_{d18}	Delay time, modem interrupt (CTS, DSR, DCD/RI) to set INTRPT (IRQx)	t_{SIM}	Figure 13		35	ns
t_{d19}	Delay time, RD MSR ($\overline{IOR}$) to reset INTRPT (IRQx)	t_{RIM}	Figure 13		40	ns
t_{d20}	Delay time, $\overline{CTS}$ low to SOUT↓		Figure 14		24	baudout cycles
t_{d21}	Delay time, receiver threshold byte (SIN) to $\overline{RTS}$↑		Figure 15		3	baudout cycles
t_{d22}	Delay time, read of last byte in receiver FIFO ($\overline{IOR}$) to $\overline{RTS}$↓		Figure 15		3	baudout cycles
t_{d23}	Delay time, first data bit of 16th character (SIN) to $\overline{RTS}$↑		Figure 16		3	baudout cycles
t_{d24}	Delay time, RD RBR ($\overline{IOR}$) ↓ to $\overline{RTS}$↓		Figure 16		3	baudout cycles

PARAMETER MEASUREMENT INFORMATION



NOTE A: When $\overline{\text{PNPBYPASS}}$ = 0, the PNPS1 terminal is acting as the $\overline{\text{BAUDOUT}}$. The above timing assumes that the prescalar value is one.

Figure 5. Baud Generator Timing Waveforms



NOTE A: The above timing assumes that AEN = 0.

Figure 6. Write Cycle Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

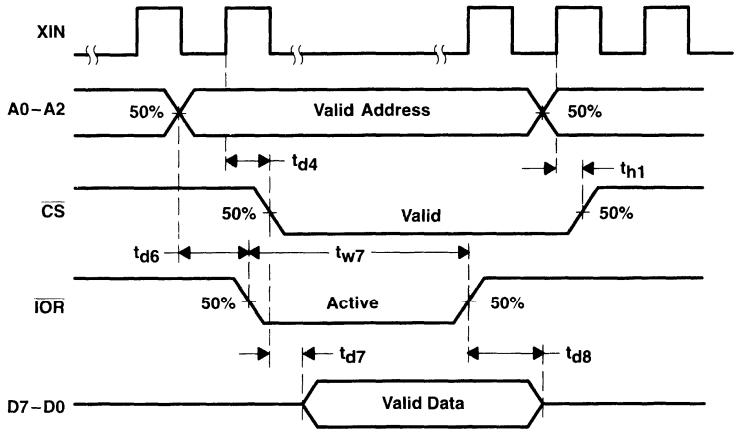


Figure 7. Read Cycle Timing Waveforms

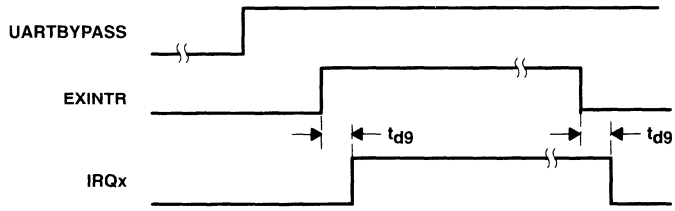
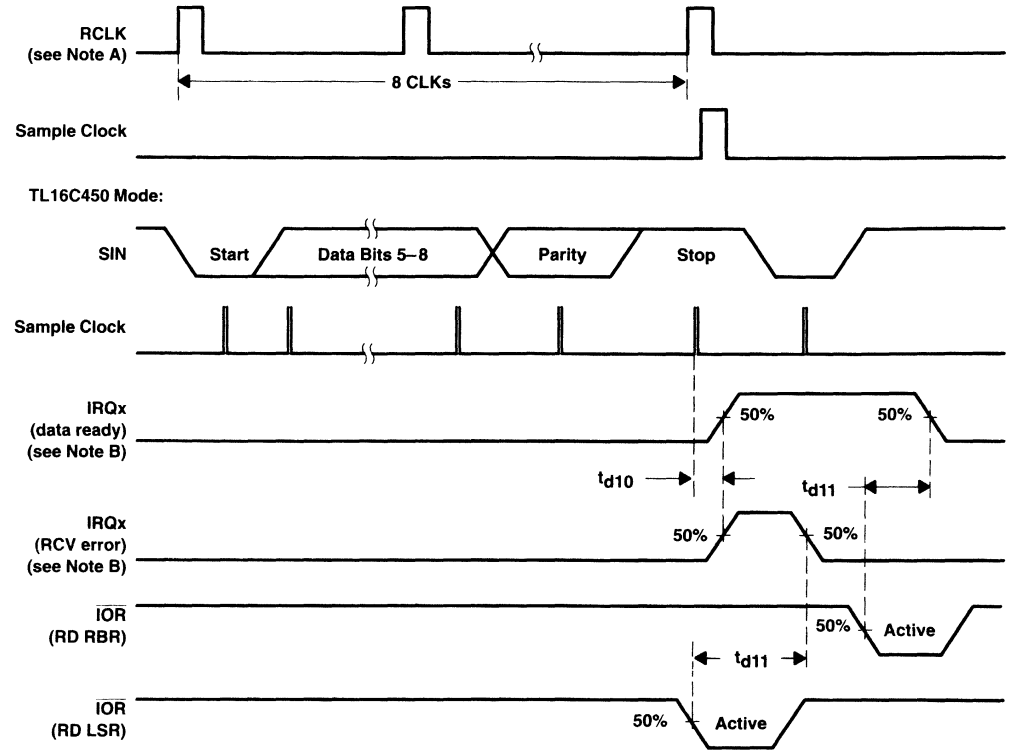


Figure 8. External Interrupt (EXINTR) Timing Waveforms

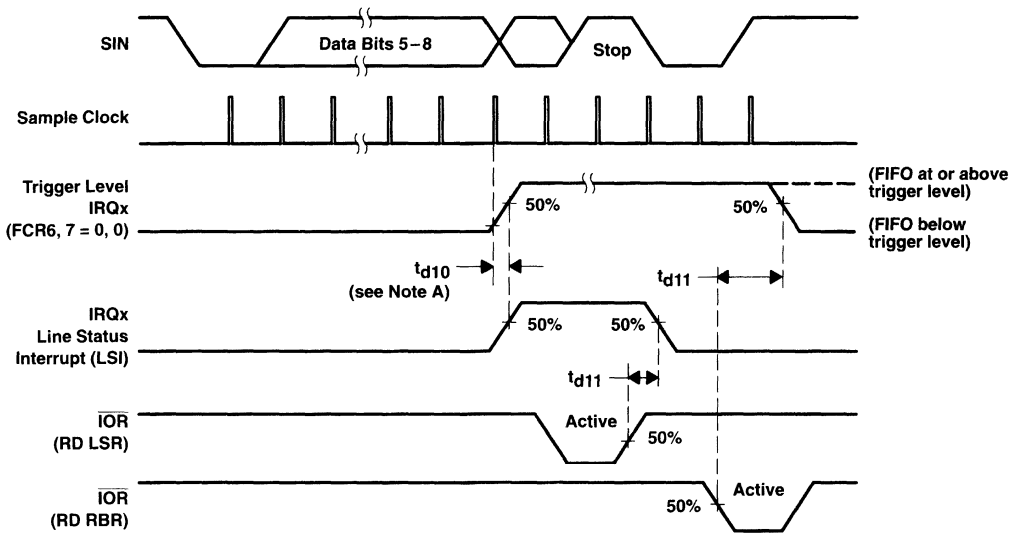
PARAMETER MEASUREMENT INFORMATION



NOTES: A. RCLK is the internal receiver clock.
B. X = 3–5, 7–12, 15

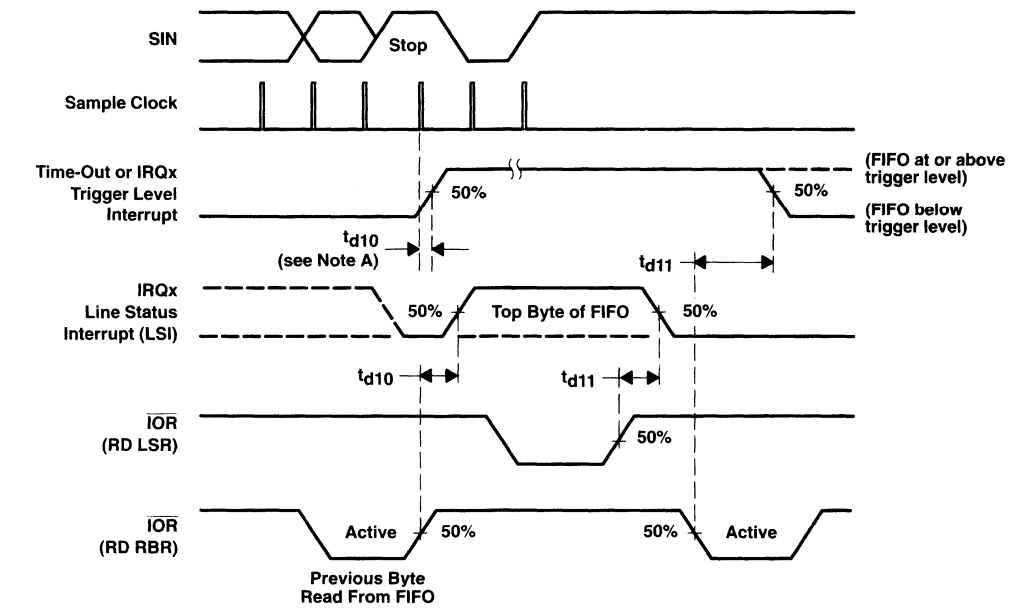
Figure 9. Receiver Timing Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: For a time-out interrupt, t_{d10} = 9 RCLKs.

Figure 10. Receive FIFO First Byte (Sets DR Bit) Waveforms



NOTE A: For a time-out interrupt, t_{d10} = 9 RCLKs.

Figure 11. Receive FIFO Bytes Other Than the First Byte (DR Internal Bit Already Set) Waveforms

PARAMETER MEASUREMENT INFORMATION

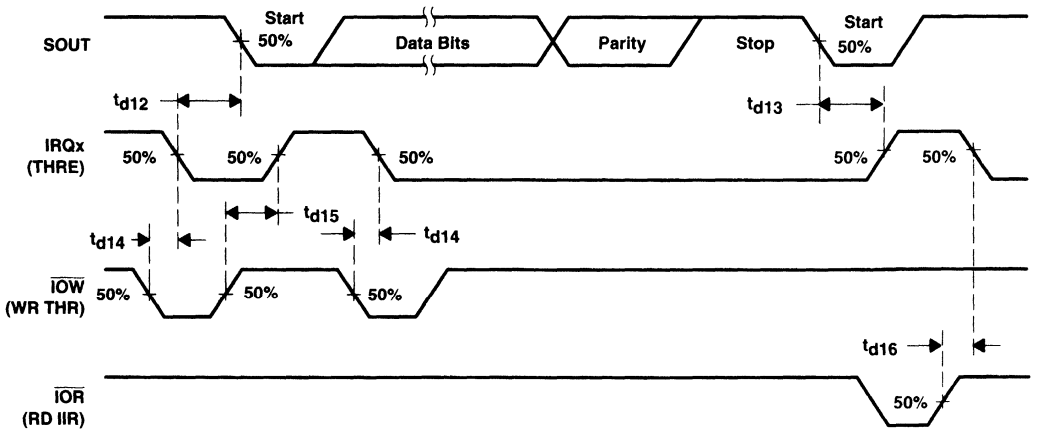


Figure 12. Transmitter Timing Waveforms

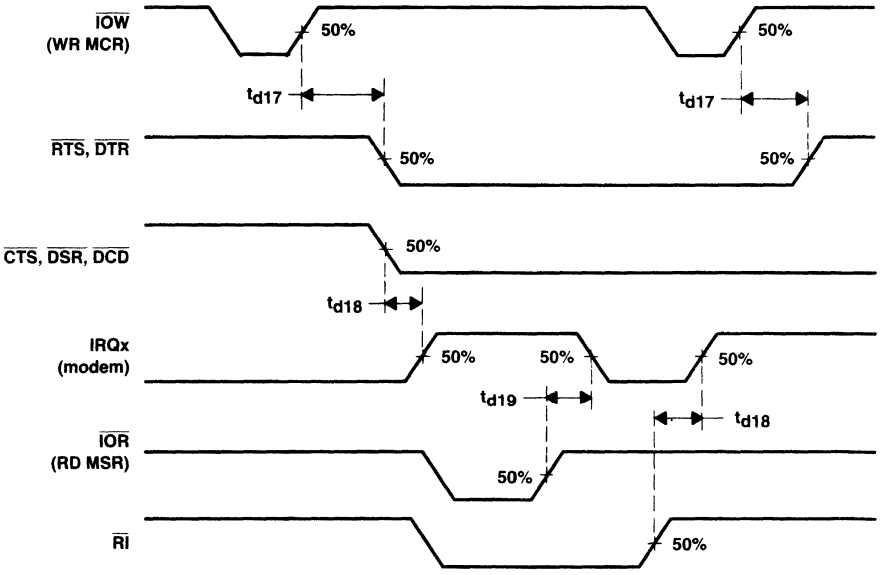


Figure 13. Modem Control Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

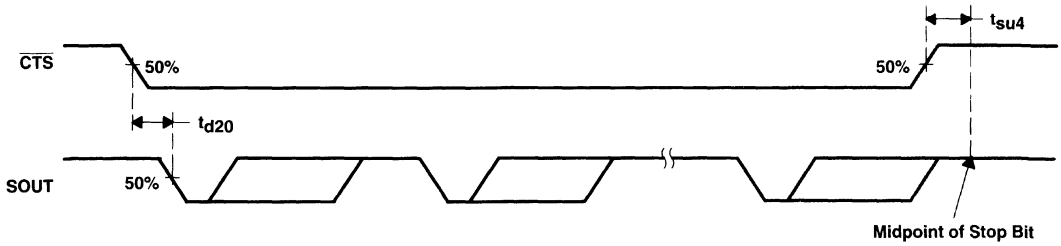


Figure 14. $\overline{CTS}$ and SOUT Autoflow Control Timing (Start and Stop) Waveforms

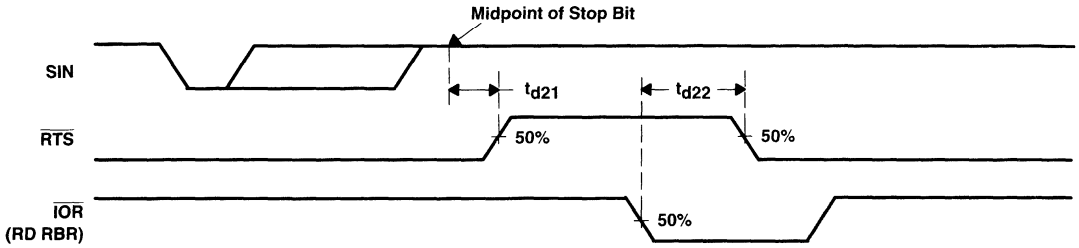


Figure 15. Auto-RTS Timing for Receiver Threshold of 1, 4, or 8 Waveforms

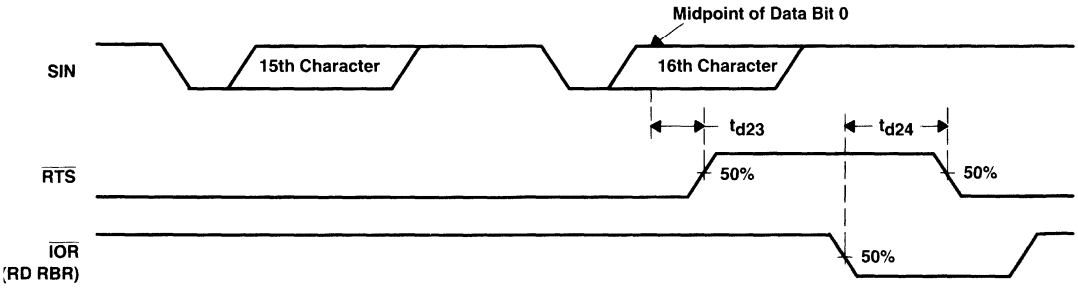


Figure 16. Auto-RTS Timing for Receiver Threshold of 14 Waveforms

PRINCIPLES OF OPERATION

The TL16PNP550A architecture (see functional block diagram) has been designed, so that it can be configured in various operational modes. These modes are described in the Table 1.

Table 1. TL16PNP550A Operational Modes†

MODE DESCRIPTION	UARTBYPASS TERMINAL	PNPBYPASS TERMINAL	ICONFIG<3:0> TERMINAL	ACONFIG <1:0> TERMINAL
PnP controller and logical device (ACE)	0	1	X	X
Stand-alone PnP Controller	1	1	X	X
ACE TL16C550C only	0	0	Active	Active
Manufacturer test mode‡	1	0	X	X

† X = irrelevant, 0 = low level, 1 = high level

‡ During manufacturer test mode, the oscillator clock is disabled. This mode is used by the manufacturer for test only.

Connecting the $\overline{\text{PNPBYPASS}}$ terminal to V_{CC} enables the PnP autoconfiguration sequence. When PnP is enabled, the ACONFIG<1:0> and ICONFIG<3:0> are irrelevant and should be tied to GND or V_{CC}.

In the stand-alone PnP controller mode, the controller responds to the autoconfiguration sequence and supports one logical device, one I/O address, one interrupt, and no DMA. The address decoder only decodes eight contiguous locations. During this mode, the UART is disabled and $\overline{\text{CS}}$ and EXINTR terminals become active. The UART input terminals should be tied to either V_{CC} or GND to avoid floating input terminals.

When PnP is disabled or bypassed, the $\overline{\text{PNPBYPASS}}$ terminal is tied to GND and the configuration in Table 2 applies.

Table 2. PnP Disabled or Bypassed Configuration

ACONFIG<1:0>	COM	I/O BASE ADDRESS
00	COM1	3F8–3FF
01	COM2	2F8–2FF
10	COM3	3E8–3EF
11	COM4	2E8–2EF

The decimal value X of ICONFIG<3:0> content enables the corresponding IRQx. For example, ICONFIG<3:0> = 0011 enables IRQ3 (Table 3).

Table 3. ICONFIG to IRQx

ICONFIG	IRQx	ICONFIG	IRQx
0000	N/A	1000	N/A
0001	N/A	1001	IRQ9
0010	N/A	1010	IRQ10
0011	IRQ3	1011	IRQ11
0100	IRQ4	1100	IRQ12
0101	IRQ5	1101	N/A
0110	IRQ6	1110	N/A
0111	IRQ7	1111	IRQ15

PRINCIPLES OF OPERATION

PnP card configuration sequence

The PnP logic is quiescent on power up and must be enabled by software. The following sequence configures the PnP card:

1. The initiation key places the PnP logic into configuration mode through a series of predefined writes to the ADDRESS port (see autoconfiguration ports section).
2. A serial identifier is accessed bit serially and isolates the Industry Standard Architecture (ISA) cards. Seventy-two READ_DATA port reads are required to isolate each card.
3. Once isolated, a card is assigned a handle [card select number (CSN)] that later selects the card. This assignment is accomplished by programming the CSN.
4. The PnP software then reads the resource data structure on each card. When all resource capabilities and demands are known, a process of resource arbitration is invoked to determine resource allocation for each card.
5. All PnP cards are then activated and removed from the configuration mode. This activation is accomplished by programming the ACTIVE register.

PnP autoconfiguration ports

Three 8-bit ports (see Table 4) are used by the software to access the configuration space on each PnP ISA card. These registers are used by the PnP software to issue commands, check status, access the resource data information, and configure the PnP hardware.

The ports have been chosen so as to avoid conflicts in the installed base of ISA functions, while at the same time minimizing the number of ports needed in the ISA I/O space.

Table 4. Autoconfiguration Ports

PORT NAME	LOCATION	TYPE
ADDRESS	0×0279 (printer status port)	Write only
WRITE_DATA	0×0A79 (printer status port + 0×0800)	Write only
READ_DATA	Relocatable in range 0×0203 to 0×03FF	Read only

The PnP registers are accessed by first writing the address of the desired register to the ADDRESS port, followed by a read of data from the READ_DATA port, or a write of data to the WRITE_DATA port. Once addressed, the desired register may be accessed using the WRITE_DATA or READ_DATA ports.

The ADDRESS port is also the destination of the initiation key writes.

The address of the READ_DATA port is set by programming the SET RD_DATA PORT register. If a card cannot be isolated for a given READ_DATA port address, the READ_DATA port address is in conflict. The READ_DATA port address must then be relocated and the isolation process begun again. The entire range between 0×0203 and 0×3FF is available; however, in practice it is expected that only a few address locations are necessary before the software determines that no PnP cards are present

PRINCIPLES OF OPERATION

PnP registers

PnP card standard registers are divided into three parts: card control, logical device control, and logical device configuration. There is exactly one of each card control register on each ISA card. Card control registers are used for global functions that control the entire card (see Table 5). Logical device control registers and logical device configuration registers are repeated for each logical device. Since the TL16PNP550A has one logical device (ACE) and it is intended only for I/O applications, not all the configuration registers are implemented.

Table 5. PnP Card Control Registers

ADDRESS PORT VALUE	REGISTER NAME VALUE	READ/WRITE CAPABILITY	POWER UP
0x00	SET RD_DATA PORT	Write only	00 00 00 00
	Writing to this location modifies the address port used for reading from the PnP ISA card. Writing to this register is only allowed when the card is in the isolation state. Bit<7:0> Become I/O port address bits [9:2].		
0x01	SERIAL ISOLATION	Read only	00 00 00 00
	A read to this register causes a card in the isolation state to compare one bit of the board ID.		
0x02	CONFIGURATION CONTROL	Write only	0 00
	This 3-bit register consists of three independent commands, which are activated by setting their corresponding register bits. These bits are automatically cleared by the hardware after the commands execute. Bit<2> Setting this bit causes the card to clear its CSN and RD DATA port. Bit<1> Setting this bit causes the card to enter the wait for key state, but the card CSN is preserved and the logical device (ACE) is unaffected. Bit<0> Setting this bit resets the logical device (ACE) configuration registers to their default state and the CSN is preserved.		
0x03	WAKE[CSN]	Write only	00 00 00 00
	A write to this register, if the write data [7:0] matches the card CSN, causes the card to go from the sleep state to either the isolation state, if the write data for this command is zero, or the configuration state if the write data is not zero. The pointer to the SERIAL IDENTIFIER is reset. This register is write only.		
0x04	RESOURCE DATA	Read only	00 00 00 00
	A read from this address reads the next byte of resource information from the EPROM. The STATUS register must be polled until its bit<0> is set, before this register may be read.		
0x05	STATUS	Read only	0
	Bit<0> A 1-bit register that when set, indicates it is okay to read the next data byte from the RESOURCE DATA register.		
0x06	CARD SELECT NUMBER	Read/write	00 00 00 00
	A write to this address sets a card CSN, which is uniquely assigned to this card after the serial identification process, so each card may be individually selected during a WAKE [CSN] command.		
0x07	LOGICAL DEVICE NUMBER	Read	00 00 00 00
	This register has a read-only value of 0x00, since the card has only 1 logical device.		

PRINCIPLES OF OPERATION

PnP logical device control registers

The following registers are repeated for each logical device. These registers control device functions, such as enabling the device onto the ISA bus (see Table 6).

Table 6. PnP Logical Device Control Registers

ADDRESS PORT VALUE	REGISTER NAME VALUE	READ/WRITE CAPABILITY	POWER UP
0×30	ACTIVE	Read/write	00 00 00 00
	This register controls whether the logical device is active on the bus. Bit<7:1> Reserved and must be cleared. Bit<0> When set, activates the logical device. An inactive device does not respond to nor drive any ISA bus signals. Before a logical device is activated, I/O range check must be disabled.		
0×31	I/O RANGE CHECK	Read/write	00 00 00 00
	This register performs a conflict check on the I/O port range programmed for use by the logical device. Bit<7:2> Reserved and must be cleared. Bit<1> When set, I/O range check is enabled. I/O range check is only valid, when the logical device is inactive. Bit<0> When set, the logical device (an ACE in this case) responds to I/O reads of the logical device (ACE) assigned I/O range with a 0×55 when I/O range check is in operation. When clear, the logical device responds with a 0×AA. This register is read/write.		

PnP logical device configuration registers

These registers program the device ISA bus resource use (see Table 7).

Table 7. PnP Logical Device Configuration Registers

ADDRESS PORT VALUE	REGISTER NAME VALUE	READ/WRITE CAPABILITY	POWER UP
0×60	I/O PORT BASE ADDRESS [15:8]	Read/write	00
	This register indicates the selected I/O upper limit address bits [15:8] for I/O descriptor 0. When the device is activated, if there is an address match to register 0×61 and an address match to this register, a chip select is generated. Bit<7:2> Bits 15–10 are not supported, since the logical device uses 10-bit address decoding. Bit<1:0> Indicates address bits 9 and 8.		
0×61	I/O PORT BASE ADDRESS [7:0]	Read/write	00 00 00 00
	This register indicates the selected I/O lower limit address bits [7:0] for I/O descriptor 0. When the device is activated, if there is an address match to register 0×60 and an address match to this register, a chip select is generated. Bit<2:0> Are not supported since the logical device has eight registers. Bit<7:3> Indicates address bits 7–3.		
0×70	INTERRUPT REQUEST LEVEL SELECT	Read/write	00 00
	This register indicates the selected interrupt level. Bit<3:0> Select the interrupt level. This device uses 10 interrupts from IRQ2 to IRQ7 and IRQ9 to IRQ12.		
0×71	INTERRUPT REQUEST TYPE	Read	00 00 00 11
	This register indicates which type of interrupt is used for the selected interrupt level. Bit<7:2> Are reserved. Bit<1> Is set to indicate active high. Bit<0> Is set to indicate level sensitive.		
0×74	DMA CHANNEL SELECT 0	Read only	00 00 01 00
	This register has a value of 4 to indicate that DMA is not supported.		
0×75	DMA CHANNEL SELECT 1	Read only	00 00 01 00
	This register has a value of 4 to indicate that DMA is not supported.		

PRINCIPLES OF OPERATION

PnP terminal states

Terminals PNPS1 and PNPS0 reflect the states of PnP logic when $\overline{\text{PNPBYPASS}}$ is set (see Table 8).

Table 8. PNPx Terminal States

PNPS1	PNPS0	PnP STATE
0	0	WAIT FOR KEY
0	1	SLEEP
1	0	ISOLATION
1	1	CONFIGURATION

If the device leaves the wait-for-key state, it means the device is in configuration mode.

Please note, when $\overline{\text{PNPBYPASS}}$ = 0, $\overline{\text{BAUDOUT}}$ is monitored using PNPS1 and $\overline{\text{RXRDY}}$ is monitored using PNPS0.

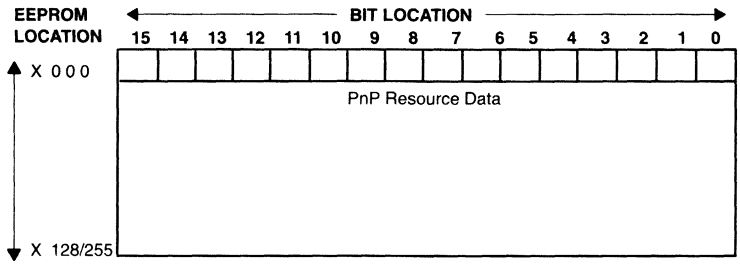
EEPROM

The TL16PNP550A has been designed to interface with the ST93C56/66 EEPROM (SGS-Thomson) or equivalent. The EEPROM provides the clock prescalar divisor and PnP resource data.

memory organization

The EEPROM should be organized as 128/255 words times 16 bits, so its ORG terminal should be connected to V_{CC} or left unconnected. The EEPROM memory organization is shown in Table 9.

Table 9. EEPROM Memory Organization



PRINCIPLES OF OPERATION

clock prescalar

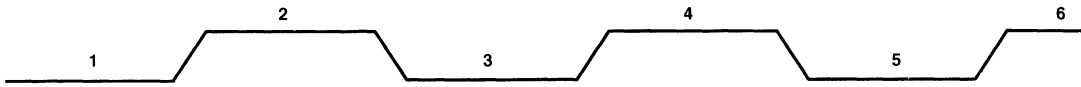
The TL16PNP550A includes a clock prescalar block. The block takes the 22-MHz input clock and divides it by a divisor read from the EEPROM at address zero. After reset, the device reads the EEPROM content at address zero. The 2 most significant data bits of the word (2 bytes) define the divisor value as show in Table 10.

Table 10. Default Deviser Value

EEPROM LOCATION 000 (BITS 15 AND 14)	DIVISOR VALUE
00	12
01	6
10	3
11	1 (default)

The device monitors the EEPROM to check whether the divisor value has been updated or not. Read the EEPROM interface section for more details in this mode. Note the EEPROM address location zero is reserved for the divisor value.

$\overline{\text{EEPROM}}$ signal description (see Figure 17)

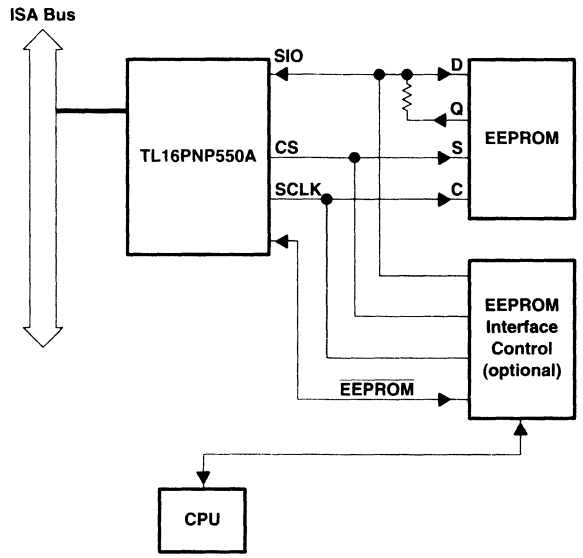


1. During and after reset, the TL16PNP550A gains access to EEPROM interface by asserting $\overline{\text{EEPROM}}$ (low). The device reads the prescalar divisor value from address zero. After it receives the WAKE command, the device starts receiving PnP resource data from address location 00x01H.
2. After the device is configured and leaves the configuration mode (the device is activated and it is in the wait for key state), the TL16PNP550A releases the EEPROM interface by releasing signals $\overline{\text{EEPROM}}$, SCLK, SIO, and CS.
3. The on-board controller is accessing the EEPROM.
4. The TL16PNP550A assumes the prescalar divisor value has been updated.
5. The TL16PNP550A accesses the EEPROM by asserting $\overline{\text{EEPROM}}$ signal. It reads location 00 and updates the prescalar divisor.
6. The TL16PNP550A releases the $\overline{\text{EEPROM}}$ signal and SCLK, CS and SIO signals.

If the device enters the configuration mode again (leaves the wait for key state), it gains access directly to the EEPROM after the $\overline{\text{EEPROM}}$ signal is released.

If the $\overline{\text{EEPROM}}$ is driven by an on-board controller and the TL16PNP550A enters the configuration mode, it is highly recommended that the controller release the $\overline{\text{EEPROM}}$ signal to allow the TL16PNP550A to gain control of $\overline{\text{EEPROM}}$. It is possible to deactivate and reconfigure the TL16PNP550A when it enters the configuration mode. PNPS0 and PNPS1 terminals inform the controller when the TL16PNP550A enters the configuration mode.

PRINCIPLES OF OPERATION



NOTE A: It is recommended that a 2-kΩ resistor be connected between D and Q terminals.

Figure 17. TL16PNP550A and EEPROM Interface

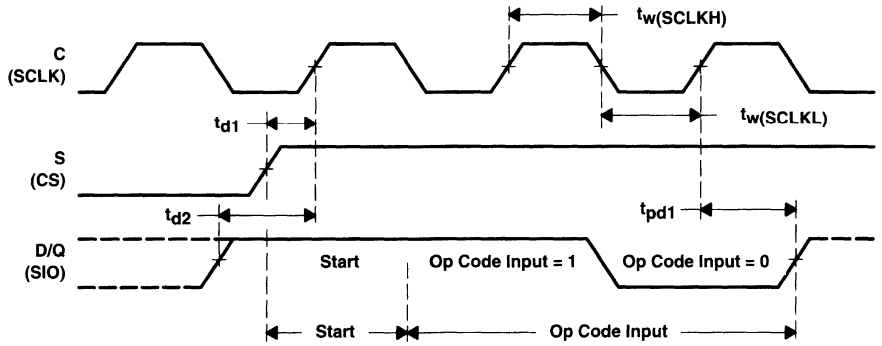
EEPROM READ

The TL16PNP550A only supports read transactions. The READ op code instruction (10) must be sent into the EEPROM. The op code is then followed by an address for the 16-bit word, which is 8-bits long . The READ op code with accompanying address directs the EEPROM to output serial data on the EEPROM data terminal D/Q which is connected to the TL16PNP550A bidirectional serial data bus (SIO). Specifically, when a READ op code and address are received, the instruction and address are decoded and the addressed EEPROM data is transferred into an output shift register in the EEPROM. Each read transaction consists of a start bit, 2-bit op code (10), 8-bit address, and 16-bit data. The TL16PNP550A does not accommodate the EEPROM auto-address next word feature.

PRINCIPLES OF OPERATION

READ op code transfer (see Figure 18)

Initially, the EEPROM chip select signal, S, which is connected to the TL16PNP550A EEPROM chip select (CS), is raised. The EEPROM data, D/Q then samples the TL16PNP550A (SIO) line on the following rising edges of the TL16PNP550A clock (SCLK), until a 1 is sampled and decoded by the EEPROM as a start bit. The TL16PNP550A (SCLK) signal is connected to the EEPROM clock, C. The READ op code (10) is then sampled on the next two rising edges of SCLK. TL16PNP550A sources the op code at the falling edges of SCLK.

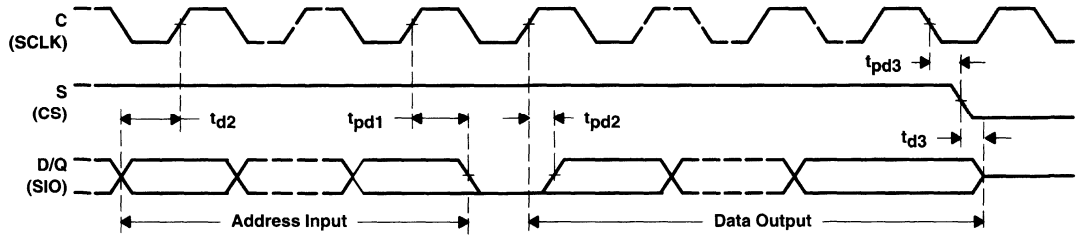


NOTE A: The corresponding TL16PNP550A terminal names are provided in parentheses. D/Q indicates that D and Q terminals in the EEPROMs are tied together with a 2-kΩ resistor.

Figure 18. READ Op Code Transfer Waveforms

READ address and data transfer (see Figure 19)

After receiving the READ op code, the EEPROM samples the READ address on the next eight rising edges of (SCLK). The device sources the address at the falling edge of SCLK. The EEPROM then sends out a dummy 0 bit on the D/Q line, which is followed by the 16-bit data word with the MSB first. Output data changes are triggered by the rising edges of SCLK. The data is also read by the TL16PNP550A on the rising edges of SCLK.



NOTE A: The corresponding terminal names are provided in parentheses. D/Q indicates that D and Q terminals in the EEPROMs are tied together with a 2-kΩ resistor.

Figure 19. READ Address and Data Transfer Waveforms

PRINCIPLES OF OPERATION

Table 11. ACE Register Selection

DLAB†	A2	A1	A0	REGISTER
0	L	L	L	Receiver buffer (read), transmitter holding register (write)
0	L	L	H	Interrupt enable
X	L	H	L	Interrupt identification (read only)
X	L	H	L	FIFO control (write)
X	L	H	H	Line control
X	H	L	L	Modem control
X	H	L	H	Line status
X	H	H	L	Modem status
X	H	H	H	Scratch
1	L	L	L	Divisor latch (LSB)
1	L	L	H	Divisor latch (MSB)

† The divisor latch access bit (DLAB) is the most significant bit of the line control register. The DLAB signal is controlled by writing to this bit location (see Table 13).

Table 12. ACE Reset Functions

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	Master Reset	All bits cleared (0–3 forced and 4–7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is set, bits 1–3, 6, 7 are cleared, and bits 4–5 are permanently cleared
FIFO Control Register	Master Reset	All bits cleared
Line Control Register	Master Reset	All bits cleared
Modem Control Register	Master Reset	All bits cleared (6–7 permanent)
Line Status Register	Master Reset	Bits 5 and 6 are set, all other bits are cleared
Modem Status Register	Master Reset	Bits 0–3 are cleared, bits 4–7 are input signals
SOUT	Master Reset	High
INTRPT (receiver error flag)	Read LSR/MR	Low
INTRPT (received data available)	Read RBR/MR	Low
INTRPT (transmitter holding register empty)	Read IR/Write THR/MR	Low
INTRPT (modem status changes)	Read MSR/MR	Low
$\overline{RTS}$	Master Reset	High
$\overline{DTR}$	Master Reset	High
Scratch Register	Master Reset	No effect
Divisor Latch (LSB and MSB) Registers	Master Reset	No effect
Receiver Buffer Registers	Master Reset	No effect
Transmitter Holding Register	Master Reset	No effect
Receiver FIFO	MR/FCR1–FCR0/ ΔFCR0	All bits cleared
XMIT FIFO	MR/FCR2–FCR0/ ΔFCR0	All bits cleared

PRINCIPLES OF OPERATION

accessible registers

The system programmer, using the CPU, has access to and control over any of the ACE registers. These registers control ACE operations, receive data, and transmit data. Descriptions of these registers follow in Table 13.

Table 13. Summary of Accessible Registers

Bit No.	REGISTER ADDRESS											
	0 DLAB = 0	0 DLAB = 0	1 DLAB = 0	2	2	3	4	5	6	7	0 DLAB = 1	1 DLAB = 1
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident. Register (Read Only)	FIFO Control Register (Write Only)	Line Control Register	Modem Control Register	Line Status Register	Modem Status Register	Scratch Register	Divisor Latch (LSB)	Latch (MSB)
	RBR	THR	IER	IIR	FCR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Data Bit 0†	Data Bit 0	Enable Received Data Available Interrupt (ERBI)	0 If Interrupt Pending	FIFO Enable	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (ΔCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit 1	Receiver FIFO Reset	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (ΔDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit 2	Transmitter FIFO Reset	Number of Stop Bits (STB)	OUT1	Parity Error (PE)	Trailing Edge of Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable Modem Status Interrupt (EDSSI)	Interrupt ID Bit 3‡	Reserved	Parity Enable (PEN)	OUT2 UART Interrupt Enable§	Framing Error (FE)	Delta Data Carrier Detect (ΔDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity	Flow Control Enable (AUTO)	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	FIFOs Enabled‡	Receiver Trigger (LSB)	Break Control	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	FIFOs Enabled‡	Receiver Trigger (MSB)	Divisor Latch Access Bit (DLAB)	0	Error in Receiver FIFO (see Note 6)	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

† Bit 0 is the least significant bit. It is the first bit serially transmitted or received.
‡ These bits are always 0 in the TL16C450 mode.
§ By setting this bit high in PNPBYPASS mode, the selected interrupt (IRQx) is enabled, otherwise, IRQx output is in the high-impedance state.

PRINCIPLES OF OPERATION

FIFO control register (FCR)

The FCR is a write-only register at the same location as the IIR, which is a read-only register. The FCR enables the FIFOs, clears the FIFOs, sets the receiver FIFO trigger level, and selects the type of DMA signaling.

- Bit 0: FCR0, when set, enables the transmit and receive FIFOs. This bit must be set when other FCR bits are written to or they are not programmed. Changing this bit clears the FIFOs.
- Bit 1: FCR1, when set, clears all bytes in the receiver FIFO and resets its counter. The shift register is not cleared. The logic 1 that is written to this bit position is self clearing.
- Bit 2: FCR2, when set, clears all bytes in the transmit FIFO and resets its counter. The shift register is not cleared. The logic 1 that is written to this bit position is self clearing.
- Bits 3, 4, and 5: FCR3, FCR4, and FCR5 are reserved for future use.
- Bits 6 and 7: FCR6 and FCR7 set the trigger level for the receiver FIFO interrupt (see Table 14).

Table 14. Receiver FIFO Trigger Level

BIT 7	BIT 6	RECEIVER FIFO TRIGGER LEVEL (BYTES)
0	0	01
0	1	04
1	0	08
1	1	14

FIFO interrupt mode operation

When the receiver FIFO and receiver interrupts are enabled (FCR0 = 1, IER0 = 1, IER2 = 1), receiver interrupt occur as follows:

1. When the receiver FIFO reaches its programmed trigger level, the received data available interrupt is issued to the microprocessor and IIR (3–0) are set to the value 6 (to indicate received data available). The received data available interrupt is cleared and IIR (3–0) are set (no interrupt) when the FIFO drops below its programmed trigger level.
2. The data ready bit (LSR0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is cleared when the FIFO is empty.
3. The receiver line status interrupt (IIR = 0110h) has higher priority than the received data available (IIR = 0100h) interrupt.

PRINCIPLES OF OPERATION

FIFO interrupt mode operation (continued)

When the receiver FIFO and receiver interrupts are enabled, receiver FIFO time-out interrupt occurs as follows:

1. FIFO time-out interrupt occurs when the following conditions exist:
   a. At least one character is in the FIFO.
   b. The most recent serial character received is longer than the four previous continuous character times (if two stop bits are programmed, the second one is included in this time delay).
   c. The most recent microprocessor read of the FIFO is longer than four previous continuous character times. This causes a maximum character received to interrupt an issued delay of 160 ms at 300 baud with a 12-bit character.
2. Character times are calculated by using the internal receiver clock (RCLK) input for a clock signal (makes the delay proportional to the baud rate). The RCLK frequency equals the clock frequency generated by the prescalar block divided by the user-defined internal UART baud rate generator divisor.
3. When a time-out interrupt has occurred, it is cleared and the timer is reset when the microprocessor reads one character from the receiver FIFO.
4. When a time-out interrupt has not occurred, the time-out timer is reset after a new character is received or after the microprocessor reads the receiver FIFO.

When the transmit FIFO and transmitter interrupts are enabled (FCR0 = 1, IER1 = 1), transmit interrupts occur as follows:

1. The transmitter holding register empty interrupt [IIR (3–0) = 2] occurs when the transmit FIFO is empty. It is cleared [IIR (3–0) = 1] as soon as the THR is written to (1 to 16 characters may be written to the transmit FIFO while servicing this interrupt) or the IIR is read.
2. The transmitter FIFO empty indicator [LSR5 (THRE) = 1] is delayed one character time minus the last stop bit time when there have not been at least two bytes in the transmitter FIFO at the same time since the last time that THRE = 1. The first transmitter interrupt after changing FCR0 is immediate when it is enabled.

Character time-out and receiver FIFO trigger level interrupts have the same priority as the current received data available interrupt; transmit FIFO empty has the same priority as the current transmitter holding register empty interrupt.

FIFO polled mode operation

With FCR0 = 1 (transmitter and receiver FIFOs enabled), clearing IER0, IER1, IER2, IER3, or all four puts the ACE in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately, either one or both can be in the polled mode of operation.

In this mode, the user program checks receiver and transmitter status using the LSR.

- LSR0 is set as long as there is one byte in the receiver FIFO.
- LSR1 – LSR4 specify which error(s) have occurred. Character error status is handled the same way as when in the interrupt mode; the IIR is not affected since IER2 = 0.
- LSR5 indicates when the transmit FIFO is empty.
- LSR6 indicates that both the transmit FIFO and shift registers are empty.
- LSR7 indicates whether there are any errors in the receiver FIFO.

There is no trigger level reached or time-out condition indicated in the FIFO polled mode. However, the receiver and transmit FIFOs are still fully capable of holding characters.

PRINCIPLES OF OPERATION

interrupt enable register (IER)

The IER enables each of the five types of interrupts (refer to Table 15) and the internal INTRPT output signal in response to an interrupt generation. The IER can also disable the interrupt system by clearing bits 0 through 3. The contents of this register are summarized in Table 13 and are described in the following bulleted list.

- Bit 0: This bit, when set, enables the received data available interrupt.
- Bit 1: This bit, when set, enables the transmitter holding register empty interrupt.
- Bit 2: This bit, when set, enables the receiver line status interrupt.
- Bit 3: This bit, when set, enables the modem status interrupt.
- Bits 4 – 7: These bits in the IER are not used and are always cleared.

interrupt identification register (IIR)

The ACE has an on-chip interrupt generation and prioritization capability that permits a flexible interface with most popular microprocessors.

The ACE provides four prioritized levels of interrupts:

- Priority 1 – Receiver line status (highest priority)
- Priority 2 – Receiver data ready or receiver character time out
- Priority 3 – Transmitter holding register empty
- Priority 4 – Modem status (lowest priority)

When an interrupt is generated, the IIR indicates that an interrupt is pending and the type of that interrupt in its three least significant bits (bits 0, 1, and 2). The contents of this register are summarized in Table 13 and described in Table 15. Details on each bit are as follows:

- Bit 0: This bit can be used either in a hardwire prioritized, or polled interrupt system. When this bit is cleared, an interrupt is pending. When bit 0 is set, no interrupt is pending.
- Bits 1 and 2: These two bits identify the highest priority interrupt pending, as indicated in Table 15.
- Bit 3: This bit is always cleared in the TL16C450 mode. In FIFO mode, this bit is set with bit 2 to indicate that a time-out interrupt is pending.
- Bits 4 and 5: These two bits are not used and are always cleared.
- Bits 6 and 7: These two bits are always cleared in the TL16C450 mode. They are set when bit 0 of the FIFO control register is set.

PRINCIPLES OF OPERATION

interrupt identification register (IIR) (continued)

Table 15. Interrupt Control Functions

INTERRUPT IDENTIFICATION REGISTER				PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET METHOD
BIT 3	BIT 2	BIT 1	BIT 0				
0	0	0	1	None	None	None	None
0	1	1	0	1	Receiver line status	Overrun error, parity error, framing error or break interrupt	Reading the line status register
0	1	0	0	2	Received data available	Receiver data available in the TL16C450 mode or trigger level reached in the FIFO mode	Reading the receiver buffer register
1	1	0	0	2	Character time-out indication	No characters have been removed from or input to the receiver FIFO during the last four character times, and there is at least one character in it during this time	Reading the receiver buffer register
0	0	1	0	3	Transmitter holding register empty	Transmitter holding register empty	Reading the interrupt identification register (if source of interrupt) or writing into the transmitter holding register
0	0	0	0	4	Modem status	Clear to send, data set ready, ring indicator, or data carrier detect	Reading the modem status register

line control register (LCR)

The system programmer controls the format of the asynchronous data communication exchange through the LCR. In addition, the programmer is able to retrieve, inspect, and modify the contents of the LCR; this eliminates the need for separate storage of the line characteristics in system memory. The contents of this register are summarized in Table 13 and described in the following bulleted list.

- Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. These bits are encoded as shown in Table 16.

Table 16. Serial Character Word Length

BIT 1	BIT 0	WORD LENGTH
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

- Bit 2: This bit specifies either one, one and one-half, or two stop bits in each transmitted character. When bit 2 is cleared, one stop bit is generated in the data. When bit 2 is set, the number of stop bits generated is dependent on the word length selected with bits 0 and 1. The receiver clocks only the first stop bit, regardless of the number of stop bits selected. The number of stop bits generated, in relation to word length and bit 2, is shown in Table 17.

PRINCIPLES OF OPERATION

line control register (LCR) (continued)

Table 17. Number of Stop Bits Generated

BIT 2	WORD LENGTH SELECTED BY BITS 1 AND 2	NUMBER OF STOP BITS GENERATED
0	Any word length	1
1	5 bits	1 1/2
1	6 bits	2
1	7 bits	2
1	8 bits	2

- Bit 3: This bit is the parity enable bit. When bit 3 is set, a parity bit is generated in transmitted data between the last data word bit and the first stop bit. In received data, when bit 3 is set, parity is checked. When bit 3 is cleared, no parity is generated or checked.
- Bit 4: Bit 4 is the even parity select bit. When parity is enabled (bit 3 is set) and bit 4 is set, even parity (an even number of logic 1s in the data and parity bits) is selected. When parity is enabled and bit 4 is cleared, odd parity (an odd number of logic 1s) is selected.
- Bit 5: This bit is the stick parity bit. When bits 3, 4, and 5 are set, the parity bit is transmitted and checked as cleared. When bits 3 and 5 are set and bit 4 is cleared, the parity bit is transmitted and checked as set. When bit 5 is cleared, stick parity is disabled.
- Bit 6: This bit is the break control bit. Bit 6 is set to force a break condition; i.e., a condition where the serial output (SOUT) is forced to the spacing (low) state. When bit 6 is cleared, the break condition is disabled and has no affect on the transmitter logic; it only affects the serial output.
- Bit 7: This bit is the divisor latch access bit (DLAB). Bit 7 must be set to access the divisor latches of the baud generator during a read or write. Bit 7 must be cleared during a read or write to access the receiver buffer, the THR, or the IER.

line status register (LSR)†

The LSR provides information to the CPU concerning the status of data transfers. The contents of this register are described in the following bulleted list and summarized in Table 13.

- Bit 0: Bit 0 is the data ready (DR) indicator for the receiver. This bit is set whenever a complete incoming character has been received and transferred into the RBR or the FIFO. Bit 0 is cleared by reading all of the data in the RBR or the FIFO.
- Bit 1‡: Bit 1 is the overrun error (OE) indicator. When this bit is set, it indicates that before the character in the RBR is read, it is overwritten by the next character transferred into the register. The OE indicator is cleared every time the CPU reads the contents of the LSR. If the FIFO mode data continues to fill the FIFO beyond the trigger level, an overrun error occurs only after the FIFO is full and the next character has been completely received in the shift register. An OE is indicated to the CPU as soon as it happens. The character in the shift register is overwritten, but it is not transferred to the FIFO.
- Bit 2‡: Bit 2 is the parity error (PE) indicator. When this bit is set, it indicates that the parity of the received data character does not match the parity selected in the LCR (bit 4). The PE bit is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO.

† The line status register is intended for read operations only; writing to this register is not recommended outside a factory testing environment.
‡ Bits 1 through 4 are the error conditions that produce a receiver line status interrupt.

PRINCIPLES OF OPERATION

line status register (LSR) (continued)†

- Bit 3‡: Bit 3 is the framing error (FE) indicator. When this bit is set, it indicates that the received character did not have a valid (set) stop bit. The FE bit is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. The ACE tries to resynchronize after a framing error. To accomplish this, it is assumed that the framing error is due to the next start bit. The ACE samples this start bit twice and then accepts the input data.
- Bit 4‡: Bit 4 is the break interrupt (BI) indicator. When this bit is set, it indicates that the received data input was held in the low state for longer than a full-word transmission time. A full-word transmission time is defined as the total time of the start, data, parity, and stop bits. The BI bit is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. When a break occurs, only one 0 character is loaded into the FIFO. The next character transfer is enabled after SIN goes to the marking state and receives the next valid start bit.
- Bit 5: Bit 5 is the transmitter holding register empty (THRE) indicator. This bit is set when the THR is empty, indicating that the ACE is ready to accept a new character. If the THRE interrupt is enabled when the THRE bit is set, an interrupt is generated. THRE is set when the contents of the THR are transferred to the TSR. This bit is cleared concurrent with the loading of the THR by the CPU. In the FIFO mode, this bit is set when the transmit FIFO is empty; it is cleared when at least one byte is written to the transmit FIFO.
- Bit 6: Bit 6 is the transmitter empty (TEMT) indicator. This bit is set when the THR and the TSR are both empty. When either the THR or the TSR contains a data character, the TEMT bit is cleared. In the FIFO mode, this bit is set when the transmitter FIFO and shift register are both empty.
- Bit 7: In the TL16C550C mode, this bit is always cleared. In the TL16C450 mode, this bit is always cleared. In the FIFO mode, LSR7 is set when there is at least one parity error, framing error, or break error in the FIFO. It is cleared when the microprocessor reads the LSR and there are no subsequent errors in the FIFO.

modem control register (MCR)

The MCR is an 8-bit register that controls an interface with a modem, data set, or peripheral device that is emulating a modem. The contents of this register are summarized in Table 13 and are described in the following bulleted list.

- Bit 0: Bit 0 (DTR) controls the data terminal ready ($\overline{\text{DTR}}$) output. Setting this bit forces the $\overline{\text{DTR}}$ output to its low state. When bit 0 is cleared, $\overline{\text{DTR}}$ goes high.
- Bit 1: Bit 1 (RTS) controls the request-to-send ($\overline{\text{RTS}}$) output in a manner identical to bit 0's control over the $\overline{\text{DTR}}$ output.
- Bit 2: Bit 2 (OUT1) controls the internal signal $\overline{\text{OUT1}}$.
- Bit 3: Bit 3 (OUT2) when set in PNPBYPASS mode, the selected interrupt line IRQx is enabled; otherwise, IRQx is 3-state.

† The line status register is intended for read operations only; writing to this register is not recommended outside a factory testing environment.

PRINCIPLES OF OPERATION

modem control register (MCR) (continued)

- Bit 4: Bit 4 provides a local loop back feature for diagnostic testing of the ACE. When this bit is set, the following occurs:
  - The transmitter serial output (SOUT) is asserted high.
  - The receiver serial input (SIN) is disconnected.
  - The output of the TSR is looped back into the receiver shift register input.
  - The four modem control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$) are disconnected.
  - The four modem control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT1}$, and $\overline{OUT2}$) are internally connected to the four modem control inputs.
  - The four modem control outputs are forced to their inactive (high) states.

NOTE

$\overline{OUT1}$ is a user-designated output signal for TL16C550. It is an internal signal and not used in the TL16PNP550A.

In the diagnostic mode, data that is transmitted is immediately received. This allows the processor to verify the transmit and receive data paths to the ACE. The receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational, but the modem control interrupt sources are now the lower four bits of the MCR instead of the four modem control inputs. All interrupts are still controlled by the IER.

The ACE flow can be configured by programming bits 1 and 5 of the MCR. Table 18 shows that autoflow control can be enabled by setting MCR bit 5, autoflow enable (AFE) and also setting MCR bit 1, RTS. autoflow incorporates both auto-RTS and auto-CTS. If only auto-CTS is desired, set bit 5 and clear bit 1. If neither auto-RTS nor auto-CTS is desired, clear bit 5.

Table 18. ACE Flow Configuration

MCR BIT 5 (AFE)	MCR BIT 1 (RTS)	ACE FLOW CONFIGURATION
1	1	Auto-RTS and auto-CTS enabled (autoflow control enabled)
1	0	Auto-CTS only enabled
0	X	Auto-RTS and auto-CTS disabled

modem status register (MSR)

The MSR is an 8-bit register that provides information about the current state of the control lines from the modem, data set, or peripheral device to the CPU. Additionally, four bits of this register provide change information; when a control input from the modem changes state, the appropriate bit is set. All four bits are cleared when the CPU reads the MSR. The contents of this register are summarized in Table 13 and are described in the following bulleted list.

- Bit 0: Bit 0 is the change in the clear-to-send (ΔCTS) indicator. This bit indicates that the $\overline{CTS}$ input has changed state since the last time it was read by the CPU . When this bit is set (autoflow control is not enabled and the modem status interrupt is enabled), a modem status interrupt is generated. When autoflow control is enabled, no interrupt is generated.
- Bit 1: Bit 1 is the change in the data set ready (ΔDSR) indicator. This bit indicates that the $\overline{DSR}$ input has changed state since the last time it was read by the CPU. When this bit is set and the modem status interrupt is enabled, a modem status interrupt is generated.

PRINCIPLES OF OPERATION

modem status register (MSR) (continued)

- Bit 2: Bit 2 is the trailing edge of ring indicator (TERI) detector. This bit indicates that the $\overline{RI}$ input to the chip has changed from a low to a high state. When this bit is set and the modem status interrupt is enabled, a modem status interrupt is generated.
- Bit 3: Bit 3 is the change in data carrier detect (ΔDCD) indicator. This bit indicates that the $\overline{DCD}$ input to the chip has changed state since the last time it was read by the CPU. When this bit is set and the modem status interrupt is enabled, a modem status interrupt is generated.
- Bit 4: Bit 4 is the complement of the clear-to-send ($\overline{CTS}$) input. When bit 4 (loop) of the MCR is set, this bit is equivalent to the MCR bit 1 (RTS).
- Bit 5: Bit 5 is the complement of the data set ready ($\overline{DSR}$) input. When bit 4 (loop) of the MCR is set, this bit is equivalent to the MCR bit 1 (DTR).
- Bit 6; Bit 6 is the complement of the ring indicator ($\overline{RI}$) input. When bit 4 (loop) of the MCR is set, this bit is equivalent to the MCR bit 2 (OUT1).
- Bit 7: Bit 7 is the complement of the data carrier detect ($\overline{DCD}$) input. When bit 4 (loop) of the MCR is set, this bit is equivalent to the MCR bit 3 (OUT2).

programmable baud generator

The ACE contains a programmable baud generator that receives a clock input generated by the prescalar block in the range between 1.833 and 22 MHz and divides it by a divisor in the range between 1 and ($2^{16}-1$). The output frequency of the baud generator is sixteen times (16×) the baud rate. The formula for the divisor is:

divisor # = clock frequency generated by the prescalar block ÷ (desired baud rate × 16)

Two 8-bit registers, called divisor latches, store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization of the ACE in order to ensure correct operation of the baud generator. When either of the divisor latches is loaded, a 16-bit baud counter is also loaded to prevent long counts on initial load.

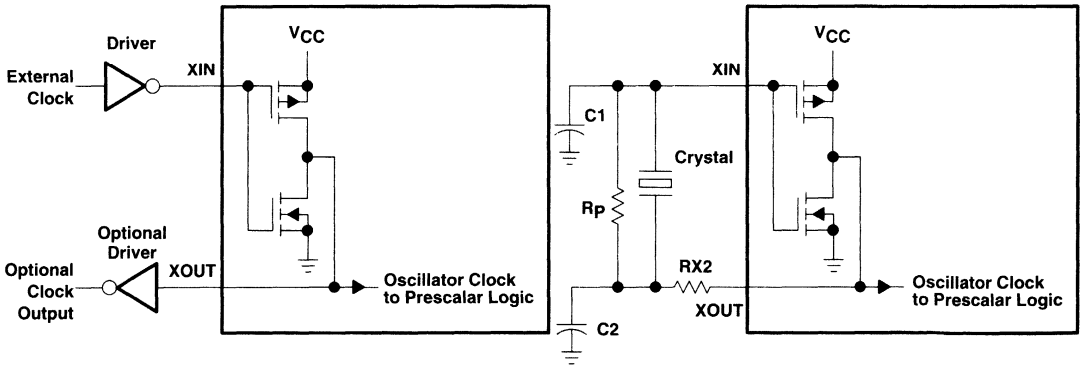
Table 19 illustrates the use of the baud generator with a crystal frequency of 22 MHz and a prescalar divisor of 12. Refer to Figure 20 for an example of a typical clock circuit.

PRINCIPLES OF OPERATION

programmable baud generator (continued)

Table 19. Baud Rates Using a 22-MHz Crystal and a Prescalar Divisor of 12

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16× CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
1800	64	
2000	58	0.69
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19200	6	
38400	3	
56000	2	2.86



TYPICAL CRYSTAL OSCILLATOR NETWORK

CRYSTAL	Rp	RX2	C1	C2
22 MHz	1 MΩ	1.5 kΩ	10–30 pF	40–60 pF

Figure 20. Typical Clock Circuits

PRINCIPLES OF OPERATION

receiver buffer register (RBR)

The ACE receiver section consists of a receiver shift register (RSR) and a RBR. The RBR is actually a 16-byte FIFO. Timing is supplied by the 16× receiver clock (RCLK). Receiver section control is a function of the ACE line control register.

The ACE RSR receives serial data from the serial input (SIN) terminal. The RSR then deserializes the data and moves it into the RBR FIFO. In the TL16C450 mode, when a character is placed in the RBR and the received data available interrupt is enabled, an interrupt is generated. This interrupt is cleared when the data is read out of the RBR. In the FIFO mode, the interrupts are generated based on the control setup in the FIFO control register.

scratch register

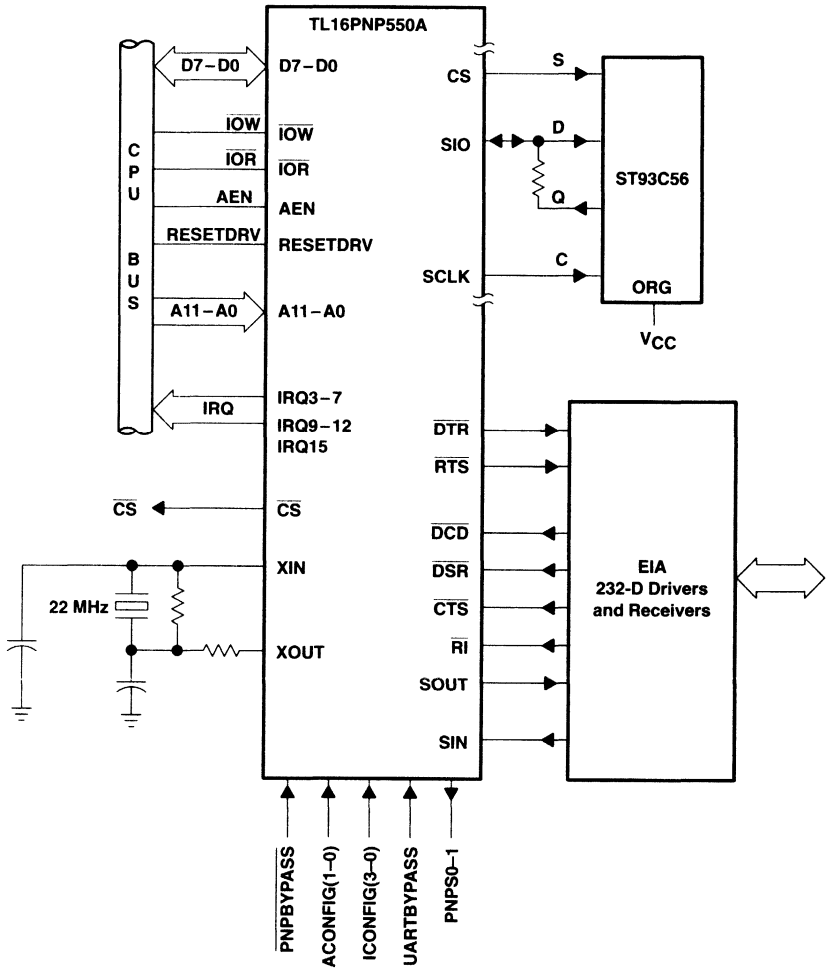
The scratch register is an 8-bit register that is intended for the programmer's use as a scratchpad in the sense that it temporarily holds the programmer's data without affecting any other ACE operation.

transmitter holding register (THR)

The ACE transmitter section consists of a THR and a transmitter shift register (TSR). The THR is actually a 16-byte FIFO. Timing is supplied by the baud out ($\overline{\text{BAUDOUT}}$) clock signal. Transmitter section control is a function of the ACE line control register.

The ACE THR receives data off the internal data bus and when the TSR is idle, moves the data into the TSR. The TSR serializes the data and outputs it at the serial output (SOUT). In the TL16C450 mode, if the THR is empty and the transmitter holding register empty (THRE) interrupt is enabled, an interrupt is generated. This interrupt is cleared when a character is loaded into the register. In the FIFO mode, the interrupts are generated based on the control setup in the FIFO control register.

APPLICATION INFORMATION



NOTES: A. No data or IRQ buffer is needed.
B. Check ST93C56 application note: When D and Q terminals are shorted it is recommended that a 2-kΩ resistor be inserted between terminals D and Q.

Figure 21. Basic TL16PNP550A Configuration

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3 UART Product Previews

- **Software Compatible with TL16C550C UART**
- **IEEE 1284 Bidirectional Parallel Data port**
  - **Compatible with Standard Centronics Parallel Interface**
  - **Support for Parallel Protocols ECP and EPP**
  - **Data Path 16-Byte FIFO Buffer**
  - **Direct Memory Access (DMA) Transfer**
  - **Decompression of Run Length Encoded Data in ECP Reverse Mode**
  - **Direct Connection to Printer, No External Transceiver is Needed**
- **Serial Ports Have IrDA Inputs and Outputs**
  - **1200 bit/s to 115.2 kbit/s Data Rate**
- **16-Byte FIFOs Reduce CPU Interrupts**
- **12 mA Drive Current for All 1284 Control Pins and Parallel Port Data Pins**
- **Programmable Auto-$\overline{\text{RTS}}$ and Auto-$\overline{\text{CTS}}$**
- **Capable of Running With All Existing TL16C452 Software**
- **After Reset, All Registers Are Identical to the TL16C450 Register Set**
- **Up to 16-MHz Clock Rate for Up to 1-Mbaud Operation**
- **Programmable Baud Rate Generator Allows Division of Any Input Reference Clock by 1 to ($2^{16}-1$) and Generates an Internal 16× Clock**
- **Independent Receiver Clock Input**
- **Independent Control of Transmit, Receive, Line Status, and Data Set Interrupts on Each Channel**
- **Modem Control Functions ($\overline{\text{CTS}}$, $\overline{\text{RTS}}$, $\overline{\text{DSR}}$, $\overline{\text{DTR}}$, $\overline{\text{RI}}$, and $\overline{\text{DCD}}$)**
- **Available in 80-Pin PQFP**

PRODUCT PREVIEW

description

Functionally equivalent to the TL16C450 on power up (character or TL16C450 mode), the TL16PIR552 can also be placed in FIFO mode. This relieves the CPU of excessive software overhead by buffering received and transmitted characters. The receiver and transmitter FIFOs store up to 16 bytes including three additional bits of error status per byte for the receiver FIFO. In the FIFO mode, there is a selectable autoflow control feature that can significantly reduce software overload and increase system efficiency by automatically controlling serial data flow using $\overline{\text{RTS}}$ output and $\overline{\text{CTS}}$ input signals.

The TL16PIR552 is similar to the TL16C552A dual-channel UART. The device serves two serial I/O ports simultaneously in a microcomputer or microprocessor-based system. Each channel performs serial-to-parallel conversion on data characters received from peripheral devices or modems and parallel-to-serial conversion on data characters transmitted by the CPU. The complete status of each channel of the dual-channel UART can be read at any time during functional operation by the CPU. The information obtained includes the type and condition of the transfer operation being performed and the error condition.

The serial ports also have a dedicated Infrared Data Association (IrDA) serial data input (IRSIN0/1) and the serial data outputs multiplex between RS-232 type serial output or IrDA serial data output. This is selected through an internal register bit and uses the same SOUT0 and SOUT1 output pins. The same UART circuit is used for the data path for the IrDA or the RS232 case.

In addition to the dual communication capabilities, the TL16PIR552 provides the user with an IEEE 1284 host-side-compatible bidirectional parallel data port. The parallel port operates in compatible mode, nibble mode, byte mode, extended capability port (ECP) mode (with RLE data decompression), or enhanced parallel port (EPP) mode. The default mode of operation is compatible with the Centronics-type printer port interface. The parallel port and the two serial ports provide IBM PC/AT™-compatible computers with a single device to serve a 3-system port. The TL16PIR552 has one IBM PC/XT™ compatible parallel port which includes a PS/2™-type bidirectional parallel port (SSP), that is supported by EPP and ECP protocols.

IBM PC/AT, IBM PC/XT, and PS/2 are a trademarks of International Business Machines Corporation.

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description (continued)

The TL16PIR552 includes a programmable baud rate generator capable of dividing a reference clock by divisors from 1 to (2^{16}–1) and producing a 16× reference clock for the internal transmitter logic. Provisions are also included to use this 16× clock for the receiver logic. The UART accommodates a 1-Mbaud serial rate (16-MHz input clock) so that a bit time is 1 µs and a typical character time consisting of a start bit, 8 data bits, and a stop bit is 10 µs.

PRODUCT PREVIEW

TL16PNP200
STAND ALONE PLUG-AND-PLAY (PnP) CONTROLLER

SLLS229 – NOVEMBER 1995

- **PnP Card Autoconfiguration Sequence Compliant**
- **Satisfies All Requirements for Qualifying for the Windows 95™ Logo**
- **Supports up to Five Logical Devices**
- **24-Bit Memory Address Decoding, and 16-Bit I/O Address Decoding With Programmable (1, 2, 4, 8, 16, 32, 64) I/O Block Size**
- **Configurable $\overline{\text{OEN}}$ Signals That Can Be Used to Enable Logical Device Transceivers**
- **Device-Interrupt Mapping to any of the 11 Interrupt Request (IRQ) Signals on the ISA Bus**
- **DMA Support For Two Logical Devices with Configurable DMA Channel Connection**
- **Simple 3-Terminal Interface to Serial EEPROM 2K/4K ST93C56/66 or Equivalent for Resource Data Storage**
- **Default Configuration Loading and Activation Upon Power-up for Non-PnP Systems**
- **Direct Connection to ISA/AT Bus Without Need for Buffers**
- **5-V Power Supply Operation**
- **Available in 80-pin PQFP**

description

The TL16PNP200 is an ISA plug-and-play (PnP) controller that provides autoconfiguration capability to ISA cards according to the ISA PnP 1.0a specification. This device interfaces to a serial EEPROM where card resource requirements and power-up defaults are stored. On power up, the controller loads the default configuration from the EEPROM making it ready for operation (non-PnP systems) or to be configured by the PnP configuration process (PnP-capable systems). During the configuration mode, the PnP autoconfiguration process reads the card resource requirements, configures the card by writing to the TL16PNP200 configuration registers, activates the device, and removes it from the configuration mode. Thereafter, the TL16PNP200 routes all ISA transactions between the card and the ISA bus.

The TL16PNP200 operates in one of two modes. In mode 0, the device supports two logical devices with memory, I/O, interrupt, and DMA resources for each device. In mode 1, the device supports five logical devices with I/O and interrupt resources for all logical devices and direct memory access (DMA) resources for two of the five logical devices; there is no memory support in mode 1. The TL16PNP200 provides interface signals to allow on-board logic access to the serial EEPROM.

PRODUCT PREVIEW

Windows 95 is a trademark of Microsoft Corporation.

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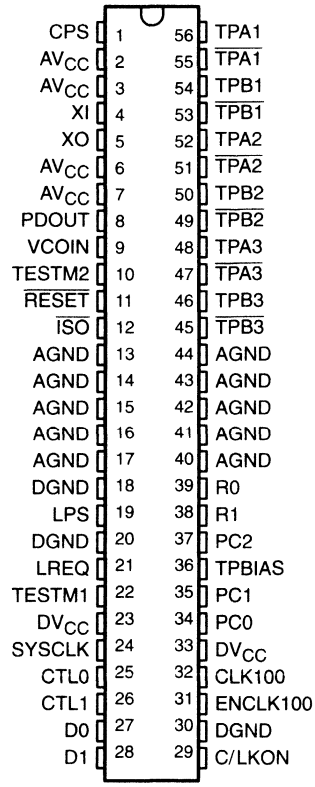
4 IEEE-1394

SLLS167A – MARCH 1994 – REVISED MARCH 1996

- **Supports Provisions of IEEE 1394-1995 for High-Performance Serial Bus**
- **Fully Interoperable With FireWire™ Implementation of IEEE 1394-1995**
- **Provides Three Fully Compliant Cable Ports at 100 Mbits Per Second (Mbits/s)**
- **Cable Ports Monitor Line Conditions for Active Connection to Remote Node**
- **Inactive Ports Disabled to Save Power**
- **Logic Performs System Initialization and Arbitration Functions**
- **Encode and Decode Functions Included for Data Strobe Bit Level Encoding**
- **Incoming Data Resynchronized to Local Clock**
- **Interface to Link Layer Controller Supports Optional Electrical Isolation**
- **Data Interface to Link Layer Controller Provided Through Two Parallel Lines at 50 Mbits/s**
- **25-MHz Crystal Oscillator and PLL Provide Transmit, Receive Data, and Link Layer Controller Clocks at 50 MHz**
- **Selectable Oscillator Input for External 100-MHz Reference Signal**
- **Node Power Class Information Signaling for System Power Management**
- **Cable Power Presence Monitoring**
- **Cable Bias and Driver Termination Voltage Supply**
- **Single 5-V Supply Operation**
- **Separate Multiple Package Terminals Provided for Analog and Digital Supplies and Grounds**
- **High-Performance 56-Pin SSOP (DL) Package**

DL PACKAGE
(TOP VIEW)



description

The TSB11C01 provides the analog transceiver functions needed to implement a 3-port node in a cable-based IEEE 1394-1995 network. Each cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions needed for determining connection status, for initialization and arbitration, and for packet reception and transmission. The TSB11C01 is designed to interface with a link layer controller, such as the TSB12C01A.

FireWire is a trademark of Apple Computer, Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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description (continued)

The TSB11C01 requires either an external 24.576-MHz crystal or an external 98.304-MHz reference oscillator input. When using the crystal oscillator option, an internal phase-locked loop (PLL) generates the required 98.304-MHz reference signal. Selecting the external oscillator option turns off both the crystal oscillator and the PLL. The 98.304-MHz reference signal is internally divided to provide the 49.152-MHz ±100 ppm clock signals that control transmission of the outbound encoded strobe and data information. The 49.152-MHz clock signal is also supplied to the associated link layer controller for synchronization of the two chips and is used for resynchronization of the received data.

Data bits to be transmitted are received from the link layer controller on two parallel paths and are latched internally in the TSB11C01 in synchronization with the 49.152-MHz system clock. These bits are combined serially, encoded, and transmitted at 98.304 Mbits/s as the outbound data strobe information stream. During transmit, the encoded data information is transmitted differentially on the TPB cable pair(s) and the encoded strobe information is transmitted differentially on the TPA cable pair(s).

During packet reception, the TPA and TPB transmitters of the receiving cable port are disabled and the receivers for that port are enabled. The encoded data information is received on the TPA cable pair, and the encoded strobe information is received on the TPB cable pair. The received data strobe information is decoded to recover the receive clock signal and the serial data bits. The serial data bits are split into two parallel streams, resynchronized to the local system clock and sent to the associated link layer controller. The received data is also transmitted (repeated) out of the other active cable ports.

Both the TPA and TPB cable interfaces incorporate differential comparators to monitor the line states during initialization and arbitration. The outputs of these comparators are used by the internal logic to determine the arbitration status. In addition, the TPB channel monitors the incoming cable common-mode voltage for the presence of the remotely supplied twisted-pair bias voltage. The presence or absence of this bias voltage is used as an indication of cable connection status.

The TSB11C01 provides a 1.86-V nominal bias voltage for driver load termination. This bias voltage, when seen through a cable by a remote receiver, senses the presence of an active connection. The value of this bias voltage has been chosen to allow interoperability between transceivers operating from either 5-V nominal supplies or 3-V nominal supplies. This bias voltage source should be stabilized by using an external filter capacitor of approximately 1 μF.

The line drivers in the TSB11C01 operate in the high-impedance current mode and are designed to work with external 112-Ω line matching resistor networks. One network is provided at each end of each twisted-pair cable. Each network is composed of a pair of series-connected 56-Ω resistors. The midpoint of the pair of resistors that is directly connected to the twisted-pair A-package terminals is connected to the TPBIAS voltage terminal. The midpoint of the pair of resistors that is directly connected to the twisted-pair B-package terminals is coupled to ground through a parallel RC network with recommended values of 5 kΩ and 250 pF. The values of the external resistors are designed to meet the IEEE 1394-1995 specifications when connected in parallel with the internal receiver circuits.

The driver output current, along with other internal operating currents, is set by an external resistor. This resistor is connected between R1 and R0 and has a value of 6.36 kΩ ±0.5%.

Two terminals set up various test conditions used in manufacturing. Terminals TESTM1 and TESTM2 should be connected to V_{CC} for normal operation.

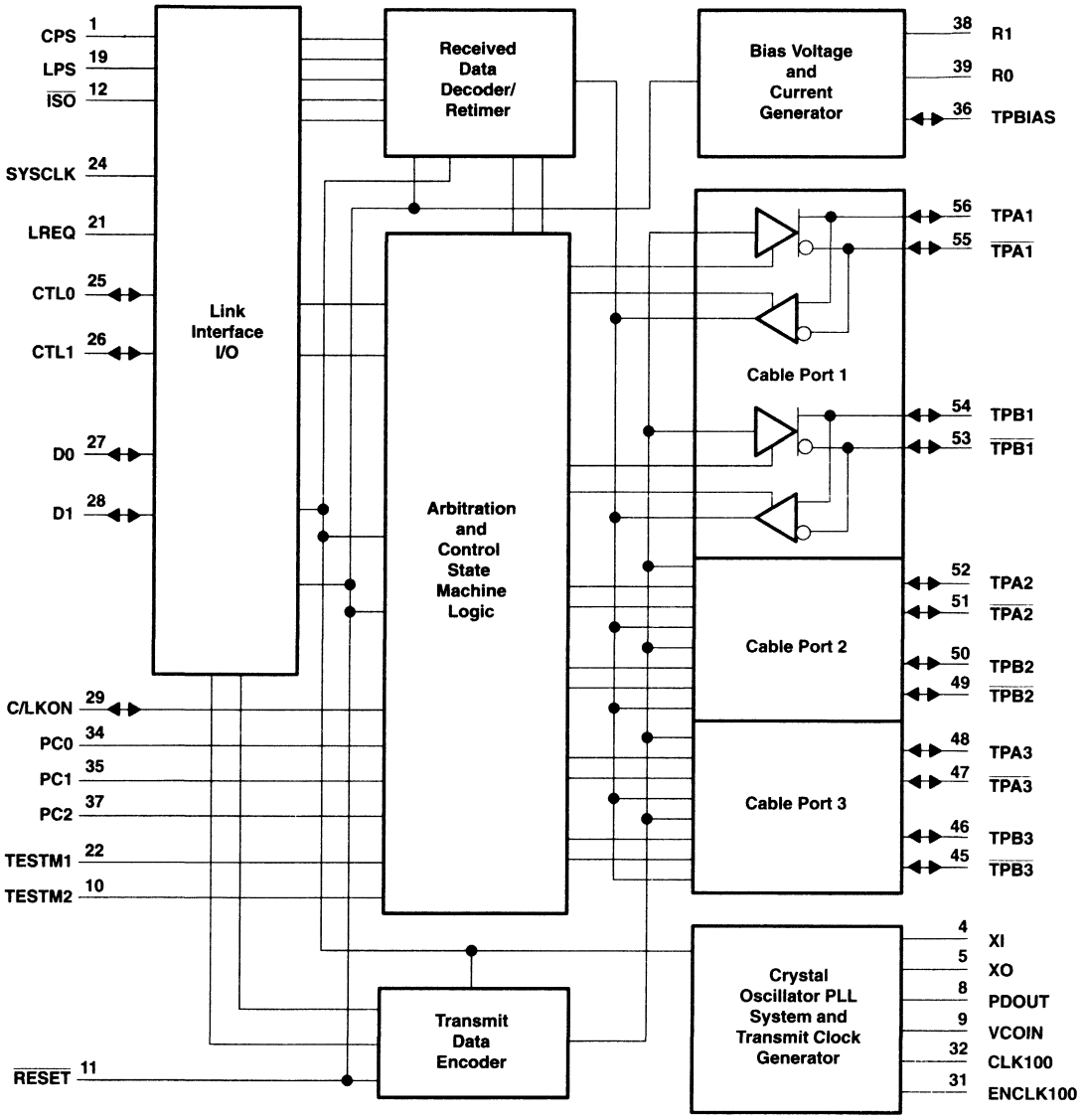
Four terminals are used as inputs to set four configuration status bits in the self identification packet. These terminals are hardwired high or low as a function of the equipment design. PC[0:2] are three terminals that indicate either the need for power from the cable or the ability to supply power to the cable. The fourth terminal, C/LKON, indicates if a node is a contender for configuration manager. C/LKON can also output a 6.114-MHz ±100 ppm signal, indicating reception of a link-on packet. See Table 4–27 of the IEEE 1394-1995 standard for additional details.

description (continued)

The TSB11C01 supports an optional isolation barrier between itself and its link layer controller. When $\overline{ISO}$ is tied high, the link interface outputs behave normally; when tied low, an internal differentiating logic is enabled and the outputs become short pulses that can be coupled through a capacitor or transformer.

The TSB11C01 is characterized for operation from 0°C to 70°C.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	13–17, 40–44		Analog circuit ground
AV_{CC}	2, 3, 6, 7		Analog circuit supply voltage
CLK100	32	I	Optional external clock input
C/LKON	29	I/O	Configuration manager contender status input or link-on output
CPS	1	I	Cable power status
CTL[0:1]	25, 26	I/O	Link interface bidirectional control signals
D[0:1]	27, 28	I/O	Link interface bidirectional data signals
DGND	18, 20, 30		Digital circuit ground
DV_{CC}	23, 33		Digital circuit supply voltage
ENCLK100	31	I	Disable crystal oscillator and PLL, enable CLK100 input
$\overline{ISO}$	12	I	Physical (phy) link interface isolation status
LPS	19	I	Link power status
LREQ	21	I	Link request from controller
PDOUT	8	O	Output from PLL phase detector, input to external filter
PC[0:2]	34, 35, 37	I	Power class bits 0 through 2 inputs
R[0:1]	38, 39		External bias current-setting resistor
$\overline{RESET}$	11	I	Reset
TESTM1, TESTM2	22, 10	I	Test mode control, normally tied high
SYSCLK	24	O	49.152-MHz clock to link controller
TPA1, TPA2, TPA3	56, 52, 48	I/O	Port n cable pair A, positive signal
$\overline{TPA1}$, $\overline{TPA2}$, $\overline{TPA3}$	55, 51, 47	I/O	Port n cable pair A, negative signal
TPB1, TPB2, TPB3	54, 50, 46	I/O	Port n cable pair B, positive signal
$\overline{TPB1}$, $\overline{TPB2}$, $\overline{TPB3}$	53, 49, 45	I/O	Port n cable pair B, negative signal
TPBIAS†	36	O	Cable termination voltage source
VCOIN	9	I	Input to VCO, output from external filter
XI, XO	4, 5	I/O	External crystal for oscillator

† The output voltage at TPBIAS (terminal 36) is approximately 50 mV below the target design value. This can cause the measured TPBIAS output voltage to fall outside the specified limits when under the worst case conditions of minimum supply voltage and maximum load current. To adjust the output voltage at TPBIAS to the specified limit, connect an external resistor of approximately 785 Ω between TPBIAS (terminal 36) and AV_{CC} (terminals 2, 3, 6, or 7). The nominal TPBIAS output voltage will be adjusted to the target design value on a future revision of this device.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 6 V
Input voltage range, V_I ..... 0.5 V to V_{CC} + 0.5 V
Output voltage range at any output, V_O ..... 0.5 V to V_{CC} + 0.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DL	2500 mW	20 mW/°C	1600 mW

‡ This is the inverse of the traditional junction-to-case thermal resistance ($R_{\theta JA}$) and uses a board mounted device rated at 50°C/W.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	CMOS inputs	0.7 V_{CC}			V
Low-level input voltage, V_{IL}	CMOS inputs			0.2 V_{CC}	V
Differential input voltage, V_{ID}	Cable inputs	142		260	mV
Common-mode input voltage, V_{IC}	Cable inputs	1.12		2.54	V
High-level output current, I_{OH}	SYSCLK			−16	mA
	CTL0, CTL1, D0, D1			−12	
Low-level output current, I_{OL}	SYSCLK			16	mA
	CTL0, CTL1, D0, D1			12	
Output current, I_O	TPBIAS	−5		2.5	mA

electrical characteristics over recommended ranges of operating conditions (unless otherwise noted)

driver

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OD}	Differential output voltage	R_L = 55 Ω	180	260	mV
I_{IC}	Common-mode input current	Driver enabled	−0.55	0.55	mA
V_{OFF}	Off-state voltage	Driver disabled		20	mV

receiver

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
I_{IC}	Common-mode input current	Driver disabled	−20	20	μA
z_{ID}	Differential input impedance		5		kΩ
				6	pF
z_{IC}	Common-mode input impedance		20		kΩ
				24	pF
	Cable bias detect threshold, TPBx inputs		0.6	1.12	V

device

PARAMETER		TEST CONDITIONS†	MIN	MAX	UNIT
	Power status threshold	0.4-MΩ resistor	4.7	7.5	V
V_{OH}	High-level output voltage	I_{OH} = MAX, V_{CC} = MIN	3.7		V
V_{OL}	Low-level output voltage	I_{OL} = MIN, V_{CC} = MAX		0.5	V
	Positive arbitration comparator threshold		89	168	mV
	Negative arbitration comparator threshold		−168	−89	mV
	TPBIAS output voltage		1.71	2	V
V_{IT+}	Positive input threshold voltage, LREQ, CTL, D inputs		$V_{CC}/2 + 0.2$	$V_{CC}/2 + 1.1$	V
V_{IT-}	Negative input threshold voltage, LREQ, CTL, D inputs		$V_{CC}/2 - 1.1$	$V_{CC}/2 + 0.2$	V
I_{CC}	Supply current	V_{CC} = 5.25 V		140	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
	Transmit jitter			±0.8	ns
t_r	Transmit rise time	C_L = 10 pF, R_L = 55 Ω		3	ns
t_f	Transmit fall time			3	ns
t_{su}	Setup time, D, CTL, LREQ low or high before SYSCLK↑		5		ns
t_h	Hold time, D, CTL, LREQ low or high after SYSCLK↑		0		ns
t_d	Delay time, SYSCLK to D, CTL		5	13	ns

thermal characteristics

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-free-air thermal resistance	Board mounted, No air flow		50		°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance			12		°C/W

PARAMETER MEASUREMENT INFORMATION

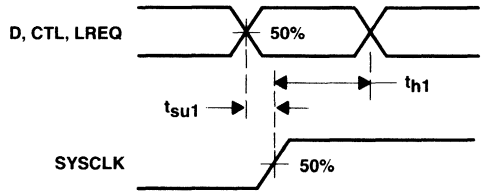


Figure 1. D, CTL Output Delay Relative to SYSCLK Waveforms

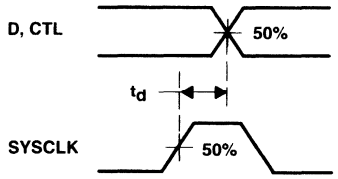


Figure 2. D, CTL, LREQ Input Setup and Hold Time Waveforms

APPLICATION INFORMATION

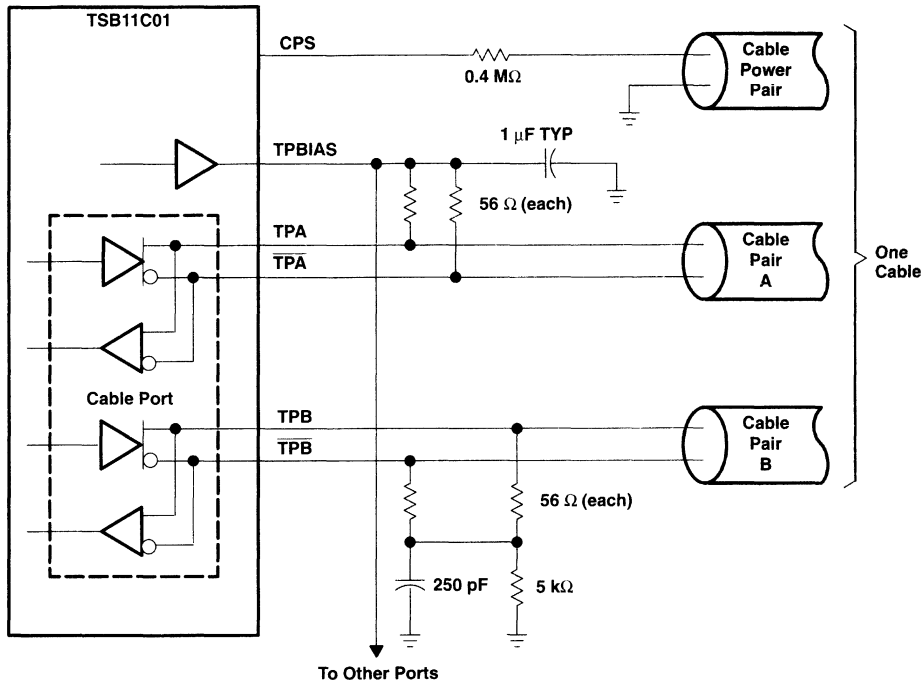


Figure 3. Twisted-Pair Cable Interface Connections

internal register configuration

The accessible internal registers of this device are listed in Table 1 and the description of the fields are listed in Table 2.

Table 1. Accessible Internal Registers

ADDRESS	0	1	2	3	4	5	6	7
0000	Physical ID						R	CPS
0001	RHB	IBR	GC					
0010	SPD		Reserved		NP			
0011	AStat1		BStat1		Ch1	Con1	Reserved	
0100	AStat2		BStat2		Ch2	Con2	Reserved	
0101	AStat3		BStat3		Ch3	Con3	Reserved	
0110	Reserved							
0111	Reserved							

APPLICATION INFORMATION

internal register configuration (continued)

Table 2. Internal Register Field Descriptions

FIELD	SIZE (Bits)	TYPE	DESCRIPTION
AStat(n)	2	Rd	These bits give the line state of TPA of port n. 11 = Z 01 = 1 10 = 0 00 = invalid
BStat(n)	2	Rd	These bits give the line state of TPB of port n, the encoding is the same as AStat(n).
Ch(n)	1	Rd	When Ch(n) = 1, then port n is a child; otherwise, it is a parent.
Con(n)	2	Rd	When Con(n) = 1, then port n is connected; otherwise it is disconnected.
CPS	1	Rd	This bit is the cable power status for the CPS terminal.
IBR	1	Rd/Wr	This bit initiates bus reset at next opportunity.
GC	6	Rd/Wr	These bits are the gap count may be changed by the serial bus manager to optimize performance. See the IEEE 1394-1995 standard for details.
NP	4	Rd	These bits are the number of ports on this TSB11C01 and are always set to 0011.
Physical ID	6	Rd	These bits contain the address of the local node determined during self identification.
R	1	Rd	This bit indicates that the local node is the root.
RHB	1	Rd/Wr	This is the root hold-off bit that instructs the local node to try to become the root during the next bus reset.
SPD	2	Rd	These bits indicate the top signalling speed of this TSB11C01 and is always cleared.

external components and connections

Cable power status (CPS): This terminal is normally connected to the cable power through a 0.4-MΩ resistor. This circuit feeds an internal comparator, which detects the presence of cable power. This information is available to the link layer controller.

Oscillator crystal (XI and XO): These terminals are usually connected to an external 24.576-MHz parallel-resonant fundamental mode crystal. The optimum values for the external shunt capacitors are dependent on the specifications of the external crystal used and on circuit board layout.

PLL/VCO filter (PDOUT and VCOIN): These terminals are for an external lag-lead filter required for stable operation of the frequency multiplier running off the crystal oscillator.

Test mode control inputs (TESTM1 and TESTM2): These terminals are used in manufacturing to enable production line testing of the TSB11C01. For normal use, these should be tied to V_{CC}.

Logic reset input ($\overline{\text{RESET}}$): When forced low, this terminal causes a bus reset condition on the active cable ports and resets the internal logic to the reset/start state. An internal pullup resistor is provided that is connected to V_{CC}, so only an external delay capacitor is required. This input is a standard logic buffer and may also be driven by a logic buffer.

Link power status input (LPS): A 10-kΩ resistor connected to V_{CC} supplying the link layer controller to monitor the link power status. When the link is not powered on, SYSCLK is disabled and the TSB11C01 performs only the basic repeater functions required for network initialization and operation.

Link request input (LREQ): An input from the link layer controller that is used by the link to signal the TSB11C01 of a request to perform some service

System clock output (SYSCLK): This terminal provides a 49.152-MHz clock signal to which the data, control, and link request information is synchronized.

APPLICATION INFORMATION

external components and connections (continued)

Control I/Os (CTL[0:1]): These terminals are bidirectional signals communicated between the TSB11C01 and the link layer controller that control passage of information between the two devices

Data I/Os (D0 and D1): These terminals are bidirectional information signals communicated between the TSB11C01 and the link layer controller

Power class bits 0 through 2 inputs (PC[0:2]): These terminals are used as inputs to set the bit values of the three power class bits in the self-ID packet. They may be programmed by tying the terminals high to V_{CC} or low to GND.

Enable external clock input (ENCLK100): This terminal is a logic input that allows a choice between using the internal crystal oscillator and PLL frequency multiplier or an external 98.304-MHz signal source. When tied high, the internal crystal oscillator and the PLL are disabled and the external clock input can be used.

External clock input (CLK100): When this terminal is asserted high (enabled), an external 98.304-MHz oscillator can drive the TSB11C01. Input voltages as low as 0.2 V peak-to-peak may be used, and the input should be ac coupled through a capacitor of 300 pF or greater. When the crystal oscillator and PLL are being used, it is recommended that this terminal be tied to GND.

Twisted-pair cable bias-voltage output (TPBIAS): This terminal provides the 1.86-V nominal bias voltage needed for proper operation of the twisted-pair cable drivers and for signalling to the remote nodes that there is a valid cable connection.

Configuration manager contender input or link-on output (C/LKON): C/LKON is a bidirectional terminal that is used as an input to specify in the self-ID packet that the node is a configuration manager contender. As an output, it signals the reception of a link-on message by supplying a 6.114-MHz signal. The bit-value programming is done by tying the terminal through a 10-kΩ resistor high (V_{CC}) or low (GND). The use of the series resistor allows the link-on output to override the input value when necessary.

Current setting resistor (R[0:1]): An internal reference voltage is applied across the resistor connected between these two terminals to set the internal operating currents and the cable driver output currents. A low temperature-coefficient (TC) resistor should be used to meet the IEEE 1394-1995 output voltage limits.

Supply filters (AV_{CC} and DV_{CC}): A combination of high-frequency decoupling capacitors is suggested for these terminals, such as paralleled 0.1 μF and 0.001 μF. These supply lines are separated on the device to provide noise isolation. They should be tied together at a low-impedance point on the circuit board. Individual filter networks are desirable.

APPLICATION INFORMATION

external components and connections (continued)

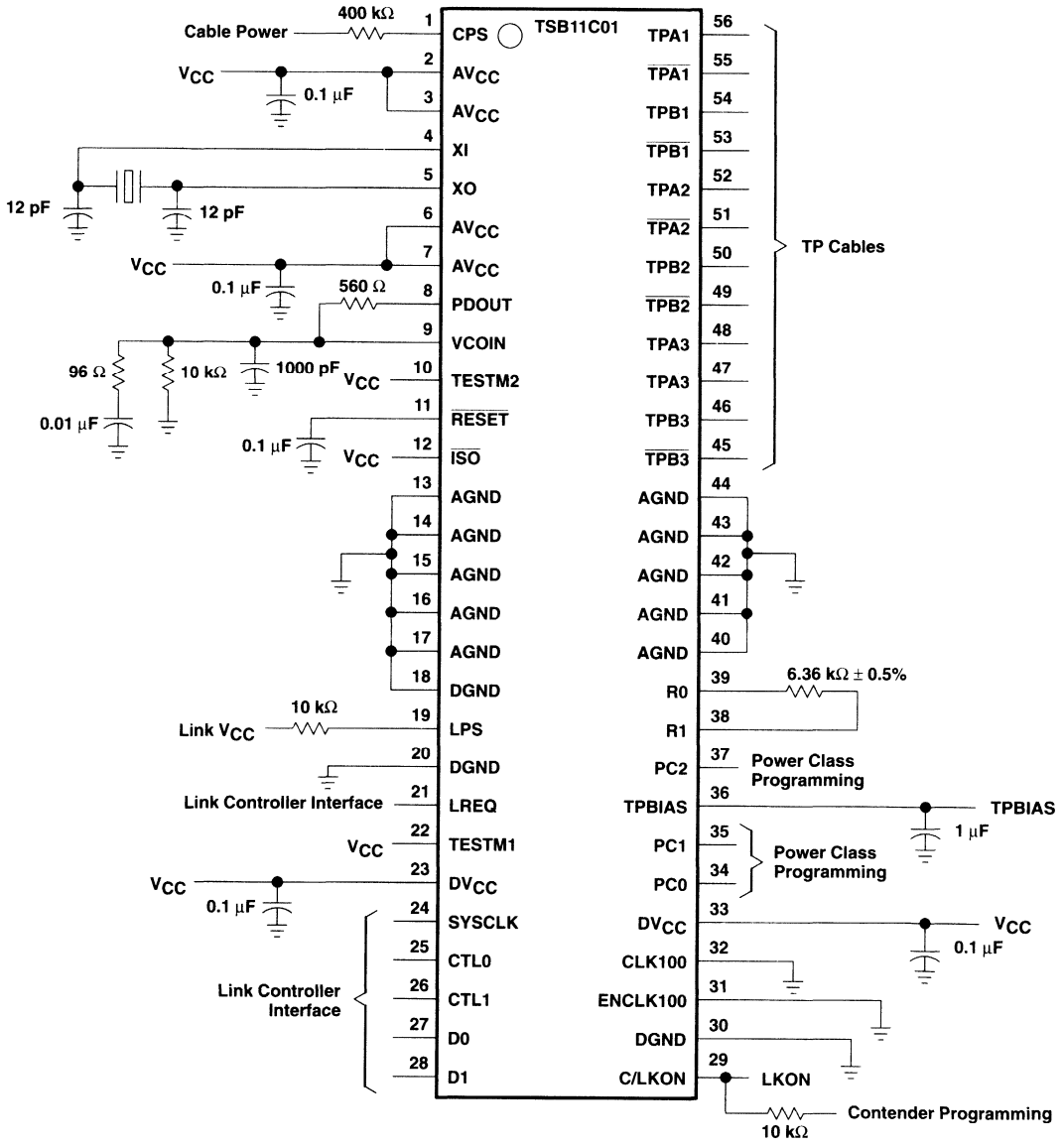


Figure 4. External Component Hookup Circuit

PRINCIPLES OF OPERATION

external components and connections (continued)

The TSB11C01 is designed to operate with a link layer controller such as the Texas Instruments TSB12C01A. These devices use an interface described in annex I of the IEEE 1394-1995 standard. Details of how the TSB12C01A devices operate are described in the TSB12C01A data manual (literature number SLLS219). The following describes the operation of the physical (phy) link interface.

The TSB11C01 supports 100 Mbits/s data transfers and has two bidirectional data lines D[0:1] crossing the interface. In addition, there are two bidirectional control lines CTL[0:1], the 50-MHz SYSCLK line from the TSB11C01 to the link, and the link request line (LREQ) from the link to the TSB11C01. The TSB11C01 has control of all the bidirectional terminals. The link is allowed to drive these terminals only after it has been given permission by the TSB11C01. The dedicated LREQ request terminal is used by the link for any activity it wishes to initiate.

There are four operations that may occur in the phy link interface: request, status, transmit, and receive. With the exception of the request operation, all actions are initiated by the TSB11C01.

When the TSB11C01 has control of the bus the CTL[0:1] lines are encoded as shown in Table 3.

Table 3. TSB11C01 Control of Bus Functions

CTL [0:1]	NAME	DESCRIPTION OF ACTIVITY
00	Idle	No activity is occurring (this is the default mode).
01	Status	Status information is being sent from the TSB11C01 to the link
10	Receive	An incoming packet is being sent from the TSB11C01 to the link
11	Transmit	The link has been given control of the bus to send an outgoing packet.

When the link has control of the bus (TSB11C01 permission) the CTL[0:1] lines are encoded as shown in Table 4.

Table 4. Link Control of Bus Functions

CTL [0:1]	NAME	DESCRIPTION OF ACTIVITY
00	Idle	The link has released the bus (transmission has been completed).
01	Hold	The link is holding the bus prior to sending a packet.
10	Transmit	An outgoing packet is being sent from the link to the TSB11C01.
11	Reserved	None

When the link wishes to request the bus or access a register that is located in the TSB11C01, a serial stream of information is sent across the LREQ line. The length of the stream varies depending on whether the transfer is a bus request, a read command, or a write command (see Table 5). Regardless of the type of transfer, a start bit of 1 is required at the beginning of the stream and a stop bit of 0 is required at the end of the stream. Bit 0 is the most significant and is transmitted first.

Table 5. Link Request Functions

NO. of BITS	REQUEST TYPE
7	Bus Request
9	Read Register Request
17	Write Register Request

PRINCIPLES OF OPERATION

external components and connections (continued)

For a bus request, the length of the LREQ data stream is 7 bits, as shown in Table 6.

Table 6. Bus Request Functions

BIT(S)	NAME	DESCRIPTION
0	Start Bit	This bit indicates the beginning of the transfer (always a 1).
1–3	Request Type	This bit indicates the type of bus request (see Table 7 for the encoding of this field).
4–5	Request Speed	These bits should always be 00 for the TSB11C01 100-Mbits/s speed.
6	Stop Bit	This bit indicates the end of the transfer (always a 0).

For a read register request, the length of the LREQ data stream is 9 bits, as shown in Table 7.

Table 7. Read Register Request Functions

BIT(S)	NAME	DESCRIPTION
0	Start Bit	This bit indicates the beginning of the transfer (always a 1).
1–3	Request Type	These bits are always a 100 indicating that this is a read register request.
4–7	Address	These bits contain the address of the TSB11C01 register to be read.
8	Stop Bit	This bit indicates the end of the transfer (always a 0).

For a write register request, the length of the LREQ data stream is 17 bits, as shown in Table 8 and LREQ timing is shown in Figure 5.

Table 8. Write Register Request Functions

BIT(S)	NAME	DESCRIPTION
0	Start Bit	This bit indicates the beginning of the transfer (always a 1).
1–3	Request Type	These bits are always a 101 indicating that this is a write register request.
4–7	Address	These bits contain the address of the TSB11C01 register to be written to.
8–15	Data	These bits contain the data that is to be written to the specified register address.
16	Stop Bit	This bit indicates the end of the transfer (always a 0).

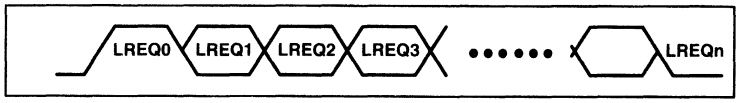


Figure 5. LREQ Timing (Each Cell Represents One Clock-Sample Time)

PRINCIPLES OF OPERATION

external components and connections (continued)

The 3-bit request-type field has the following possible values as shown in Table 9.

Table 9. Request Functions

LREQ[1:3]	NAME	DESCRIPTION
000	TakeBus	Immediate request. Upon detection of an idle, take control of the bus immediately (no arbitration).
001	IsoReq	Isochronous request. Arbitrate after an isochronous gap.
010	PriReq	Priority request. Arbitrate after a fair gap, ignore fair protocol.
011	FairReq	Fair request. Arbitrate after a fair gap; use fair protocol.
100	RdReg	Return the specified register contents through a status transfer.
101	WrReg	Write to the specified register.
110, 111	Reserved	Reserved

bus request

For fair or priority access, the link requests control of the bus at least one clock after the phy link interface becomes idle. When the link senses that the CTL terminals are in a receive state (CTL[0:1] = 10), it knows that the request has been lost. This is true any time during or after the link sends the bus request transfer. The TSB11C01 ignores any fair or priority requests when it asserts the receive state while the link is requesting the bus. The link then reissues the request one clock after the next interface idle.

The cycle master uses a normal priority request to send a cycle start message. After receiving a cycle start, the link can issue an isochronous bus request. When arbitration is won, the link proceeds with the isochronous transfer of data. The isochronous request is cleared in the TSB11C01 once the link sends another type of request or when the isochronous transfer has been completed.

The TakeBus request is issued when the link needs to send an acknowledgment after reception of a packet addressed to it. This request must be issued during packet reception. This is done to minimize the delays that the TSB11C01 has to wait between the end of a packet and the transmittal of an acknowledgment. As soon as the packet ends, the TSB11C01 immediately grants access of the bus to the link. The link sends an acknowledgment to the sender unless the header cycle redundancy check (CRC) of the packet is bad. In this case, the link releases the bus immediately; it is not be allowed to send another type of packet on this grant. To ensure this, the link is forced to wait 160 ns after the end of the packet is received. The TSB11C01 then gains control of the bus and the acknowledgment indicating the CRC error is sent. The bus is released and allowed to proceed with another request.

It is conceivable that two separate nodes might believe that an incoming packet is intended for them. The nodes then issue a TakeBus request before checking the CRC of the packet. Since both nodes seize control of the bus at the same time, a temporary localized collision of the bus occurs somewhere between the competing nodes. This collision would be interpreted by the other nodes on the network as being a ZZ line state, not a bus reset. As soon as the two nodes check the CRC, the mistaken node drops its request and the false line state is removed. The only side effect is the loss of the intended acknowledgment packet (this is handled by the higher layer protocol).

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read/write requests

When the link requests to read the specified register contents, the TSB11C01 sends the contents of the register to the link through a status transfer. If an incoming packet is received while the TSB11C01 is transferring status information to the link, the TSB11C01 continues to attempt to transfer the contents of the register until it is successful.

For write requests, the TSB11C01 loads the data field into the appropriately addressed register as soon as the transfer has been completed. The link is allowed to request read or write operations at any time.

A status transfer is initiated by the TSB11C01 when it has some status information to transfer to the link. The transfer is initiated by asserting CTL[0:1] = 01 and D[0:1] = 00 (100 Mbits/s only). The D[0:1] = 00 represents the speed at which the status transfer is to occur; status information at 100 Mbits/s is always transmitted two bits at a time.

The status transfer can be interrupted by an incoming packet from another node. When this occurs, the TSB11C01 attempts to resend the status information after the packet has been acted upon. The TSB11C01 continues to attempt to complete the transfer until the information has been successfully transmitted.

NOTE

There must be at least one idle cycle between consecutive status transfers. The definition of the bits in the status transfer is shown in Table 10.

status request

Length of stream: 4 or 16 bits

Table 10. Status Request Functions

BIT(s)	NAME	DESCRIPTION
0	Arbitration Reset Gap	This bit indicates that the TSB11C01 has detected that the bus has been idle for an arbitration reset gap time (this time is defined in the IEEE 1394-1995 standard). This bit is used by the link in its busy/retry state machine.
1	Subaction Gap	This bit indicates that the TSB11C01 has detected that the bus has been idle for a subaction gap time (this time is defined in the IEEE 1394-1995 standard). This bit is used by the link to detect the completion of an isochronous cycle.
2	Bus Reset	This bit indicates that the TSB11C01 has entered the bus reset state
3	State Time Out	The TSB11C01 has stayed in a particular state for too long.
4–7	Address	These bits hold the address of the TSB11C01 register whose contents are transferred to the link.
8–15	Data	The data that is to be sent to the link

Normally, the TSB11C01 sends just the first 4 bits of status data to the link. These bits are used by the link state machines; however, when the link has initiated a read register request the TSB11C01 sends the full status packet to the link (see Figure 6). The TSB11C01 also sends a full status packet to the link if it has some important information to pass on to the link. Currently, the only condition where this occurs is after the self identification process when the TSB11C01 needs to inform the link of its new node address (physical ID register).

PRINCIPLES OF OPERATION

status request (continued)

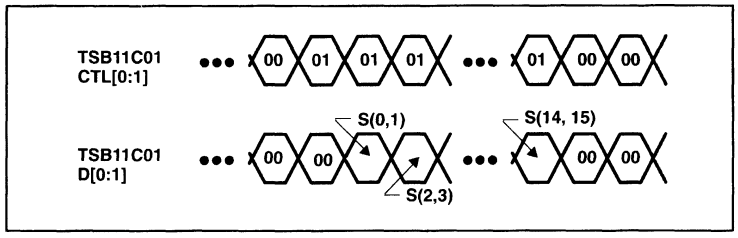


Figure 6. Status Transfer Timing

There may be times where the TSB11C01 wants to start a second status transfer. The TSB11C01 waits at least one clock cycle with the CTL lines idle before it begins a second transfer.

transmit

When the link wants to transmit information, it first requests access to the bus through the LREQ line. When the TSB11C01 receives this request, it arbitrates to gain control of the bus. When the TSB11C01 wins ownership of the bus, it grants the bus to the link by asserting the transmit state on the CTL terminals for at least one SYSCLK cycle. The link takes control of the bus by asserting either hold or transmit on the CTL lines. Hold is used by the link to keep control of the bus if it needs more time to prepare the data for transmission. The TSB11C01 keeps control of the bus for the link by asserting a data-on state on the bus. It is not necessary for the link to use hold when it is ready to transmit as soon as bus ownership is granted.

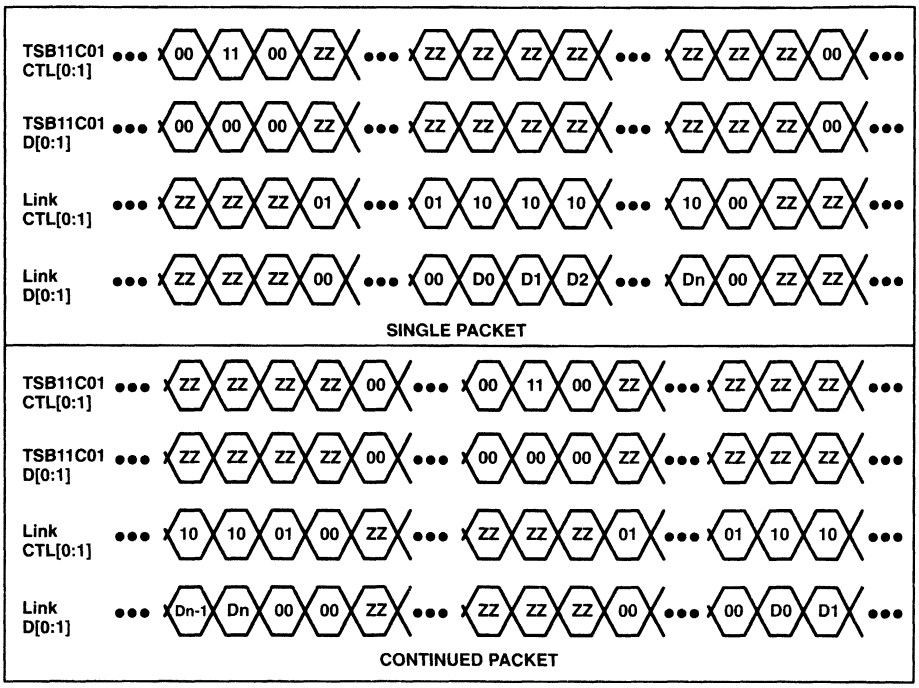
When the link is prepared to send data, it asserts transmit on the CTL lines as well as sending the first bits of the packet on the D[0:1] lines. The transmit state is held on the CTL terminals until the last bits of data have been sent. The link then asserts idle on the CTL lines for one clock cycle, after which it releases control of the interface.

There are times when the link needs to send another packet without releasing the bus. For example, the link may want to send consecutive isochronous packets or it may want to attach a response to an acknowledgment. To do this, the link asserts hold instead of idle when the first packet of data has been completely transmitted. Hold, in this case, informs the TSB11C01 that the link needs to send another packet without releasing control of the bus. The TSB11C01 waits a set amount of time before asserting transmit, and the link can then proceed with the transmission of the second packet. After all data has been transmitted and the link has asserted idle on the CTL lines, the TSB11C01 asserts its own idle state on the CTL lines. When sending multiple packets in this fashion, all data must be transmitted at the same speed. This is because the transmission speed is set during arbitration, and since the arbitration step is skipped, there is no way of informing the network of a change in speed.

PRINCIPLES OF OPERATION

transmit timing

Transmit timing is shown in Figure 7.



ZZ = high-impedance state D0 – Dn = packet data

Figure 7. Transmit Timing

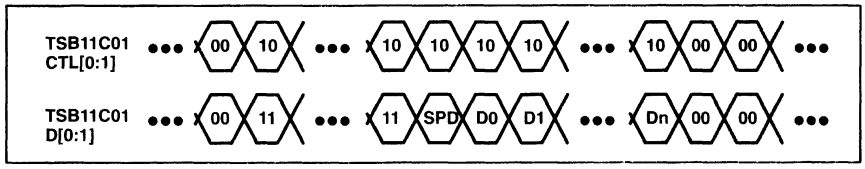
receive operation

When data is received by the TSB11C01 from the serial bus, it transfers the data to the link for further processing. The TSB11C01 asserts receive (10) on the CTL lines and 11 on the D lines. The TSB11C01 indicates the start of the packet by placing the speed code on the data bus. The TSB11C01 then proceeds with the transmission of the packet to the link on the D lines while keeping the receive status on the CTL lines. Once the packet has been completely transferred, the TSB11C01 asserts idle on the CTL lines to complete the receive operation. The speed code is a phy link protocol and not included in the CRC.

PRINCIPLES OF OPERATION

receive timing

The receive timing is shown in Figure 8.



SPD = speed code D0 – Dn = packet data

Figure 8. Receive Timing

The speed code for the receiver is shown in Table 11.

Table 11. Receiver Speed Code

D[0:1]	DATA RATE
00	100 Mbits/s

TSB12C01A
Data Manual

1394 High-Speed Serial-Bus Link-Layer Controller

TEXAS INSTRUMENTS

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1 Overview

1.1 Description

The TSB12C01A is an IEEE-1394 standard (from now on referred to only as 1394) high-speed serial-bus link-layer controller that allows for easy integration into an I/O subsystem. The TSB12C01A transmits and receives correctly formatted 1394 packets and generates and inspects the 32-bit cyclic redundancy check (CRC). The TSB12C01A is capable of being a cycle master and supports reception of isochronous data on two channels. It interfaces directly to the TSB11C01, TSB11LV01, and TSB21LV03 physical-layer chips and can support bus speeds of 100, 200, and 400 Mb/s. The TSB12C01A has a generic 32-bit host bus interface, which makes connection to most 32-bit host buses very simple. The TSB12C01A has software-adjustable FIFOs for optimal FIFO size and performance characterization and allows for variable-size asynchronous-transmit FIFO (ATF), isochronous-transmit FIFO (ITF), and general-receive FIFO (GRF).

This document is not intended to serve as a tutorial on 1394; users should refer to the IEEE draft standard 1394 serial bus for detailed information regarding the 1394 high-speed serial bus.

1.2 Features

The following are features of the TSB12C01A.

1.2.1 Link

- Complies With IEEE-1394 Standard Version 7.1v1
- Transmits and Receives Correctly Formatted 1394 Packets
- Supports Isochronous Data Transfer
- Performs Function of Cycle Master
- Generates and Checks 32-Bit CRC
- Detects Lost Cycle-Start Messages
- Contains Asynchronous, Isochronous, and General-Receive FIFOs

1.2.2 Physical-Link Interface

- Interfaces Directly to the TSB11C01, TSB11LV01, and TSB21LV03 Phy Chips
- Supports Speeds of 100, 200, and 400 Mb/s
- Implements the Physical-Link Interface Described in Annex J of the IEEE-1394 Standard

1.2.3 Host Bus Interface

- Provides Chip Control With Directly Addressable Registers
- Is Interrupt Driven to Minimize Host Polling
- Has a Generic 32-Bit Host Bus Interface

1.2.4 General

- Requires a Single 5-V ±5% Power Supply
- Manufactured with low-Power CMOS Technology
- Packaged in a 100-Pin thin quad flat package (TQFP) (PZ Package)

2 Architecture

2.1 Functional Block Diagram

The functional block architecture of the TSB12C01A is shown in Figure 2–1.

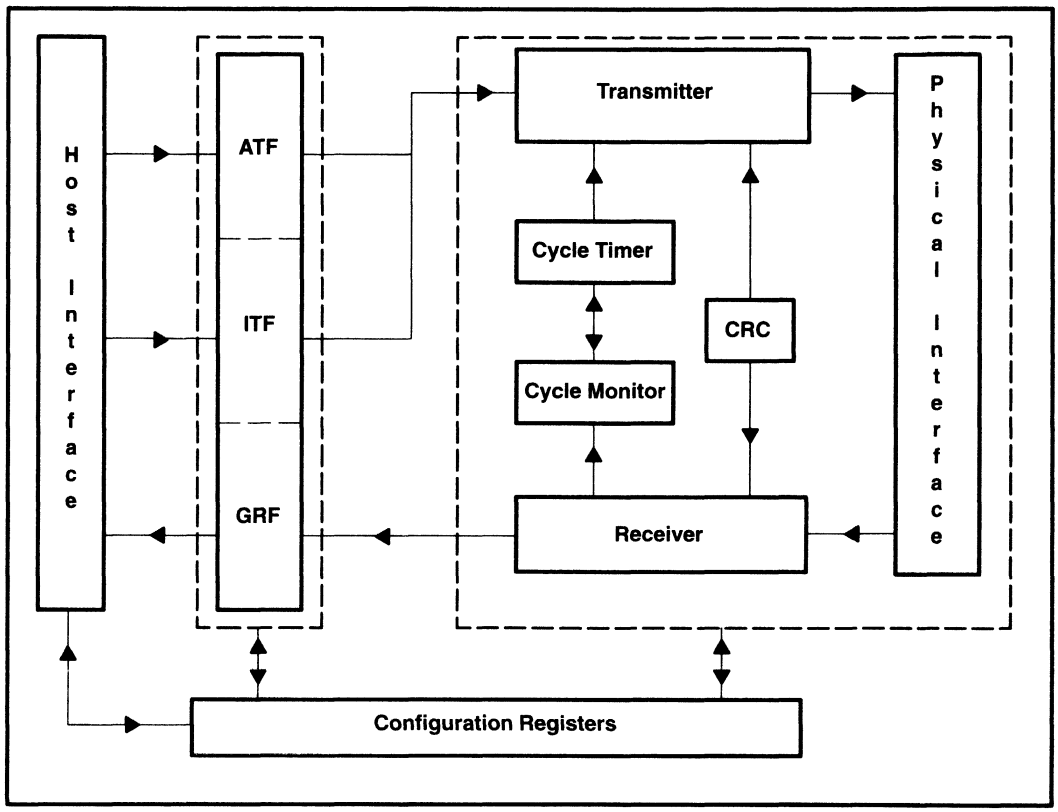


Figure 2–1. TSB12C01A Block Diagram

2.1.1 Physical Interface

The physical (phy) interface provides phy-level services to the transmitter and receiver. This includes gaining access to the serial bus, sending packets, receiving packets, and sending and receiving acknowledge packets.

The phy interface module also interfaces to the phy chip and conforms to the phy-link interface specification described in Annex J of the IEEE-1394 standard (refer to section 7 of this document for more information).

2.1.2 Transmitter

The transmitter retrieves data from either the ATF or the ITF and creates correctly formatted serial-bus packets to be transmitted through the phy interface. When data is present at the ATF interface to the transmitter, the TSB12C01A phy interface arbitrates for the serial bus and sends a packet. When data is present at the ITF interface to the transmitter, the TSB12C01A arbitrates for the serial bus during the next isochronous cycle. The transmitter autonomously sends the cycle-start packets when the chip is a cycle master.

2.1.3 Receiver

The receiver takes incoming data from the phy interface and determines if the incoming data is addressed to this node. If the incoming packet is addressed to this node, the CRC of the packet is checked. If the header CRC is good, the header is confirmed in the GRF. For block and isochronous packets, the remainder of the packet is confirmed one quadlet at a time. The receiver places a status quadlet in the GRF after the last quadlet of the packet is confirmed in the GRF. The status quadlet contains the error code for the packet. The error code is the acknowledge code that is sent for that packet. For broadcast packets that do not need acknowledge packets, the error code is the acknowledge code that would have been sent. This acknowledge code tells the transaction layer whether or not the data CRC is good or bad. When the header CRC is bad, the header is flushed and the rest of the packet is ignored.

When a cycle-start message is received, it is detected and the cycle-start message data is sent to the cycle timer. The cycle-start messages are not placed in the GRF like other quadlet packets. At the end of an isochronous cycle and if the cycle mark enable (CyMrkEn) bit of the control register is set , the receiver inserts a cycle-mark packet in the GRF to indicate the end of the isochronous cycle.

2.1.4 Transmit and Receive FIFOs

The TSB12C01A contains two transmit FIFOs (asynchronous and isochronous) and one receive FIFO (general receive). Each of these FIFOs are one quadlet wide and their length is software adjustable. These software-adjustable FIFOs allow customization of the size of each FIFO for individual applications. The sum of all FIFOs cannot be larger than 509 quadlets. To understand how to set the size of the FIFOs, see sections 3.2.11 through 3.2.13. The transmit FIFOs are write only from the host bus interface, and the receive FIFO is read only from the host bus interface.

An example of how to use software-adjustable FIFOs follows:

> In applications where isochronous packets are large and asynchronous packets are small, the implementer can set the ITF and GRF to a large size (200 quadlets each) and set the ATF to a smaller size (100 quadlets). Notice that the sum of all FIFOs is less than or equal to 509 quadlets.

2.1.5 Cycle Timer

The cycle timer is used by nodes that support isochronous data transfer. The cycle timer is a 32-bit cycle-timer register. Each node with isochronous data-transfer capability has a cycle-timer register as defined in the IEEE-1394 standard. In the TSB12C01A, the cycle-timer register is implemented in the cycle timer and is located in IEEE-1212 initial register space at location 200h and can also be accessed through the local bus at address 14h. The low-order 12 bits of the timer are a modulo 3072 counter, which increments once every 24.576-MHz clock periods (or 40.69 ns). The next 13 higher-order bits are a count of 8, 000-Hz (or 125 μs)cycles, and the highest 7 bits count seconds.

The cycle timer contains the cycle-timer register. The cycle-timer register consists of three fields: cycle offset, cycle count, and seconds count. The cycle timer has two possible sources. First, if the cycle source (CySrc) bit in the configuration register is set, then the CYCLEIN input causes the cycle count field to increment for each positive transition of the CYCLEIN input (8 kHz) and the cycle offset resets to all zeros. CYCLEIN should only be the source when the node is cycle master. When the cycle-count field increments, CYCLEOUT is generated. The timer can also be disabled using the cycle-timer-enable bit in the control register. See section 3.2.5, Cycle-Timer Register for more information.

The second cycle-source option is when the CySrc bit is cleared. In this state, the cycle-offset field of the cycle-timer register is incremented by the internal 24.576-MHz clock. The cycle timer is updated by the reception of the cycle-start packet for the noncycle master nodes. Each time the cycle-offset field rolls over, the cycle-count field is incremented and the CYCLEOUT signal is generated. The cycle-offset field in the cycle-start packet is used by the cycle-master node to keep all nodes in phase and running with a nominal isochronous cycle of 125 μs.

CYCLEOUT indicates to the cyclemaster node that it is time to send a cycle-start packet. And, on noncyclemaster nodes, CYCLEOUT indicates that it is time to expect a cycle-start packet. The cycle-start bit is set when the cycle-start packet is sent from the cyclemaster node or received by a noncyclemaster node.

2.1.6 Cycle Monitor

The cycle monitor is only used by nodes that support isochronous data transfer. The cycle monitor observes chip activity and handles scheduling of isochronous activity. When a cycle-start message is received or sent, the cycle monitor sets the cycle-started interrupt bit. It also detects missing cycle-start packets and sets the cycle-lost interrupt bit when this occurs. When the isochronous cycle is complete, the cycle monitor sets the cycle-done-interrupt bit. The cycle monitor instructs the transmitter to send a cycle-start message when the cycle-master bit is set in the control register.

2.1.7 Cyclic Redundancy Check (CRC)

The CRC module generates a 32-bit CRC for error detection. This is done for both the header and data. The CRC module generates the header and data CRC for transmitting packets and checks the header and data CRC for received packets. See the IEEE-1394 standard for details on the generation of the CRC†.

2.1.8 Internal Registers

The internal registers control the operation of the TSB12C01A. The register definitions are specified in section 3.

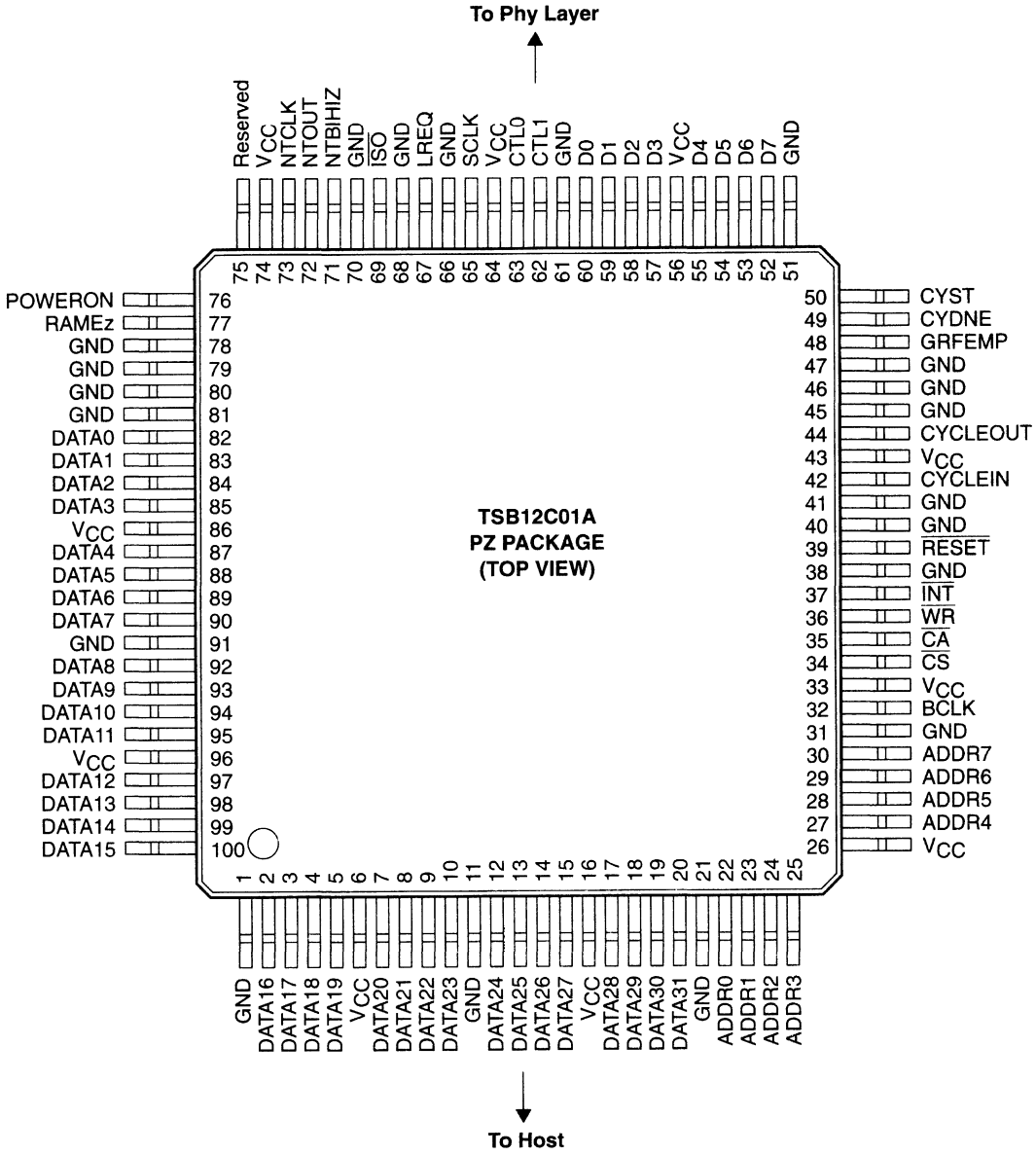
2.1.9 Host Bus Interface

The host bus interface allows the TSB12C01A to be easily connected to most host processors. This host bus interface consists of a 32-bit data bus and an 8-bit address bus. The TSB12C01A utilizes cycle-start and cycle-acknowledge handshake signals to allow the local bus clock and the 1394 clock to be asynchronous to one another. The TSB12C01A is interrupt driven to reduce polling.

† This is the same CRC used by the IEEE802 LANs and the X3T9.5 FDDI.

2.2 Terminal Assignments and Functions

2.2.1 Terminal Assignments



NOTES: A. Tie reserved terminals to GND.

B. Bit 0 is the most significant bit (MSB).

2.2.2 Terminal Functions

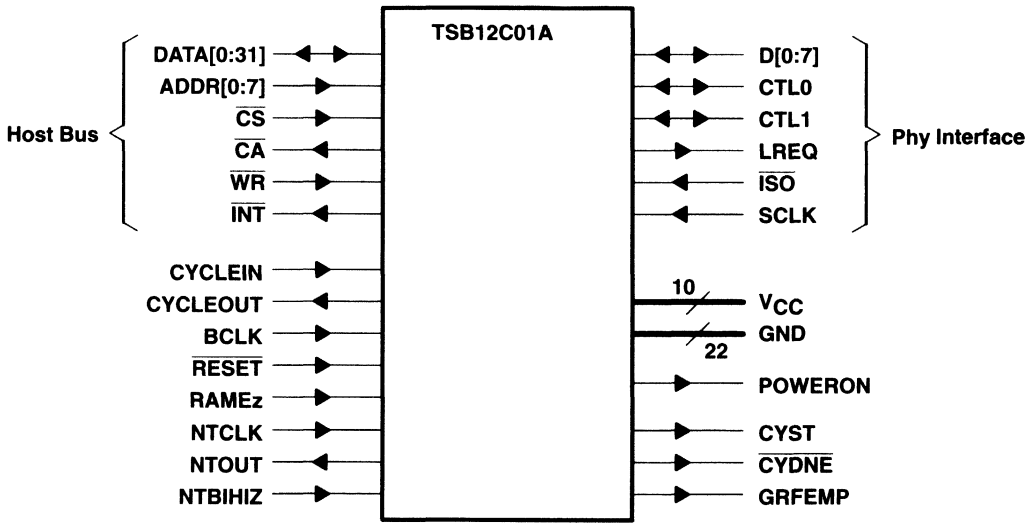


Figure 2–2. TSB12C01A Terminal Functions

2.2.3 TSB12C01A Terminal Functions

Table 2–1. Host Bus Interface Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ADDR[0:7]	22–25 27–30	I	Address 0 through address 7. Host bus address bus bits 0 through 7 that address the quadlet-aligned FIFOs and configuration registers. The two least significant address lines, 6 and 7, must be grounded.
$\overline{CA}$	35	O	Cycle acknowledge (active low). $\overline{CA}$ is a TSB12C01A control signal to the host bus. When asserted (low), access to the configuration registers or FIFO is complete.
$\overline{CS}$	34	I	Cycle start (active low). $\overline{CS}$ is a host bus control signal to enable access to the configuration registers or FIFO.
DATA [0:31]	2–5 7–10 12–15 17–20 82–85 87–90 92–95 97–100	I/O	Data 0 through 31. DATA is a host bus data bus bits 0 through 31.
$\overline{INT}$	37	O	Interrupt (active low). When $\overline{INT}$ is asserted (low), the TSB12C01A notifies the host bus that an interrupt has occurred.
$\overline{WR}$	36	I	Read/write enable. When $\overline{WR}$ is deasserted (high) in conjunction with $\overline{CS}$, a read from the TSB12C01A is requested. When $\overline{WR}$ is asserted (low) in conjunction with $\overline{CS}$, a write to the TSB12C01A is requested.

Table 2–2. Phy Interface Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CTL1, CTL0	62, 63	I/O	Control 1 and control 0 of the phy-link control bus. CTL1 and CTL0 indicate the four operations that can occur in this interface (see section 7 or annex J of the IEEE-1394 standard for more information about the four operations).
D[0:7]	52–55 57–60	I/O	Data 0 through data 7 of the phy-link data bus. Data is expected on D[0:1] for 100 Mb/s packets, D[0:3] for 200 Mb/s, and D[0:7] for 400 Mb/s.
$\overline{\text{ISO}}$	69	I	Isolation barrier (active low). This $\overline{\text{ISO}}$ is asserted (low) when an isolation barrier is present.
LREQ	67	O	Link request. LREQ is a TSB12C01A output that makes bus requests and accesses the phy layer.
POWERON	76	O	Power on indicator to phy interface. When active, POWERON has a clock output with 1/32 of the BCLK frequency and indicates to the phy interface that the TSB12C01A is powered.

Table 2–3. Miscellaneous Signals Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BCLK	32	I	Bus clock. BCLK is the host bus clock used in the host-interface module of the TSB12C01A. It is asynchronous to SCLK.
CYCLEIN	42	I	Cycle in. CYCLEIN is an optional external 8,000-Hz clock used as the cycle clock, and it should only be used when attached to the cycle-master node. It is enabled by the cycle source bit and should be tied high when not used.
CYCLEOUT	44	O	Cycle out. CYCLEOUT is the TSB12C01A version of the cycle clock. It is based on the timer controls and received cycle-start messages.
CYDNE	49	O	Status of CyDne bit. When the RevAEn bit of the control register is set, CYDNE indicates the value of the CyDne bit of the interrupt register. When RevAEn is cleared, CYDNE is a 3-state output.
CYST	50	O	Status of CySt bit. When the RevAEn bit of the control register is set, CYST indicates the value of the CySt bit of the interrupt register. When RevAEn is cleared, CYST is a 3-state output.
GND	1, 11, 21, 31, 38, 40, 41, 45–47, 51, 61, 66, 68, 70, 78–81, 91		Ground reference
GRFEMP	48	O	Status of Empty bit. When the RevAEn bit of the control register is set, GRFEMP indicates the value of the Empty bit of the GRF status register. When RevAEn is cleared, GRFEMP is a 3-state output.
RAMEz	77	I	RAM 3-state enable. When RAMEz is deasserted (low), FIFOs are enabled. When RAMEz is asserted, the FIFOs are 3-state outputs. (This is a manufacturing test-mode condition and should be grounded under normal operating conditions.)
NTBIHIZ	71	I	NAND-tree bidirectional 3-state output. When NTBIHIZ is deasserted (low), the bidirectional I/Os operate in a normal state. When NTBIHZ is asserted (high), the bidirectional I/Os are in the 3-state output mode. (This is a manufacturing test-mode condition and should be grounded under normal operating conditions.)

Table 2–3. Miscellaneous Signals Terminal Functions (Continued)

NTCLK	73	I	NAND clock input. The NAND-tree clock is used for V_{IH} and V_{IL} manufacturing tests. (This input should be grounded under normal operating conditions.)
NTOUT	72	O	NAND-tree output. This output should remain open under normal operating conditions.
$\overline{\text{RESET}}$	39	I	Reset (active low). $\overline{\text{RESET}}$ is the asynchronous reset to the TSB12C01A.
SCLK	65	I	System clock. SCLK is a 49.152-MHz clock from the phy, that generates the 24.576-MHz clock.
V_{CC}	6, 16, 26, 33, 43, 56, 64, 74, 86, 96		5-V ±5% power supplies

3 Internal Registers

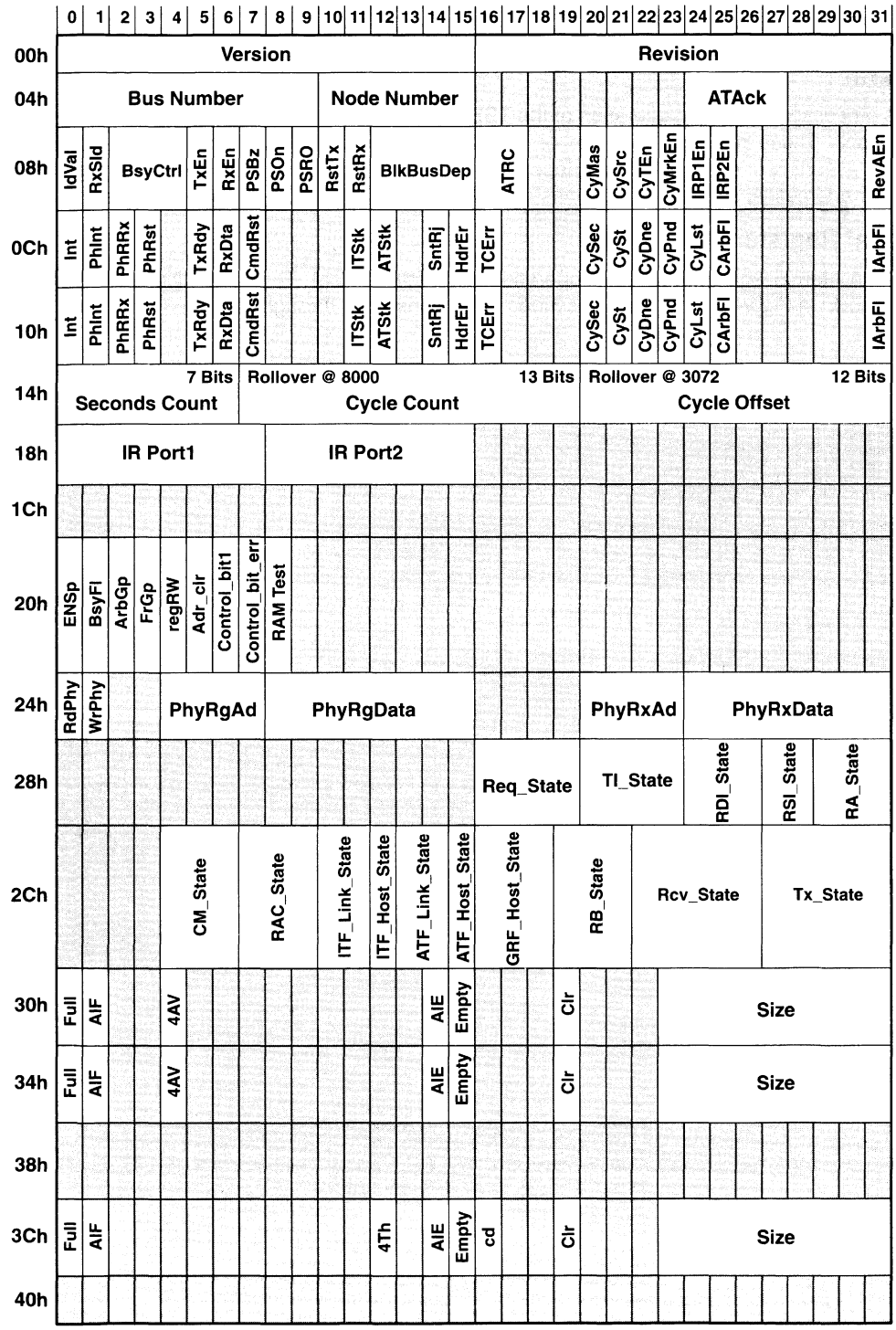
3.1 General

The host-bus processor directs the operation of the TSB12C01A through a set of registers internal to the TSB12C01A itself. These registers are read or written by asserting $\overline{CS}$ with the proper address on ADDR[0:7] and asserting or deasserting $\overline{WR}$ depending on whether a read or write is needed. Figure 3–1 lists the register addresses; subsequent sections describe the function of the various registers.

3.2 Internal Register Definitions

The TSB12C01A internal registers control the operation of the TSB12C01A. The bit definitions of the internal registers are shown in Figure 3–1 and are described in sections 3.2.1 through 3.2.13.

Figure 3–1. Internal Register Map



NOTE A: All gray areas (bits) are reserved bits.

3.2.1 Version/Revision Register

The version/revision register allows software to be written that supports multiple versions of the high-speed serial-bus link-layer controllers. This register is at address 00h and is read only. The initial value is 3031_3041h.

Table 3–1. Version/Revision Register Field Descriptions

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0–15	Version	Version	Version of the TSB12C01A
16–31	Revision	Revision	Revision of the TSB12C01A

3.2.2 Node-Address/Transmitter Acknowledge Register

The node-address/transmitter acknowledge register controls which packets are accepted/rejected, and it presents the last acknowledge received for packets sent from the ATF. This register is at offset 04h. The bus number and node number fields are read/write. The AT acknowledge (ATAck) received is normally read only. Setting the regRW bit in the diagnostic register makes these fields read/write. The initial value is FFFF_0000h.

Table 3–2. Node-Address/Transmitter Acknowledge Register Field Descriptions

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0–9	BusNumber	Bus number	BusNumber is the 10-bit IEEE 1212 bus number that the TSB12C01A uses with the node number in the SOURCE address for outgoing packets and to accept or reject incoming packets. The TSB12C01A always accepts packets with a bus number equal to 3FFh.
10–15	NodeNumber	Node number	NodeNumber is the 6-bit node number that the TSB12C01A uses with the bus number in the source address for outgoing packets and to accept or reject incoming packets. The TSB12C01A always accepts packets with the node address equal to 3Fh. See BlkBusDep bits for exceptions.
16–23	Reserved	Reserved	Reserved
24–27	ATAck	Address transmitter acknowledge received	ATAck is the last acknowledge received by the transmitting node in response to a packet sent from the asynchronous transmit-FIFO.
28–31	Reserved	Reserved	Reserved

3.2.3 Control Register

The control register dictates the basic operation of the TSB12C01A. This register is at address 08h and is read/write. The initial value is 0000_0000h.

Table 3–3. Control-Register Field Descriptions

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0	IdVal	ID Valid	When IdVal is set, the TSB12C01A accepts packets addressed to the IEEE 1212 address set (Node Number) in the node-address register. When IdVal is cleared, the TSB12C01A accepts only broadcast packets.
1	RxSId	Received self-ID packets	When RxSId is set, the self-identification packets generated by phy chips during bus initialization are received and placed into the GRF as a single packet. Each self-identification packet is composed of two quadlets, where the second quadlet is the logical inverse of the first. If ACK (4 bits) equals 1h, then the data is good. If ACK equals Dh, then the data is wrong.

Table 3–3. Control-Register Field Descriptions (Continued)

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
2–4	BsyCtrl	Busy control	These bits control which busy status the chip returns to incoming packets. The field is defined as below: 000 = follow normal busy/retry protocol, only send busy when necessary. 001 = send busyA when it is necessary to send a busy acknowledge. 010 = send busyB when it is necessary to send a busy acknowledge. 011 = reserved 100 = send a busy acknowledge to all incoming packets following the normal busy/retry protocol. 101 = send a busy acknowledge to all incoming packets by sending a busyA acknowledge. 110 = send a busy acknowledge to all incoming packets by sending a busyB acknowledge. 111 = reserved When retry_X is received and the receiving node needs to send a busy acknowledge signal, it sends an ack_busy_X signal.
5	TxEn	Transmitter enable	When TxEn is cleared, the transmitter does not arbitrate or send packets.
6	RxEn	Receiver enable	When is RXEn cleared, the receiver does not receive any packets.
7	PSBz	Physical DMA busy	When: 1) PSOn is set, 2) PSRO is cleared or the incoming packet is a read, 3) destination offset is in lower 4 Gbytes, and 4) PSBz is set, the TSB12C01A sends a busy acknowledge to the incoming packet.
8	PSOn	Physical DMA on	When PSOn is set, the TSB12C01A uses PSRO and PSBz to determine acceptance of incoming request packets addressed to the lower 4 Gbytes of initial memory space.
9	PSRO	Physical DMA read only	When PSOn is set, the TSB12C01A uses PSRO to determine acceptance of incoming write request packets addressed to the lower 4 Gbytes of initial memory space.
10	RstTx	Reset transmitter	When RstTx is set, the entire transmitter resets synchronously. This bit clears itself.
11	RstRx	Reset receiver	When RstRx is set, the entire receiver resets synchronously. This bit clears itself.
12–15	BlkBusDep	Block bus-dependent address	This field is used by the receiver to filter out broadcast packets to the bus-dependent area of CSR space. Setting the LSB of this field disables the reception of broadcast packets to the lowest 128 bytes of bus-dependent CSR space. Setting the MSB of this field disables the reception of broadcast packets to the highest 128 bytes of bus-dependent CSR space.
16–17	ATRC	AT retry code	This field contains the last retry code received. This code is logically ORed with the retry code field (00) in the transmit packet, and the packet is resent. This alleviates the need to change the retry code in the transmit packet. The retry encoding follows the IEEE-1394 standard 7.1v1. The retry code is as follows: 00 retry_o (new) 01 retry_X 10 retry_A 11 retry_B

Table 3–3. Control-Register Field Descriptions (Continued)

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
18–19	Reserved	Reserved	Reserved
20	CyMas	Cycle master	When CyMas is set and the TSB12C01A is attached to the root phy, the cyclemaster function is enabled. When the cycle_count field of the cycle timer register increments, the transmitter sends a cycle-start packet.
21	CySrc	Cycle source	When CySrc is set, the cycle_count field increments and the cycle_offset field resets for each positive transition of CYCLEIN. When CySrc is cleared, the cycle_count field increments when the cycle_offset field rolls over.
22	CyTEn	Cycle-timer enable	When CyTEn is set, the cycle_offset field increments.
23	CyMrkEn	Cycle mark enable	When CyMrkEn is set, cycle marks are inserted into GRF at the end of each isochronous cycle (TSB12C01A compatible). When CyMrkEn is cleared, no cycle marks are generated.
24	IRP1En	IR port 1 enable	When IRP1En is set, the receiver accepts isochronous packets when the channel number matches the value in the IR Port1 field.
25	IRP2En	IR port 2 enable	When IRP2En is set, the receiver accepts isochronous packets when the channel number matches the value in the IR Port2 field.
26–30	Reserved	Reserved	Reserved
31	RevAEn		

3.2.4 Interrupt and Interrupt-Mask Registers

The interrupt and interrupt-mask registers work in tandem to inform the host bus interface when the state of the TSB12C01A changes. The interrupt register is at address 0Ch. The interrupt mask register is at address 10h. The interrupt mask register is read/write. Its initial value is 0000_0000h. When regRW is zero, the interrupt register (except for the Int bit) is write to clear. When regRW is set, the interrupt register (including the Int bit) is read/write. Its initial value is 1000_0000h.

The interrupt bits all work the same. For example, when a phy interrupt occurs, the PhInt bit is set. When the PhIntMask bit is set, the Int bit is set. When the IntMask is set, the $\overline{\text{INT}}$ signal is asserted. The logic for the interrupt bits is shown in Figure 3–2. Table 3–4 defines the interrupt and interrupt-mask register field descriptions.

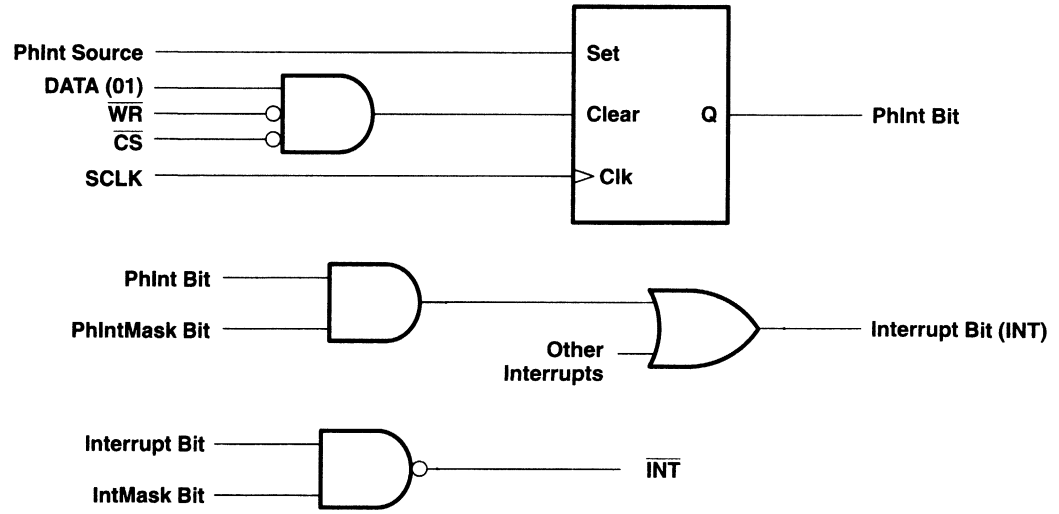


Figure 3–2. Interrupt Logic Diagram Example

Table 3–4. Interrupt- and Mask-Register Field Descriptions

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0	Int	Interrupt	Int contains the value of all interrupt and interrupt mask bits ORed together.
1	PhInt	Phy chip interrupt	When PhInt is set, the phy chip has signaled an interrupt through the Phy interface.
2	PhyRRx	Phy register information received	When PhyRRx is set, a register value has been transferred to the phy chip access register (offset 24h) from the Phy interface.
3	PhRst	Phy reset started	When PhRst is set, a phy-layer reconfiguration has started (1394 bus reset).
4	Reserved	Reserved	Reserved
5	TxRdy	Transmitter ready	When TxRdy is set, the transmitter is idle and ready.
6	RxDta	Receiver has data	When RxDta is set, the receiver has confirmed data to the GRF interface.
7	CmdRst	Command reset received	When CmdRst is set, the receiver has been sent a quadlet write request addressed to the RESET_START CSR register.
8–10	Reserved	Reserved	Reserved
11	ITStk	Transmitter is stuck (IT)	When ITStk is set, the transmitter has detected invalid data at the isochronous transmit-FIFO interface.
12	ATStk	Transmitter is stuck (AT)	When ATStk is set, the transmitter has detected invalid data at the asynchronous transmit-FIFO interface. If the first quadlet of a packet is not written to the ATF_First or ATF_First&Update, the transmitter enters a state denoted by an ATStuck interrupt. An underflow of the ATF also causes an ATStuck interrupt. If this state is entered, no asynchronous packets can be sent until the ATF is cleared via the CLR ATF control bit. Isochronous packets can be sent while in this state.
13	Reserved	Reserved	Reserved
14	SntRj	Busy acknowledge sent by receiver	When SntRj is set, the receiver is forced to send a busy acknowledge to a packet addressed to this node because the GRF overflowed.
15	HdrEr	Header error	When HdrEr is set, the receiver detected a header CRC error on an incoming packet that may have been addressed to this node.
16	TCErr	Transaction code error	When TCErr is set, the transmitter detected an invalid transaction code in the data at the transmit FIFO interface.
17–19	Reserved	Reserved	Reserved
20	CySec	Cycle second incremented	When CySec is set, the cycle-second field in the cycle-timer register incremented. This occurs approximately every second when the cycle timer is enabled.
21	CySt	Cycle started	When CySt is set, the transmitter has sent or the receiver has received a cycle-start packet.
22	CyDne	Cycle done	When CyDne is set, an arbitration gap has been detected on the bus after the transmission or reception of a cycle-start packet. This indicates that the isochronous cycle is over.
23	CyPnd	Cycle pending	When CyPnd is set, the cycle-timer offset is set to 0 (rolled over or reset) and remains set until the isochronous cycle ends.
24	CyLst	Cycle lost	When CyLst is set, the cycle timer has rolled over twice without the reception of a cycle-start packet. This occurs only when this node is not the cycle master.

Table 3–4. Interrupt- and Mask-Register Field Descriptions (Continued)

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
25	CArbFI	Cycle arbitration failed	When CArbFI is set, the arbitration to send the cycle-start packet failed.
26–30	Reserved	Reserved	Reserved
31	IArbFI	Isochronous arbitration failed	When IArbFI is set, the arbitration to send an isochronous packet failed.

3.2.5 Cycle-Timer Register

The cycle-timer register contains the seconds_count, cycle_count and cycle_offset fields of the cycle timer. The register is at address 14h and is read/write. This field is controlled by the cycle master, cycle source, and cycle timer enable bits of the control register. Its initial value is 0000_0000h.

Table 3–5. Cycle-Timer Register Field Descriptions

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0–6	seconds_count	Seconds count	1-Hz cycle-timer counter
7–19	cycle_count	Cycle count	8,000-Hz cycle-timer counter
20–31	cycle_offset	Cycle offset	24.576-MHz cycle-timer counter

3.2.6 Isochronous Receive-Port Number Register

The isochronous receive-port number register controls which isochronous channels are received by this node. This register is at address 18h. The register is read/write, and its initial value is 0000_0000h.

Table 3–6. Isochronous Receive-Port Number Register Field Descriptions

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0–7	IRPort1	Isochronous receive port 1 channel number	IRPort1 contains the channel number of the isochronous packets the receiver accepts. The receiver accepts when IRP1En is set (bits 0 and 1 are reserved).
8–15	IRPort2	Isochronous receive port 2 channel number	IRPort2 contains the channel number of the isochronous packets the receiver accepts. The receiver accepts when IRP2En is set (bits 8 and 9 are reserved).
16–31	Reserved	Reserved	Reserved

3.2.7 Diagnostic Control and Status Register

The diagnostic control and status register allows for the monitoring and control of the diagnostic features of the TSB12C01A. The register is at address 20h. The regRW and enable snoop bits are read/write. When regRW is cleared, all other bits are read only. When regRW is set, all bits are read/write. Its initial value is 0000_0000h. For a RAM test read/write, enable RAM test mode and set Adr_clr to clear the RAM internal address counter. Do the host bus read/write to location 80h; this accesses RAM starting at location 00h. With each read/write the RAM internal address counter increments by one.

Table 3–7. Diagnostic Control and Status-Register Field Descriptions

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0	ENSp	Enable Snoop	When ENSp is set, the receiver accepts all packets on the bus regardless of address or format. The receiver uses the snoop data format defined in Section 4.4, Quadlet Receive.
1	BsyFl	Busy flag	When BsyFl is set, the receiver sends an ack_busyB the next time the receiver must busy a packet. When cleared, the receiver sends an ack_busyA the next time the receiver must busy a packet.
2	ArbGp	Arbitration reset gap	When ArbGp is set, the serial bus has been idle for an arbitration reset gap.
3	FrGp	Fair gap	When FrGp is set, the serial bus has been idle for a fair-gap time (Sub-Action Gap).
4	regR/W	Register read/write access	When regR/W is set, most registers are fully read/write.
5	Adr_clr	Address clear	When Adr_clr is set, the internal RAM address counter and the Control_bit_err flag are cleared.
6	Control_bit1	Control bit for RAM test write	During RAM test mode, Control_bit1 is written into the control bit of RAM (bit 33) for RAM write transaction.
7	Control_bit_err	Control bit error flag	When Control_bit_err is set, the control bit of the RAM does not match Control_bit1 during RAM test mode.
8	RAMTest	RAM test mode	When RAMTest and regRW are set, RAM test mode is enabled.
9–31	Reserved	Reserved	Reserved

3.2.8 Phy-Chip Access Register

The phy-chip access register allows access to the registers in the attached phy chip. The most significant 16 bits send read and write requests to the phy-chip registers. The least significant 16 bits are for the phy chip to respond to a read request sent by the TSB12C01A. The phy-chip access register also allows the phy interface to send important information back to the TSB12C01A. When the phy interface sends new information to the TSB12C01A, the phy register-information-receive (PhyRRx) interrupt is set. The register is at address 24h and is read/write. Its initial value is 0000_0000h.

Table 3–8. Phy-Chip Access Register

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0	RdPhy	Read phy-chip register	When RdPhy is set, the TSB12C01A sends a read register request with address equal to phyRgAd to the Phy interface. This bit is cleared when the request is sent.
1	WrPhy	Write phy-chip register	When WrPhy is set, the TSB12C01A sends a write register request with address equal to phyRgAd to the Phy interface. This bit is cleared when the request is sent.
2–3	Reserved	Reserved	Reserved
4–7	PhyRgAd	Phy-chip-register address	PhyRgAd is the address of the phy-chip register that is to be accessed.
8–15	PhyRgData	Phy-chip-register data	PhyRgData is the data to be written to the phy-chip register indicated in PhyRgAd.
16–19	Reserved	Reserved	Reserved
20–23	PhyRxAd	Phy-chip-register-received address	PhyRxAd is the address of the register from which PhyRxData came.
24–31	PhyRxData	Phy-chip-register-received data	PhyRxData contains the data from register addressed by PhyRxAd.

3.2.9 Phy-Interface State Register

The Phy-interface state register contains the state values of the internal state machines of the Phy interface module and is used for debugging purposes. The register is at 28h and is read only. Its initial value is 0000_0000h.

Table 3–9. Phy-Interface State Register

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0–15	Reserved	Reserved	Reserved
16–19	Req_State	State of the request module	Req_State is the state value of the request module.
20–23	TI_State	State of the transmit interface module	TI_State is the state value of the transmit interface module.
24–26	RDI_State	State of the receiver data interface module	RDI_State is the state value of the receiver data interface module.
27–28	RSI_State	State of the receiver status interface module	RSI_State is the state value of the receiver status interface module.
29–31	RA_State	State of the receive acknowledge module	RA_State is the state value of the receive ack module.

3.2.10 Other State Register

The other state register contains state values of all other modules except phy interface module. It is used for debugging purposes. The register is at address 2Ch and is read only. Its initial value is 0000_0000h.

Table 3–10. Other State Register

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0–3	Reserved	Reserved	Reserved
4–6	CM_State	Cycle monitor	CM_State is the state value of the cycle monitor module.
7–9	RAC_State	RAM access control	RAC_State is the state value of the RAM access control module
10–11	ITF_Link_State	Link transmit FIFO logic	ITF_Link_State is the state value of the link transmit FIFO logic module for the ITF
12	ITF_Host_State	Host transmit FIFO logic	ITF_Host_State is the state value of the host transmit FIFO logic module for the ITF.
13–14	ATF_Link_State	Link transmit FIFO logic	ATF_Link_State is the state value of the link transmit FIFO logic module for the ATF.
15	ATF_Host_State	Host transmit FIFO logic	ATF_Host_State is the state value of the host transmit FIFO logic module for the ATF.
16–18	GRF_Host_State	Host receive FIFO logic	GRF_Host_State is the state value of the host receive FIFO logic module for the GRF.
19–21	RB_State	Receive busy	RB_State is the state value of the receive busy module.
20–22	Rcv_State	Receive	Rcv_State is the state value of the receive module.
23–31	Tx_State	Transmit	Tx_State is the state value of the transmit module.

3.2.11 Asynchronous Transmit-FIFO (ATF) Status Register

The ATF status register allows access to the registers that control or monitor the ATF. The register is at address 30h. All the FIFO flag bits are read only, and the FIFO control bits are read/write. Its initial value is 0000_0000h.

Table 3–11. ATF Status Register

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0	Full	ATF full flag	When Full is set, the FIFO is full. Writes are ignored.
1	AIF	ATF almost-full flag	When AIF is set, the FIFO can accept one more write.
2–3	Reserved	Reserved	Reserved
4	4AV	ATF-4-available flag	When 4AV is set, the FIFO has space available for at least four quadlets.
5–13	Reserved	Reserved	Reserved
14	AIE	ATF-almost-empty flag	When AIE is set, the FIFO has only one quadlet in it.
15	Empty	ATF-empty flag	When Empty is set, the FIFO is empty.
16–18	Reserved	Reserved	Reserved
19	Clr	ATF-clear control bit	When Clr is set by software/firmware, the FIFO is cleared of all entries.
20–22	Reserved	Reserved	Reserved
23–31	Size	ATF-size control bits	Size is equal to the ATF size number in quadlets.

3.2.12 ITF Status Register

The ITF status register allows access to the registers that control or monitor the ITF. The register is at address 34h. All the FIFO flag bits are read only, and the FIFO control bits are read/write. Its initial value is 0000_0000h.

Table 3–12. ITF Status Register

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0	Full	ITF full flag	When Full is set, the FIFO is full and all writes are ignored.
1	AIF	ITF almost-full flag	When AIF is set, the FIFO can accept only one more write.
2–3	Reserved	Reserved	Reserved
4	4AV	ITF-4-available flag	When 4AV is set, the FIFO has space for at least four more quadlets.
5–13	Reserved	Reserved	Reserved
14	AIE	ITF-almost-empty flag	When AIE is set, the FIFO has only one quadlet in it.
15	Empty	ITF-empty flag	When Empty is set, the FIFO is empty.
16–18	Reserved	Reserved	Reserved
19	Clr	ITF-clear control bit	When Clr is set by software/firmware, the FIFO is cleared of all entries.
20–22	Reserved	Reserved	Reserved
23–31	Size	ITF-size control bits	The size is equal to the ITF size number in quadlets.

3.2.13 GRF Status Register

The GRF status register allows access to the registers that control or monitor the GRF. The register is at address 3Ch. All the FIFO flag bits are read only, and the FIFO control bits are read/write. Its initial value is 0000_0000h.

Table 3–13. GRF Status Register

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0	Full	GRF full flag	When Full is set, the FIFO is full.
1	AIF	GRF-almost-full flag	When AIF is set, the FIFO can accept only one more write.
2–11	Reserved	Reserved	Reserved
12	4Th	GRF four there	When 4Th is set, the FIFO has at least four quadlets in it.
13	Reserved	Reserved	Reserved
14	AIE	GRF-almost-empty flag	When AIE is set, the FIFO has one quadlet in it.
15	Empty	GRF-empty flag	When Empty is set, the FIFO is empty and reads are ignored.
16	cd	GRF control bit	This is the control bit for the GRF. When cd is set, the first quadlet of a packet is being read from the GRF_Data address.
17–18	Reserved	Reserved	Reserved
19	Clr	GRF-clear control bit	When Clr is set by software/firmware, the FIFO is cleared of all entries.
20–22	Reserved	Reserved	Reserved
23–31	Size	GRF-size control bits	The size is equal to the GRF size number in quadlets.

3.3 FIFO Access

Access to all the transmit FIFOs is fundamentally the same; only the address to where the write is made changes.

3.3.1 General

The TSB12C01A controller FIFO-access address map shown in Figure 3–3 illustrates how the FIFOs are mapped. The suffix _First denotes a write to the FIFO location where the first quadlet of a packet should be written when the writer wants the packet to be held in the FIFO until a quadlet is written to an update location.

The suffix _Continue denotes a write to the FIFO location where the second through n–1 quadlets of a packet could be written.

The suffix _First&Update denotes a write to the FIFO location where the first quadlet of a packet should be written when the writer wants the packet to be transmitted as soon as possible.

The suffix _Continue&Update denotes a write to the FIFO location where the second through n quadlets of a packet could be written when the writer wants the packet to be transmitted as soon as possible. The last quadlet of a multiple quadlet packet should be written to the FIFO location with the notation _Continue&Update.

	0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
80h	ATF_First
84h	ATF_Continue
88h	ATF_First & Update
8Ch	ATF_Continue & Update
90h	ITF_First
94h	ITF_Continue
98h	ITF_First & Update
9Ch	ITF_Continue & Update
A0h	Reserved
A4h	Reserved
A8h	Reserved
ACh	Reserved
B0h	Reserved
B4h	Reserved
B8h	Reserved
BCh	Reserved
C0h	GRF Data
C4h	Reserved
C8h	Reserved
CCh	Reserved

Figure 3–3. TSB12C01A Controller-FIFO-Access Address Map

3.3.2 ATF Access

Access to the ATF is as follows:

1. Write to ATF location 80h: the data is not confirmed for transmission (first quadlet of the packet).
2. Write to ATF location 84h: the data is not confirmed for transmission (second n–1 quadlets of the packet).
3. Write to ATF location 88h: the data is confirmed for transmission (first quadlet of the packet). The read logic sees all data written to the FIFO since the last confirm (update).
4. Write to ATF location 8Ch: the data is confirmed for transmission (second n quadlets of the packet).

   If the first quadlet of a packet is not written to the ATF_First or ATF_First&Update, the transmitter enters a state denoted by an ATStuck interrupt. An underflow of the ATF also causes an ATStuck interrupt. When this state is entered, no asynchronous packets can be sent until the ATF is cleared via the CLR ATF control bit. Isochronous packets can be sent while in this state.

ATF access example:

The first quadlet of n quadlets is written to ATF location 80h. Quadlets (2 to n-1) are written to ATF location 84h. The last quadlet (nth) is written to ATF location 8Ch. If the ATFEmpty bit is true, it is set to false and the TSB12C01A requests the phy layer to arbitrate for the bus. To ensure that an ATF underflow condition does not occur, loading of the ATF in this manner is suggested.

3.3.3 ITF Access

Access to the ITF is as follows:

1. Write to ITF location 90h: the data is not confirmed for transmission (first quadlet of the packet).
2. Write to ITF location 94h: the data is not confirmed for transmission (second n–1 quadlets of the packet).
3. Write to ITF location 98h: the data is confirmed for transmission (first quadlet of the packet). The read logic sees all data written to the FIFO since the last confirm (update).
4. Write to ITF location 9Ch: the data is confirmed for transmission (second n quadlet of the packet).

   If the first quadlet of a packet is not written to the ITF_First or ITF_First&Update, the transmitter enters a state denoted by an ITStuck interrupt. An underflow of the ITF also causes an ITStuck interrupt. When this state is entered, no isochronous packets can be sent until the ITF is cleared by the CLR ITF control bit. Asynchronous packets can be sent while in this state.

ITF access example:

The first quadlet of n quadlets is written to ITF location 90h. Quadlets (2 to n-1) are written to ITF location 94h. The last quadlet (nth) is written to ITF location 9Ch. If the ITFEmpty is true, it is set to false and the TSB12C01A requests the phy layer to arbitrate for the bus. To ensure that an ITF underflow condition does not occur, loading of the ITF in this manner is suggested.

3.3.4 General-Receive-FIFO (GRF)

Access to the GRF is done with a read from the GRF, which requires a read from address C0h.

3.3.5 RAM Test Mode

The purpose of RAM test mode is to test the RAM with writes and reads. During RAM test mode, RAM, which makes up the ATF, ITF, and GRF, is accessed directly from the host bus. Different data is written to and read back from the RAM and compared with what was expected to be read back. ATF status, ITF status, and GRF status are not changed during RAM test mode, but the stored data in RAM is changed by any write transaction. To enable RAM test mode, set regRW bit and RAMTest bit of the diagnostics register. Before beginning any read or write to the RAM, the Adr_clr bit of the diagnostics register should be set to clear the internal RAM address counter. This action also clears the Adr_clr bit.

During RAM test mode, the host bus address should be 80h. The first host bus transaction (either read or write) accesses location 0 of the RAM. The second host bus transaction accesses location 1 of the RAM. The nth host bus transaction accesses location n–1 of the RAM. After each transaction, the internal RAM address counter is incremented by one.

The RAM has 512 locations with each location containing 33 bits. The most significant bit is the control bit. When it is set, that indicates the quadlet is the start of the packet. In order to set the control bit, Control-bit1 of the diagnostics register has to be set. In order to clear the control bit, Control_bit1 of the diagnostics register has to be cleared. When a write occurs, the 32 bits of data from the host bus is written to the low order 32 bits of the RAM and the value in Control-bit1 is written to the control bit. When a read occurs, the low order 32 bits of RAM are sent to the host data bus and the control bit is compared to Control_bit1. If the control bit and Control_bit1 do not match, Control_bit_err of the diagnostics register is set. This does not stop operation and another read or write can immediately be transmitted. To clear Control_bit_err, set Adr_clr of the diagnostics register, or transact another write.

4 TSB12C01A Data Formats

The data formats for transmission and reception of data are shown in the following sections. The transmit format describes the expected organization of data presented to the TSB12C01A at the host-bus interface. The receive formats describe the data format that the TSB12C01A presents to the host-bus interface.

4.1 Asynchronous Transmit (Host Bus to TSB12C01A)

Asynchronous transmit refers to the use of the asynchronous-transmit FIFO (ATF) interface. The general-receive FIFO (GRF) is shared by asynchronous data and isochronous data. There are two basic formats for data to be transmitted and received. The first is for quadlet packets, and the second is for block packets. For transmits, the FIFO address indicates the beginning, middle, and end of a packet. For receives, the data length, which is found in the header of the packet, determines the number of bytes in a block packet.

4.1.1 Quadlet Transmit

The quadlet-transmit format is shown in Figure 4–1. The first quadlet contains packet control information. The second and third quadlets contain the 64-bit, quadlet-aligned address. The fourth quadlet is data used only for write requests and read responses. For read requests and write responses, the quadlet data field is omitted.

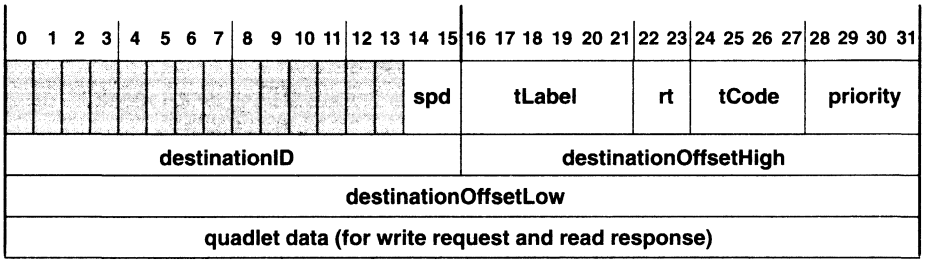


Figure 4–1. Quadlet-Transmit Format

Table 4–1. Quadlet-Transmit Format

FIELD NAME	DESCRIPTION
spd	This field indicates the speed at which this packet is to be sent. 00 = 100 Mb/s, 01 = 200 Mb/s, and 10 = 400 Mb/s, and 11 is undefined for this implementation.
tLabel	This field is the transaction label, which is a unique tag for each outstanding transaction between two nodes. This is used to pair up a response packet with its corresponding request packet.
rt	The retry code for this packet is: 00 = new, 01 = retry_X, 10 = retryA, and 11 = retryB.
tCode	tCode is the transaction code for this packet. (see Table 6–10 of IEEE-1394 standard)
priority	The priority level for this packet. For cable implementation, the value of the bits must be zero. For backplane implementation, see clause 5.4.1.3 and 5.4.2.1 of the IEEE-1394 standard.
destinationID	This is the concatenation of the 10-bit bus number and the 6-bit node number that forms the destination node address of this packet.
destination OffsetHigh, destination OffsetLow	The concatenation of these two fields addresses a quadlet in the destination nodes address space. This address must be quadlet aligned (modulo 4).
quadlet data	For write requests and read responses, this field holds the data to be transferred. For write responses and read requests, this field is not used and should not be written into the FIFO.

4.1.2 Block Transmit

The block-transmit format is shown in Figure 4–2. The first quadlet contains packet-control information. The second and third quadlets contain the 64-bit address. The first 16 bits of the fourth quadlet contains the

dataLength field. This is the number of bytes of data in the packet. The remaining 16 bits represent the extended_tCode field. (See Table 6–11 of the IEEE-1394 standard for more information on extended_tCodes.) The block data, if any, follows the extended_tCode. Block write responses are identical to the quadlet write response and use the format described in section 4.1.3, Quadlet Receive.

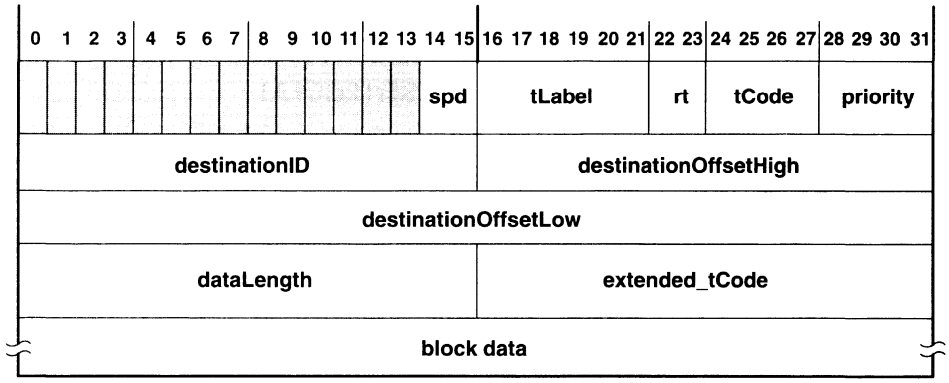


Figure 4–2. Block-Transmit Format

Table 4–2. Block-Transmit Format Functions

FIELD NAME	DESCRIPTION
spd	This field indicates the speed at which this packet is to be sent. 00 = 100 Mb/s, 01 = 200 Mb/s, and 10 = 400 Mb/s, and 11 is undefined for this implementation.
tLabel	This field is the transaction label, which is a unique tag for each outstanding transaction between two nodes. This is used to pair up a response packet with its corresponding request packet.
rt	The retry code for this packet is 00 = new, 01 = retry_X, 10 = retryA, and 11 = retryB.
tCode	tCode is the transaction code for this packet (see Table 6–10 of IEEE-1394 standard).
priority	The priority level for this packet. For cable implementation, the value of the bits must be zero. For backplane implementation, see clause 5.4.1.3 and 5.4.2.1 of the IEEE-1394 standard.
destinationID	This is the concatenation of the 10-bit bus number and the 6-bit node number that forms the node address to which this packet is being sent.
destination OffsetHigh, destination OffsetLow	The concatenation of these two fields addresses a quadlet in the destination node's address space. This address must be quadlet aligned (modulo 4). The upper four bits of the destination OffsetHigh field are used as the response code for lock-response packets and the remaining bits are reserved.
dataLength	The number of bytes of data to be transmitted in the packet.
extended_tCode	The block extended_tCode to be performed on the data in this packet. See Table 6–11 of the IEEE-1394 standard.
block data	The data to be sent. If dataLength is 0, no data should be written into the FIFO for this field. Regardless of the destination or source alignment of the data, the first byte of the block must appear in byte 0 of the first quadlet.

4.1.3 Quadlet Receive

The quadlet-receive format is shown in Figure 4–3. The first 16 bits of the first quadlet contain the destination node and bus id, and the remaining 16 bits contain packet-control information. The first 16 bits of the second quadlet contain the node and bus ID of the source, and the remaining 16 bits of the second and third quadlets contain the 48-bit, quadlet-aligned destination offset address. The fourth quadlet contains data that was used by write requests and read responses. For read requests and write responses, the quadlet data field is omitted. The last quadlet contains packet-reception status, added by the TSB12C01A.

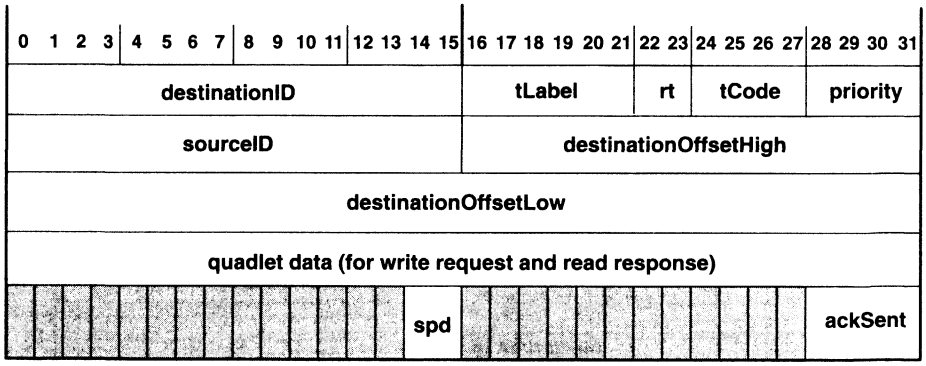


Figure 4–3. Quadlet-Receive Format

Table 4–3. Quadlet-Receive Format Functions

FIELD NAME	DESCRIPTION
destinationID	This is the concatenation of the 10-bit bus number and the 6-bit node number that forms the node address to which this packet is being sent.
tLabel	This field is the transaction label, which is a unique tag for each outstanding transaction between two nodes. This is used to pair up a response packet with its corresponding request packet.
rt	The retry code for this packet is 00 = new, 01 = retry_X, 10 = retryA, and 11 = retryB.
tCode	tCode is the transaction code for this packet. (See Table 6–10 of the IEEE-1394 standard).
priority	The priority level for this packet. For cable implementation, the value of the bits must be zero. For backplane implementation, see clause 5.4.1.3 and 5.4.2.1 of the IEEE-1394 standard.
sourceID	This is the node ID of the sender of this packet.
destination OffsetHigh, destination OffsetLow	The concatenation of these two fields addresses a quadlet in the destination nodes address space. This address must be quadlet aligned (modulo 4). (The upper four bits of the destination OffsetHigh field are used as the response code for lock-response packets, and the remaining bits are reserved.)
quadlet data	For write requests and read responses, this field holds the transferred data. For write responses and read requests, this field is not present.
spd	This field indicates the speed at which this packet was sent. 00 = 100 Mb/s, 01 = 200 Mb/s, 10 = 400 Mb/s, and 11 is undefined for this implementation.
ackSent	This field holds the acknowledge sent by the receiver for this packet. (See Table 6–13 in the draft standard.)

4.1.4 Block Receive

The block-receive format is shown in Figure 4–4. The first 16 bits of the first quadlet contain the node and bus ID of the destination node, and the last 16 bits contain packet-control information. The first 16 bits of the second quadlet contain the node and bus ID of the source node, and the last 16 bits of the second quadlet and all of the third quadlet contain the 48-bit, quadlet-aligned destination offset address. All remaining quadlets, except for the last one, contain data that is used only for write requests and read responses. For block read requests and block write responses, the data field is omitted. The last quadlet contains packet-reception status.

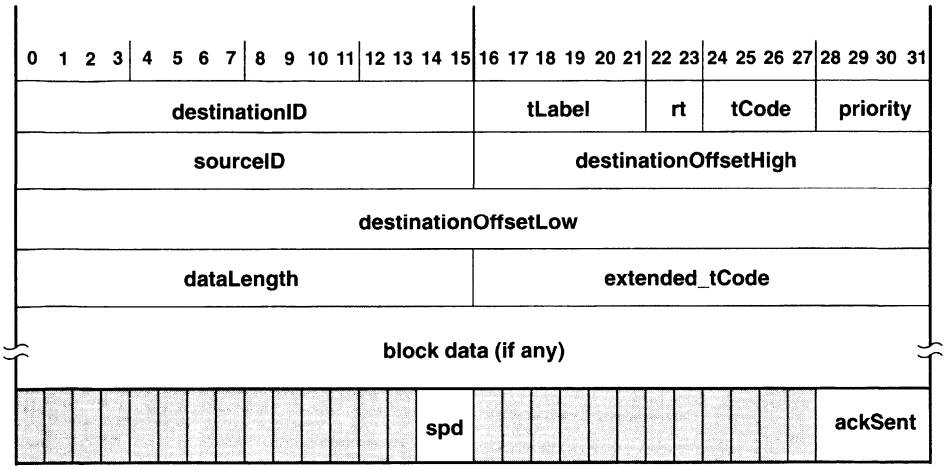


Figure 4–4. Block-Receive Format

Table 4–4. Block-Receive Format Functions

FIELD NAME	DESCRIPTION
destinationID	This is the concatenation of the 10-bit bus number and the 6-bit node number that forms the node address to which this packet is being sent.
tLabel	This field is the transaction label, which is a unique tag for each outstanding transaction between two nodes. This is used to pair up a response packet with its corresponding request packet.
rt	The retry code for this packet is 00 = new, 01 = retry_X, 10 = retryA, and 11 = retryB.
tCode	tCode is the transaction code for this packet. (See Table 6–10 of the IEEE-1394 standard).
priority	The priority level for this packet. For cable implementation, the value of the bits must be zero. For backplane implementation, see clause 5.4.1.3 and 5.4.2.1 of the IEEE-1394 standard.
sourceID	This is the node ID of the sender of this packet.
destination OffsetHigh, destination OffsetLow	The concatenation of these two fields addresses a quadlet in the destination nodes address space. This address must be quadlet aligned (modulo 4). The upper four bits of the destination OffsetHigh field are used as the response code for lock-response packets and the remaining bits are reserved.
dataLength	For write request, read responses, and locks, this field indicates the number of bytes being transferred. For read requests, this field indicates the number of bytes of data to be read. A write-response packet does not use this field. Note that the number of bytes does not include the head, only the bytes of block data.
extended_tCode	The block extended_tCode to be performed on the data in this packet. See Table 6–11 of the IEEE-1394 standard.
block data	This field contains any data being transferred for this packet. Regardless of the destination address or memory alignment, the first byte of the data appears in byte 0 of the first quadlet of this field. The last quadlet of this field is padded with zeros out to four bytes, if necessary.
spd	This field indicates the speed at which this packet was sent. 00 = 100 Mb/s, 01 = 200 Mb/s, 10 = 400 Mb/s, and 11 is undefined for this implementation.
ackSent	This field holds the acknowledge sent by the receiver for this packet.

4.2 Isochronous Transmit (Host Bus to TSB12C01A)

The format of the isochronous-transmit packet is shown in Figure 4–5. The data for each channel must be presented to the isochronous-transmit FIFO interface in this format in the order that packets are to be sent. The transmitter sends any packets available at the isochronous-transmit interface immediately following reception or transmission of the cycle-start message.

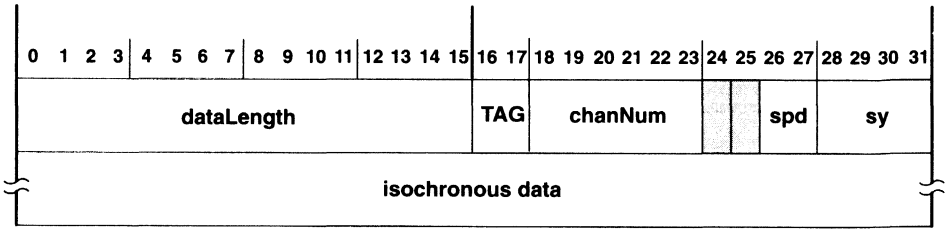


Figure 4–5. Isochronous-Transmit Format

Table 4–5. Isochronous-Transmit Functions

FIELD NAME	DESCRIPTION
dataLength	This field indicates the number of bytes in this packet
TAG	This field indicates the format of data carried by isochronous packet (00 = formatted, 01 – 11 are reserved).
chanNum	This field carries the channel number with which this data is associated
spd	This field contains the speed at which to send this packet
sy	This field carries the transaction layer-specific synchronization bits
isochronous data	This field contains the data to be sent with this packet. The first byte of data must appear in byte 0 of the first quadlet of this field. If the last quadlet does not contain four bytes of data, the unused bytes should be padded with zeros.

4.3 Isochronous Receive (TSB12C01A to Host Bus)

The format of the iscohronous-receive data is shown in Figure 4–6. The data length, which is found in the header of the packet, determines the number of bytes in an isochronous packet.

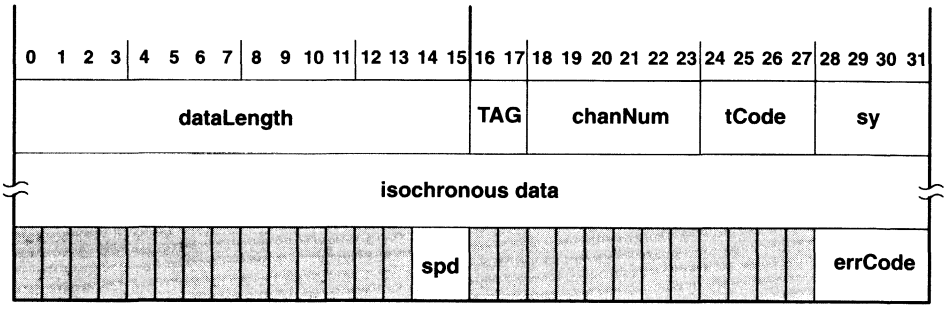


Figure 4–6. Isochronous-Receive Format

Table 4–6. Isochronous-Receive Functions

FIELD NAME	DESCRIPTION
dataLength	This field indicates the number of bytes in this packet
TAG	This field indicates the format of data carried by isochronous packet (00 = formatted, 01 – 11 are reserved).
chanNum	This field contains the channel number with which this data is associated
tCode	This field carries the transaction code for this packet. (tCode = Ah)
sy	This field carries the transaction layer-specific synchronization bits
isochronous data	This field has the data to be sent with this packet. The first byte of data must appear in byte 0 of the first quadlet of this field. The last quadlet should be padded with zeros.
spd	This field indicates the speed at which this packet was sent
errCode	This field indicates whether this packet was received correctly. The possibilities are Complete, DataErr, or CRCErr and have the same encoding as the corresponding acknowledge codes.

4.4 Snoop

The format of the snoop data is shown in Figure 4–7. The receiver module can be directed to receive any and all packets that pass by on the serial bus. In this mode, the receiver presents the data received to the receive-FIFO interface.

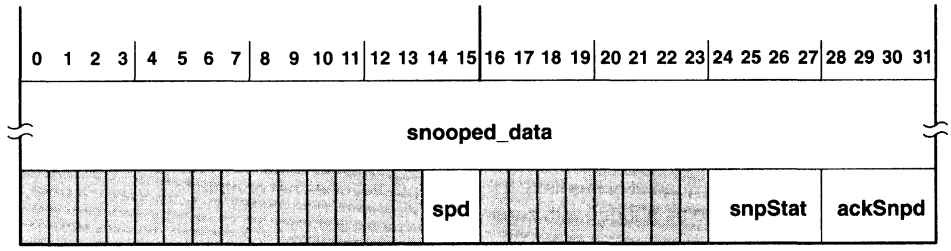


Figure 4–7. Snoop Format

Table 4–7. Snoop Functions

FIELD NAME	DESCRIPTION
snooped_data	This field contains the entire packet received or as much as could be received.
spd	This field carries the speed at which this packet was sent
snpStat	This field indicates whether the entire packet snooped was received correctly. A value equal to the complete acknowledge code indicates complete reception. A busyA or busyB acknowledge code indicates incomplete reception.
ackSnpd	This field indicates the acknowledge seen on the bus after the packet is received.

4.5 CycleMark

The format of the CycleMark data is shown in Figure 4–8. The receiver module inserts a single quadlet to mark the end of an isochronous cycle. The quadlet is inserted into the receive-FIFO.

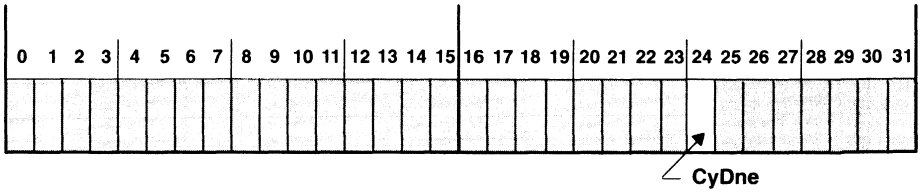


Figure 4–8. CycleMark Format

Table 4–8. CycleMark Functions

FIELD NAME	DESCRIPTION
CyDne	This field indicates the end of an isochronous cycle.

4.6 Phy Configuration

The format of the phy configuration packet is shown in Figure 4–9. The phy configuration packet transmit contains two quadlets, which are loaded into the ATF. The first quadlet is written to address 80h. The second quadlet is written to address 8Ch. The 00E0h in the first quadlet tells the TSB12C01A that this is the phy configuration packet. The Eh is then replaced with 0h before the packet is transmitted to the phy interface.

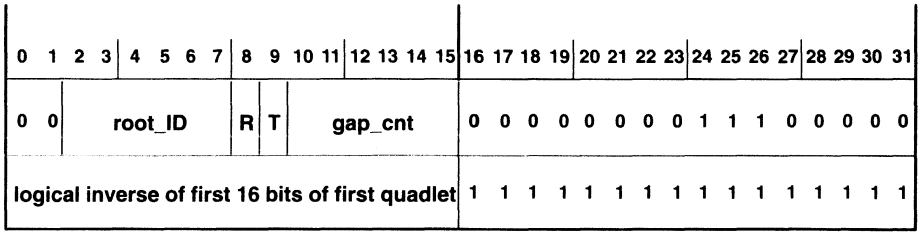


Figure 4–9. Phy Configuration Format

Table 4–9. Phy Configuration Functions

FIELD NAME	DESCRIPTION
00	This field is the phy configuration packet identifier.
root_ID	This field is the physical_ID of the node to have its force_root bit set (only meaningful when R is set).
R†	When R is set, the force-root bit of the node identified in root_ID is set and the force_root bit of all other nodes are cleared. When R is cleared, root_ID is ignored.
T†	When T is set, the PHY_CONFIGURATION.gap_count field of all the nodes is set to the value in the gap_cnt field.
gap_cnt	This field contains the new value for PHY_CONFIGURATION.gap_count for all nodes. This value goes into effect immediately upon receipt and remains valid after the next bus reset. After the second reset, gap_cnt is set to 63h unless a new Phy configuration packet is received.

† A phy configuration packet with R = 0, and T = 0 is reserved and is ignored when received.

4.7 Receive Self-ID

The format of the receive self-ID packet is shown in Figure 4–10. When RxSId (bit 1 of the control register) is set, the receive self-ID packet is stored in GRF.

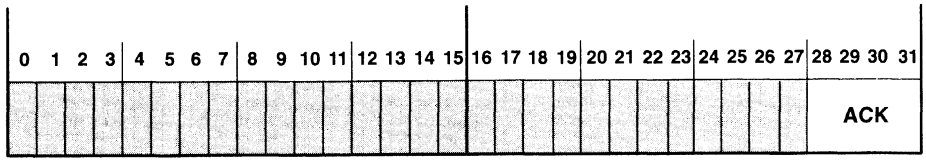


Figure 4–10. Receive Self-ID Format

Table 4–10. Receive Self-ID Functions

FIELD NAME	DESCRIPTION
ACK	When this field is set, the data in the self-ID packet is correct. When ACK is cleared, the data in the self-ID packet is incorrect.

5 Electrical Characteristics

5.1 Absolute Maximum Ratings Over Free-Air Temperature Range (Unless Otherwise Noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 6 V
Input voltage range, at any input, V_I ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) (see Note 2) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) (see Note 3) ..... ±20 mA
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Case temperature for 10 seconds, T_C ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. This applies to all inputs.
3. This applies to all outputs.

5.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Input voltage, V_I		0		V_{CC}	V
High-level input voltage, V_{IH}		2		V_{CC}	V
Low-level input voltage, V_{IL}		0		0.8	V
Clock frequency	BCLK		25	33	MHz
	SCLK		49.152		
Operating free-air temperature, T_A		0		70	°C
Virtual junction temperature range, T_J		0		115	°C

5.3 Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Free-Air Temperature (Unless Otherwise Noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −4 mA	V_{CC} − 0.8			V
V_{OL}	Low-level output voltage		I_{OL} = 4 mA			0.5	V
V_{IT+}	Positive-going input threshold voltage		Phy interface			0.7 V_{CC}	V
			All other inputs (see Note 4)			2	
V_{IT-}	Negative-going input threshold voltage		Phy interface	0.2 V_{CC}			V
			All other inputs (see Note 4)	0.8			
I_{IL}	Low-level input current		V_I = GND			−1	µA
I_{IH}	High-level input current		V_I = V_{CC}			1	µA
I_{OZ}	High-impedance-state output current		V_I = V_{CC} or GND (see Note 5)			±10	µA
I_{CC}	Supply current		No load on outputs, SCLK = 49.152 MHz BCLK = 25 MHz		150		mA
C_i	Input capacitance	Input terminals	V_{CC} = 5 V, TA = 25°C		5		pF
		Bidirectional terminals			13		
C_o	Output capacitance				8		pF

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

NOTES: 4. This applies for all inputs except SCLK, BCLK, and $\overline{\text{RESET}}$.
5. All outputs are in the high-impedance state.

5.4 Host-Interface Timing Requirements Over Operating Free-Air Temperature Range

PARAMETER		MIN	MAX	UNIT
t_{c1}	Cycle time, BCLK (see Figure 6–1)	30		ns
$t_{w1(H)}$	Pulse duration, BCLK high (see Figure 6–1)	10		ns
$t_{w1(L)}$	Pulse duration, BCLK low (see Figure 6–1)	10		ns
t_{su1}	Setup time, DATA[0:31] before BCLK↑ (see Figure 6–2)	4		ns
t_{h1}	Hold time, DATA[0:31] after BCLK↑ (see Figure 6–2)	2		ns
t_{su2}	Setup time, ADDR[0:7] before BCLK↑ (see Figures 6–2 and 6–3)	12		ns
t_{h2}	Hold time, ADDR[0:7] after BCLK↑ (see Figures 6–2 and 6–3)	2		ns
t_{su3}	Setup time, $\overline{\text{CS}}$ before BCLK↑ (see Figures 6–2 and 6–3)	12		ns
t_{h3}	Hold time, $\overline{\text{CS}}$ after BCLK↑ (see Figures 6–2 and 6–3)	2		ns
t_{su4}	Setup time, $\overline{\text{WR}}$ before BCLK↑ (see Figures 6–2 and 6–3)	12		ns
t_{h4}	Hold time, $\overline{\text{WR}}$ after BCLK↑ (see Figures 6–2 and 6–3)	2		ns

5.5 Host-Interface Switching Characteristics Over Operating Free-Air Temperature Range, C_L = 45 pF (unless otherwise noted)

	PARAMETER	MIN	MAX	UNIT
t_{d1}	Delay time, BCLK↑ to $\overline{CA}$ (see Figure 6–2)	4	16	ns
t_{d2}	Delay time, BCLK↑ to $\overline{CA}$ (see Figure 6–2)	4	16	ns
t_{d3}	Delay time, BCLK↑ to DATA[0:31] valid (see Figure 6–3)	4	24	ns
t_{d4}	Delay time, BCLK↑ to DATA[0:31] invalid (see Figure 6–3)	4	24	ns

5.6 Phy-Interface Timing Requirements Over Operating Free-Air Temperature Range

	PARAMETER	MIN	MAX	UNIT
t_{c2}	Cycle time, SCLK (see Figure 6–4)	20.24	20.45	ns
$t_{w2(H)}$	Pulse duration, SCLK high (see Figure 6–4)	9		ns
$t_{w2(L)}$	Pulse duration, SCLK low (see Figure 6–4)	9		ns
t_{su5}	Setup time, DATA[0:7] before SCLK↑ (see Figure 6–6)	6		ns
t_{h5}	Hold time, DATA[0:7] after SCLK↑ (see Figure 6–6)	0		ns
t_{su6}	Setup time, CTL[0:1] before SCLK↑ (see Figure 6–6)	6		ns
t_{h6}	Hold time, CTL[0:1] after SCLK↑ (see Figure 6–6)	0		ns

5.7 Phy-Interface Switching Characteristics Over Operating Free-Air Temperature Range, C_L = 45 pF (unless otherwise noted)

	PARAMETER	MIN	MAX	UNIT
t_{d5}	Delay time, SCLK↑ to D[0:7] valid (see Figure 6–5)	3	14	ns
t_{d6}	Delay time, SCLK↑ to D[0:7] (see Figure 6–5)	3	14	ns
t_{d7}	Delay time, SCLK↑ to D[0:7] invalid (see Figure 6–5)	3	14	ns
t_{d8}	Delay time, SCLK↑ to CTL[0:1] valid (see Figure 6–5)	3	14	ns
t_{d9}	Delay time, SCLK↑ to CTL[0:1] (see Figure 6–5)	3	14	ns
t_{d10}	Delay time, SCLK↑ to CTL[0:1] invalid (see Figure 6–5)	3	14	ns
t_{d11}	Delay time, SCLK↑ to LREQ (see Figure 6–7)	3	14	ns

5.8 Miscellaneous Timing Requirements Over Operating Free-Air Temperature Range (see Figure 6–9)

	PARAMETER	MIN	MAX	UNIT
t_{c3}	Cycle time, CYCLEIN	124.99	125.01	µs
$t_{w3(H)}$	Pulse duration, CYCLEIN high	62		µs
$t_{w3(L)}$	Pulse duration, CYCLEIN low	62		µs

5.9 Miscellaneous Signal Switching Characteristics Over Operating Free-Air Temperature Range

	PARAMETER	MIN	MAX	UNIT
t_{d12}	Delay time, SCLK↑ to $\overline{INT}$ low (see Figure 6–8)	4	18	ns
t_{d13}	Delay time, SCLK↑ to $\overline{INT}$ high (see Figure 6–8)	4	18	ns
t_{d14}	Delay time, SCLK↑ to CYCLEOUT high (see Figure 6–10)	4	16	ns
t_{d15}	Delay time, SCLK↑ to CYCLEOUT low (see Figure 6–10)	4	16	ns

6 Parameter Measurement Information

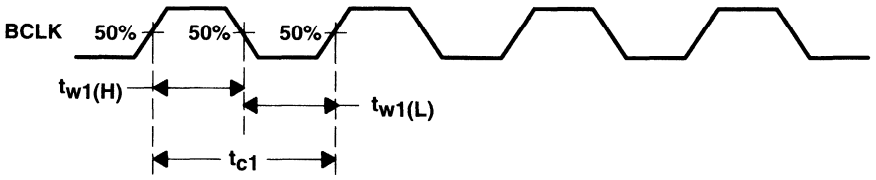
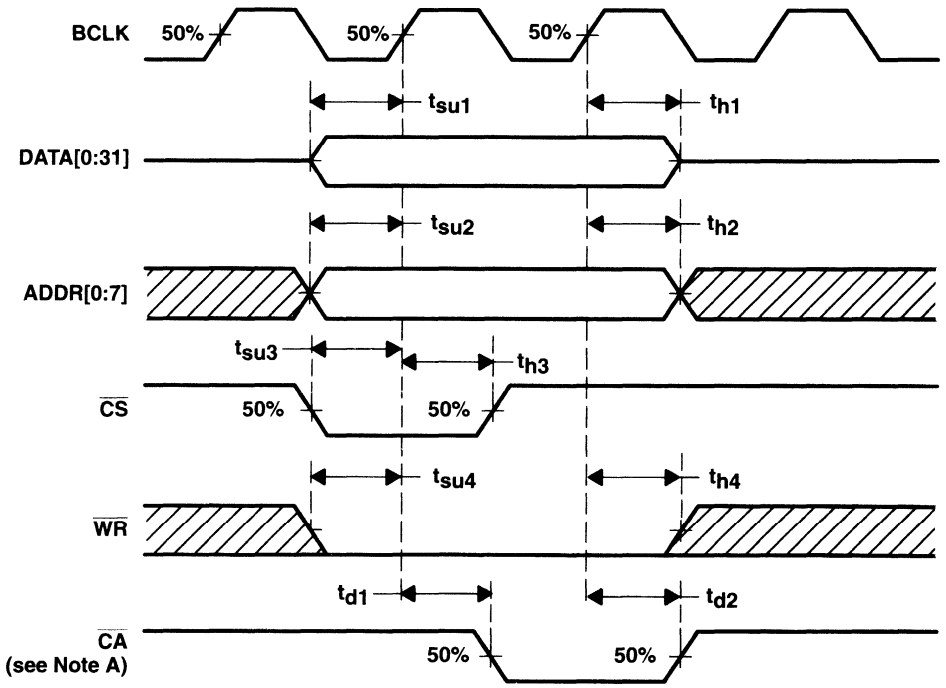
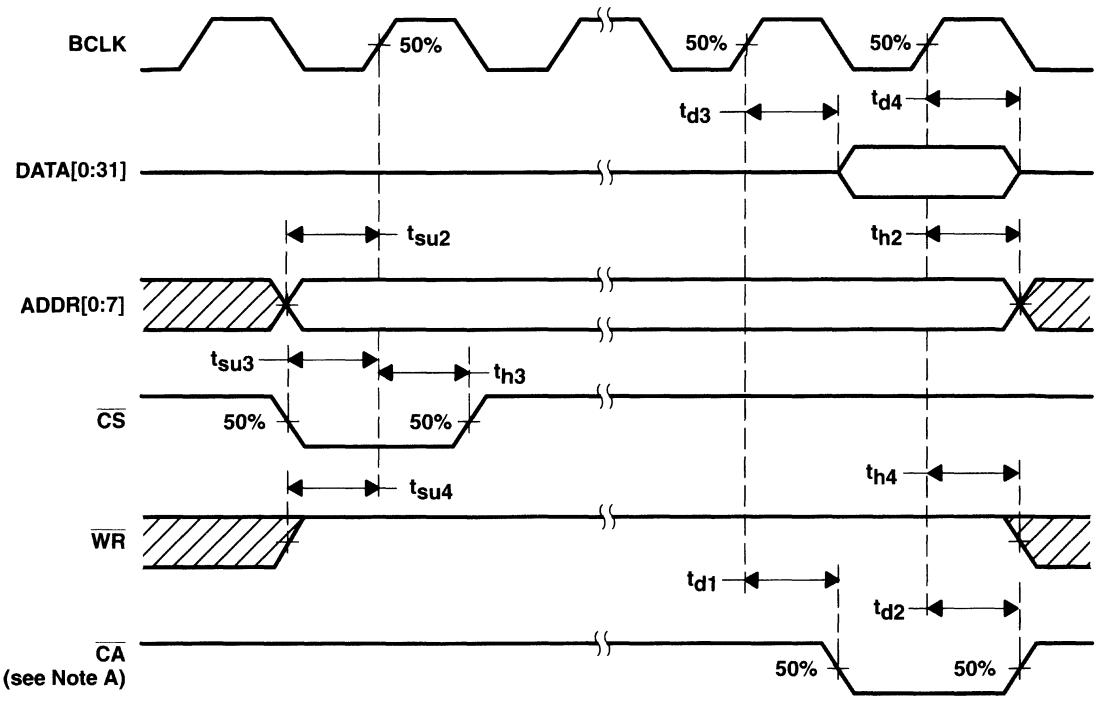


Figure 6–1. BCLK Waveform



NOTE A: When back-to-back write cycles are done, a maximum of 9 BCLK cycles may be required after the falling edge of $\overline{CS}$ before $\overline{CA}$ is asserted (low). DATA[0:31], ADDR[0:7], and $\overline{WR}$ need to remain valid until $\overline{CA}$ is asserted (low).

Figure 6–2. Host-Interface Write-Cycle Waveforms



NOTE A: When back-to-back read cycles are done, a maximum of 9 BCLK cycles may be required after the falling edge of $\overline{CS}$ and before $\overline{CA}$ is asserted (low). ADDR[0:7] and $\overline{WR}$ need to remain valid until $\overline{CA}$ is asserted (low).

Figure 6–3. Host-Interface Read-Cycle Waveforms

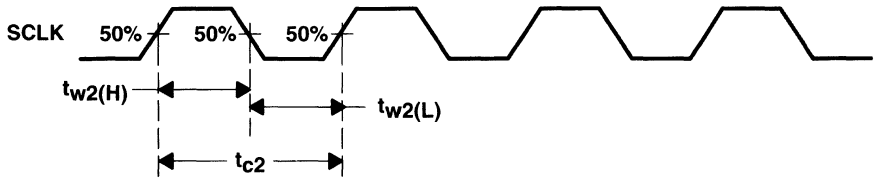


Figure 6–4. SCLK Waveform

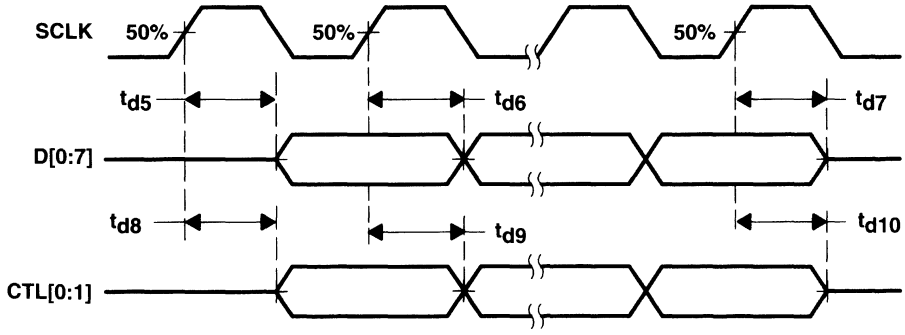


Figure 6–5. TSB12C01A-to-Phy-Layer Transfer Waveforms

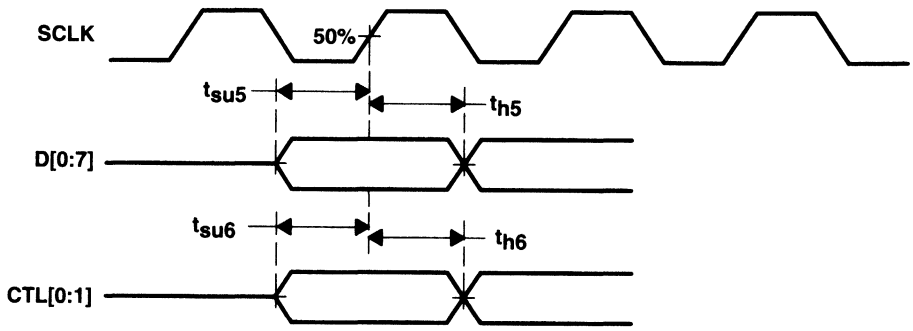


Figure 6–6. Phy-Layer-to-TSB12C01A Transfer Waveforms

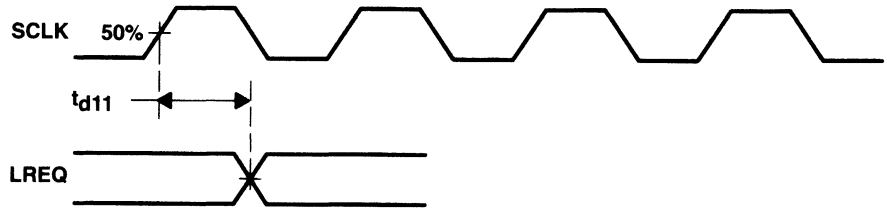


Figure 6–7. TSB12C01A-Link-Request-to-Phy-Layer Waveforms

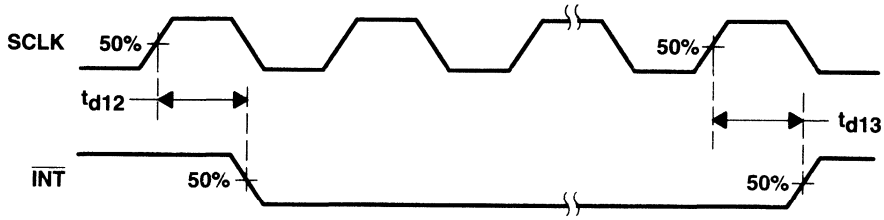


Figure 6–8. Interrupt Waveform

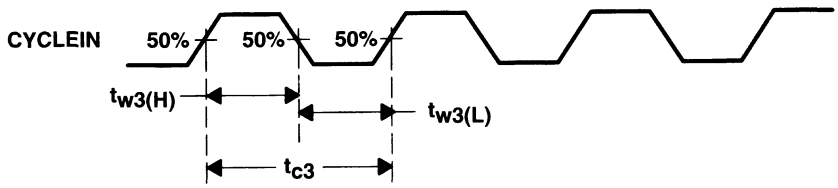


Figure 6–9. CYCLEIN Waveform

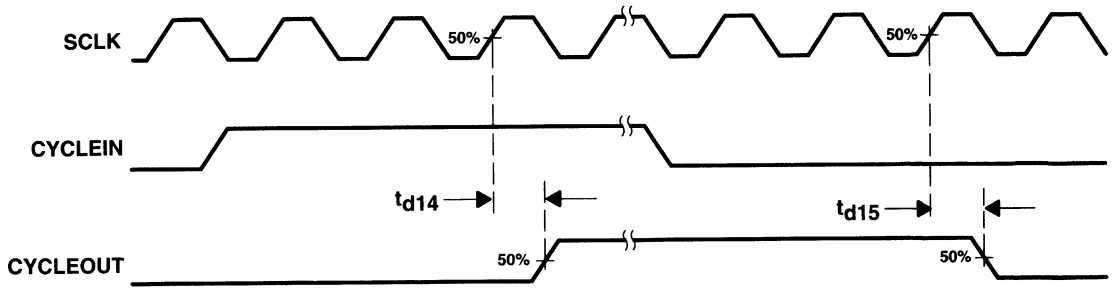


Figure 6–10. CYCLEIN and CYCLEOUT Waveforms

7 TSB12C01A to 1394 Phy Interface Specification

7.1 Introduction

This chapter provides an overview of a TSB12C01A to the phy interface. The information that follows helps guide you through the process of connecting the TSB12C01A to a 1394 physical-layer device. The part numbers referenced, the TSB11C01 and the TSB12C01A, represent the Texas Instruments implementation of the phy (TSB11C01) and link (TSB12C01A) layers of the IEEE-1394 standard.

The specific details of how the TSB11C01 device operates is not discussed in this document. Only those parts that relate to the TSB12C01A phy-link interface are mentioned.

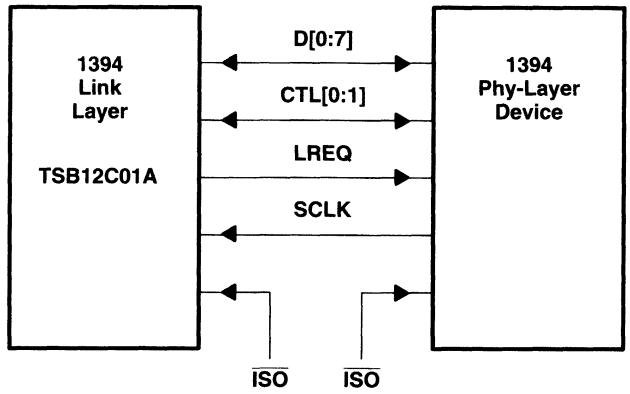
7.2 Assumptions

The TSB12C01A is capable of supporting 100 Mb/s, 200 Mb/s and 400 Mb/s phy-layer devices. For that reason, this document describes an interface to a 400-Mb/s (actually 393.216-Mb/s) device. To support lower-speed phy layers, adjust the width of the data bus by two terminals per 100 Mb/s. For example, for 100-, 200- and 400-Mb/s devices, the data bus is 2, 4, and 8 bits wide respectively. The width of the CTL bus and the clock rate between the devices, however, does not change regardless of the transmission speed that is used.

Finally, the 1394 phy layer has control of all bidirectional terminals that run between the phy layer and TSB12C01A. The TSB12C01A can drive these terminals only after it has been given permission by the phy layer. A dedicated request terminal (LREQ) is used by the TSB12C01A for any activity that you wish to initiate.

7.3 Block Diagram

The functional block diagram of the TSB12C01A to phy layer is shown in Figure 7–1.



NOTE A: See Table 2–2 for signal definition.

Figure 7–1. Functional Block Diagram of the TSB12C01A to Phy Layer

7.4 Operational Overview

The four operations that can occur in the phy-link interface are request, status, transmit, and receive. With the exception of the request operation, all actions are initiated by the phy layer.

The CTL[0:1] bus is encoded as shown in the following sections.

7.4.1 Phy Interface Has Control of the Bus

Table 7–1. Phy Interface Control of Bus Functions

CTL[0:1]	NAME	DESCRIPTION OF ACTIVITY
00	Idle	No activity is occurring (this is the default mode).
01	Status	Status information is being sent from the phy layer to the TSB12C01A.
10	Receive	An incoming packet is being sent from the phy layer to the TSB12C01A.
11	Transmit	The TSB12C01A has been given control of the bus to send an outgoing packet.

The TSB12C01A has control of the bus after receiving permission from the phy layer.

Table 7–2. TSB12C01A Control of Bus Functions

CTL[0:1]	NAME	DESCRIPTION OF ACTIVITY
00	Idle	The TSB12C01A releases the bus (transmission has been completed).
01	Hold	The TSB12C01A is holding the bus while data is being prepared for transmission, or the TSB12C01A wants to send another packet without arbitration.
10	Transmit	An outgoing packet is being sent from the TSB12C01A to phy layer.
11	Reserved	None

7.5 Request

A serial stream of information is sent across the LREQ terminal whenever the TSB12C01A needs to request the bus or access a register that is located in the phy layer. The size of the stream varies depending on whether the transfer is a bus request, a read command, or a write command. Regardless of the type of transfer, a start bit of 1 is required at the beginning of the stream and a stop bit of 0 is required at the end of the stream.

Table 7–3. Request Functions

# of BITS	NAME
7	Bus Request
9	Read Register Request
17	Write Register Request

7.5.1 LREQ Transfer

The definition of the bits in the three different types of transfers are shown in Table 7–4.

7.5.1.1 TSB12C01A Bus Request

Table 7–4. Bus-Request Functions (Length of Stream: 7 Bits)

BIT(S)	NAME	DESCRIPTION
0	Start Bit	Start bit indicates the beginning of the transfer (always set).
1–3	Request Type	Request type indicates the type of bus request (see Table 7–7 for the encoding of this field).
4–5	Request Speed	Request speed indicates the speed at which the phy interface sends the packet for this particular request (see Table 7–8 for the encoding of this field).
6	Stop Bit	Stop bit indicates the end of the transfer (always cleared).

7.5.1.2 TSB12C01A Read-Register Request

Table 7–5. Read-Register Request Functions (Length of Stream: 9 Bits)

BIT(S)	NAME	DESCRIPTION
0	Start Bit	Start bit indicates the beginning of the transfer (always set).
1–3	Request Type	Request type indicates the type of request function (see Table 7–7 for the encoding of this field).
4–7	Address	The address of the phy register to be read.
8	Stop Bit	Stop bit indicates the end of the transfer (always cleared).

7.5.1.3 TSB12C01A Write-Register Request

Table 7–6. Write-Register Request (Length of Stream: 17 Bits)

BIT(S)	NAME	DESCRIPTION
0	Start Bit	Start bit indicates the beginning of the transfer (always set).
1–3	Request Type	Request type indicates that this is a write-register request (see Table 7–7 for the encoding of this field).
4–7	Address	The address of the phy register to be written to.
8–15	Data	The data that is to be written to the specified register address.
16	Stop Bit	Stop bit indicates the end of the transfer (always cleared).

7.5.1.4 Request-Type Field for TSB12C01A Request

Table 7–7. TSB12C01A Request Functions

LREQ[1:3]	NAME	DESCRIPTION
000	TakeBus	Immediate request. Upon detection of an idle, take control of the bus immediately (no arbitration) for asynchronous packet ACK response.
001	IsoReq	Isochronous request. IsoReq arbitrates for control of the bus after isochronous gap.
010	PriReq	Priority request. PriReq arbitrates for control of the bus after a fair gap, ignore fair protocol.
011	FairReq	Fair request. FairReq arbitrates for control of the bus after a fair gap; use fair protocol.
100	RdReg	Read request. RdReg returns the specified register contents through a status transfer.
101	WrReg	Write request. WrReg writes to the specified register.
110, 111	Reserved	Reserved

7.5.1.5 Request-Speed Field for TSB12C01A Request

Table 7–8. TSB12C01A Request-Speed Functions

LREQ[4:5]	DATA RATE
00	100 Mb/s
01	200 Mb/s
10	400 Mb/s
11	Reserved

7.5.2 Bus Request

For fair or priority access, the TSB12C01A requests control of the bus at least one clock after the TSB12C01A phy interface becomes idle CTL[0:1] = 00, which indicates the physical layer is in an idle state. If the TSB12C01A senses that CTL[0:1] = 10, then it knows that its request has been lost. This is true any time during or after the TSB12C01A sends the bus request transfer. Additionally, the phy interface ignores any fair or priority requests when it asserts the receive state while the TSB12C01A is requesting the bus. The link then reissues the request one clock after the next interface idle.

The cycle master uses a normal priority request to send a cycle-start message. After receiving a cycle start, the TSB12C01A can issue an isochronous bus request. When arbitration is won, the TSB12C01A proceeds with the isochronous transfer of data. The isochronous request is cleared in the phy interface once the TSB12C01A sends another type of request or when the isochronous transfer has been completed.

The TakeBus request is issued when the TSB12C01A needs to send an acknowledgment after reception of a packet addressed to it. This request must be issued during packet reception. This is done to minimize the delay times that a phy interface would have to wait between the end of a packet reception and the transmittal of an acknowledgment. As soon as the packet ends, the phy interface immediately grants access of the bus to the TSB12C01A. The TSB12C01A sends an acknowledgment to the sender unless the header CRC of the packet turns out to be bad. In this case, the TSB12C01A releases the bus immediately; it is not allowed to send another type of packet on this grant. To ensure this, the TSB12C01A is forced to wait 160 ns after the end of the packet is received. The phy interface then gains control of the bus and the acknowledge with the CRC error sent. The bus is then released and allowed to proceed with another request.

Although highly improbable, it is conceivable that two separate nodes believe that an incoming packet is intended for them. The nodes then issue a TakeBus request before checking the CRC of the packet. Since both phys seize control of the bus at the same time, a temporary, localized collision of the bus occurs somewhere between the competing nodes. This collision would be interpreted by the other nodes on the network as being a ZZ line state, not a bus reset. As soon as the two nodes check the CRC, the mistaken node drops its request and the false line state is removed. The only side effect is the loss of the intended acknowledgment packet (this is handled by the higher layer protocol).

7.5.3 Read/Write Requests

When the TSB12C01A requests to read the specified register contents, the phy interface sends the contents of the register to the TSB12C01A through a status transfer. When an incoming packet is received while the phy interface is transferring status information to the TSB12C01A, the phy interface continues to attempt to transfer the contents of the register until it is successful.

For write requests, the phy interface loads the data field into the appropriately addressed register as soon as the transfer has been completed. The TSB12C01A is allowed to request read or write operations at any time.

See section 7.6, Status, for a more detailed description of the status transfer.

7.6 Status

A status transfer is initiated by the phy interface when it has some status information to transfer to the TSB12C01A. The transfer is initiated by asserting the following: CTL[0:1] = 01 and D[0:7] = the appropriate states; see Table 7–9 for status-request functions.

The status transfer can be interrupted by an incoming packet from another node. When this occurs, the phy interface attempts to resend the status information after the packet has been acted upon. The phy interface continues to attempt to complete the transfer until the information has been successfully transmitted.

NOTE

There must be at least one idle cycle between consecutive status transfers.

7.6.1 Status Request

The definition of the bits in the status transfer is shown in Table 7–9.

Table 7–9. Status-Request Functions (Length of Stream: 16 Bits)

BIT(s)	NAME	DESCRIPTION
0	Arbitration Reset Gap	The arbitration-reset gap bit indicates that the phy interface has detected that the bus has been idle for an arbitration reset gap time (this time is defined in the IEEE-1394 standard). This bit is used by the TSB12C01A in its busy/retry state machine.
1	Fair Gap	The fair-gap bit indicates that the phy interface has detected that the bus has been idle for a fair-gap time (this time is defined in the IEEE-1394 standard). This bit is used by the TSB12C01A to detect the completion of an isochronous cycle.
2	Bus Reset	The bus reset bit indicates that the phy interface has entered the bus reset state.
3	phy Interrupt	The phy interrupt bit indicates that the phy interface is requesting an interrupt to the host.
4–7	Address	The address bits hold the address of the phy register whose contents are transferred to the TSB12C01A.
8–15	Data	The data bits hold the data that is to be sent to the TSB12C01A.

Normally, the phy interface sends just the first four bits of data to the TSB12C01A. These bits are used by the TSB12C01A state machine. However, if the TSB12C01A initiates a read request (through a request transfer), then the phy interface sends the entire status packet to the TSB12C01A. Additionally, the phy interface sends the contents of the register to the TSB12C01A when it has some important information to pass on. Currently, the only condition where this occurs is after the self-identification process when the phy interface needs to inform the TSB12C01A of its new node address (physical ID register).

There may be times when the phy interface wants to start a second status transfer. The phy interface first has to wait at least one clock cycle with the CTL lines idle before it can begin a second transfer.

7.6.2 Transmit

When the TSB12C01A wants to transmit information, it first requests access to the bus through an LREQ signal. Once the phy interface receives this request, it arbitrates to gain control of the bus. When the phy interface wins ownership of the serial bus, it grants the bus to the TSB12C01A by asserting the transmit state on the CTL terminals for at least one SCLK cycle. The TSB12C01A takes control of the bus by asserting either hold or transmit on the CTL lines. Hold is used by the TSB12C01A to keep control of the bus when it needs some time to prepare the data for transmission. The phy interface keeps control of the bus for the TSB12C01A by asserting a data-on state on the bus. It is not necessary for the TSB12C01A to use hold when it is ready to transmit as soon as bus ownership is granted.

When the TSB12C01A is prepared to send data, it asserts transmit on the CTL lines as well as sends the first bits of the packet on the D[0:1] lines (assuming 100 Mb/s). The transmit state is held on the CTL terminals until the last bits of data have been sent. The TSB12C01A then asserts idle on the CTL lines for one clock cycle after which it releases control of the interface.

However, there are times when the TSB12C01A needs to send another packet without releasing the bus. For example, the TSB12C01A may want to send consecutive isochronous packets or it may want to attach a response to an acknowledgment. To do this, the TSB12C01A asserts hold instead of idle when the first packet of data has been completely transmitted. Hold, in this case, informs the phy interface that the TSB12C01A needs to send another packet without releasing control of the bus. The phy interface then waits a set amount of time before asserting transmit. The TSB12C01A can then proceed with the transmittal of the second packet. After all data has been transmitted and the TSB12C01A has asserted idle on the CTL terminals, the phy interface asserts its own idle state on the CTL lines. When sending multiple packets in this fashion, it is required that all data be transmitted at the same speed. This is required because the transmission speed is set during arbitration, and since the arbitration step is skipped, there is no way of informing the network of a change in speed.

7.6.3 Receive

When data is received by the phy interface from the serial bus, it transfers the data to the TSB12C01A for further processing. The phy interface asserts receive on the CTL lines and logic 1 on each D terminal. The phy interface indicates the start of the packet by placing the speed code on the data bus (see the following note). The phy interface then proceeds with the transmittal of the packet to the TSB12C01A on the D lines while still keeping the receive status on the CTL terminals. Once the packet has been completely transferred, the phy interface asserts idle on the CTL terminals that completes the receive operation.

NOTE

The speed code sent is a phy-TSB12C01A protocol and not included in the packets CRC calculation.

SPD = Speed code
D0 => Dn = Packet data

Table 7–10. Speed Code for Receive

D[0:7]	DATA RATE
00xxxxxx†	100 Mb/s
0100xxxx†	200 Mb/s
01010000	400 Mb/s
111111111	Data-on indication

† Note the x means transmitted as 0 and ignored by phy layer.

7.7 TSB12C01A to Phy Bus Timing

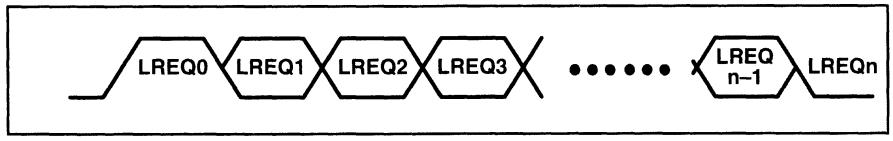


Figure 7–2. LREQ Timing

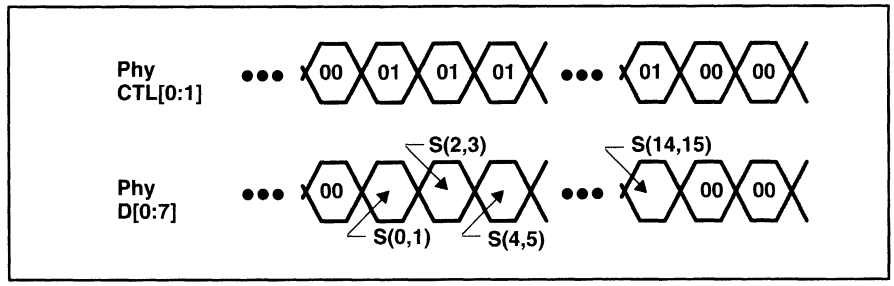
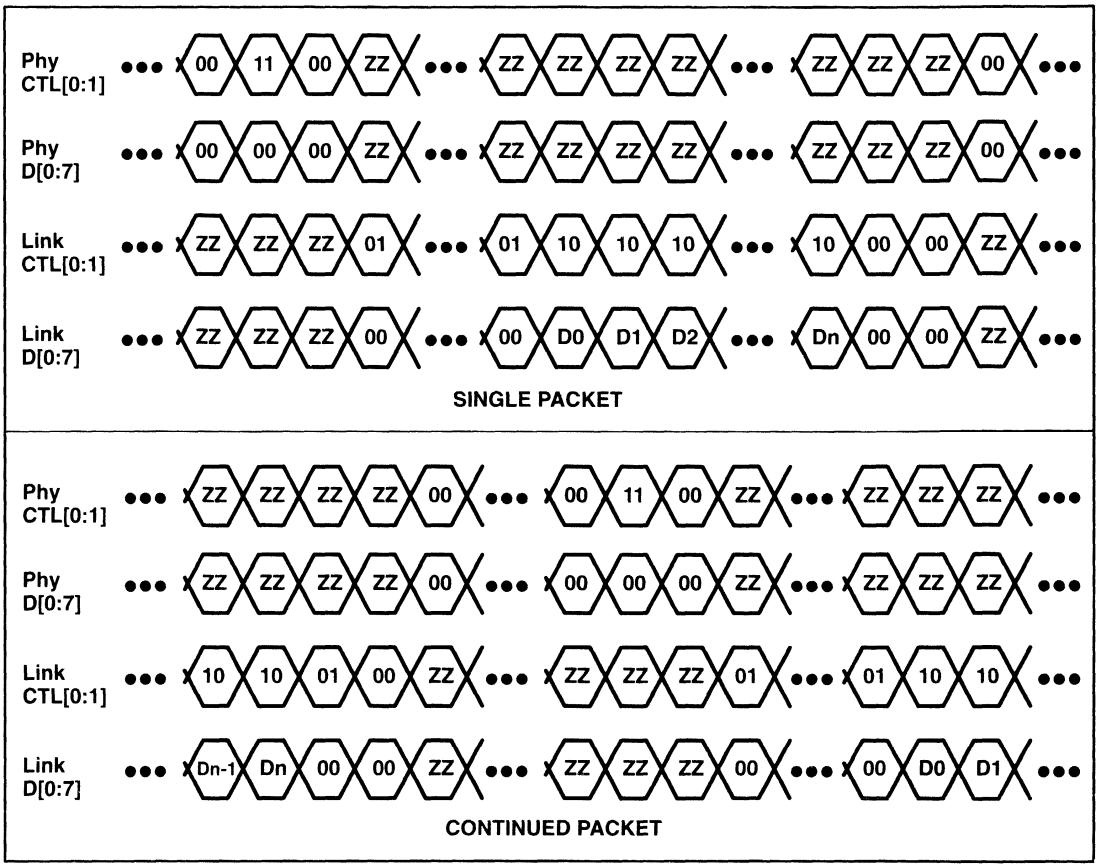


Figure 7–3. Status-Transfer Timing

NOTE A: Each cell represents one SCLK sample time.



NOTE A: ZZ = high-impedance state, D0 – Dn = packet data

Figure 7–4. Transmit Timing

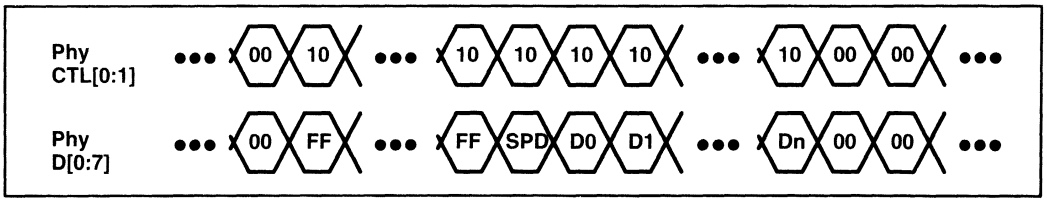
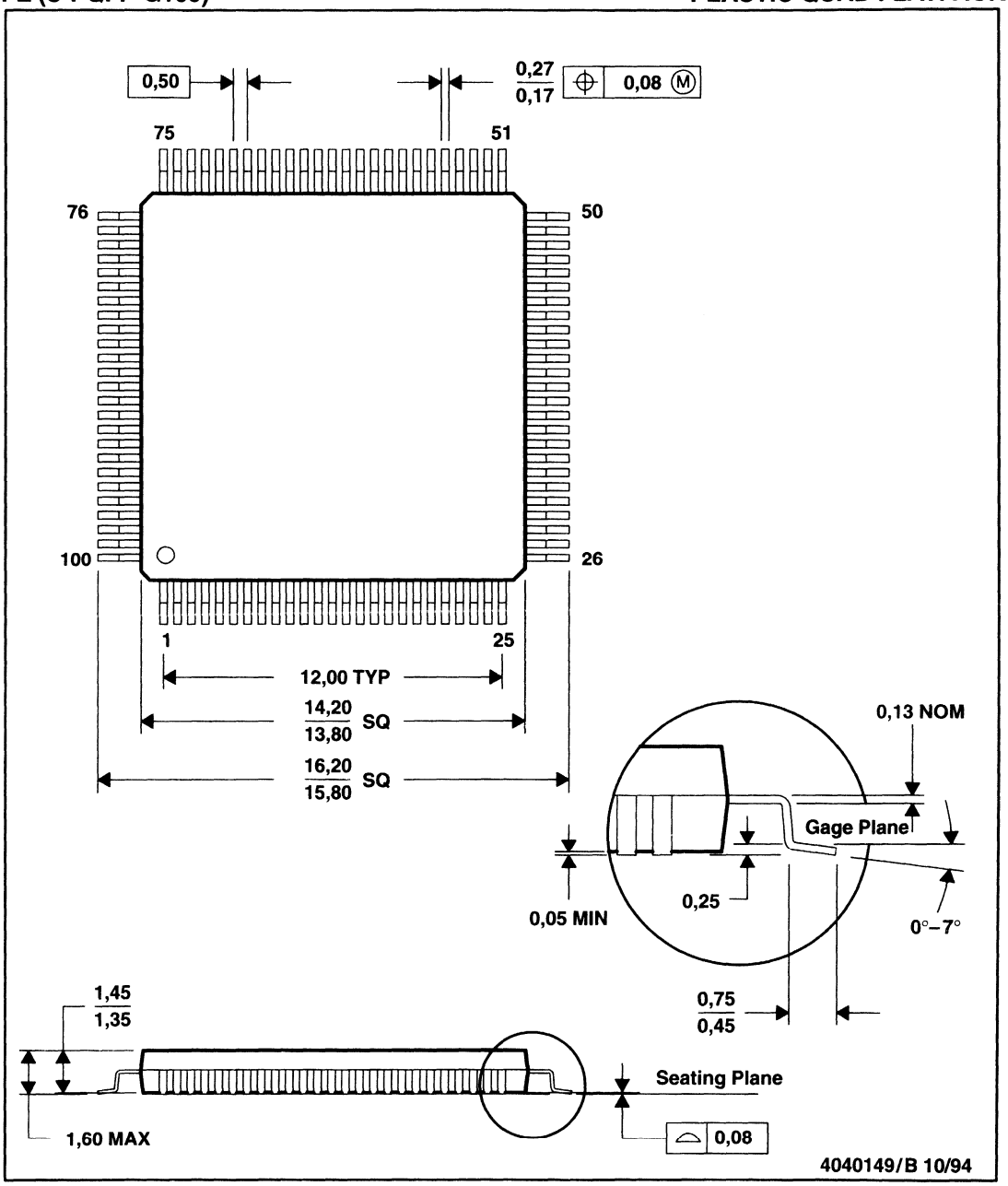


Figure 7–5. Receiver Timing

8 Mechanical Data

PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

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5 IEEE-1394 Product Previews

- **Supports Provisions of IEEE P1394 Draft Standard† for High-Performance Serial Bus‡**
- **Fully Interoperable With FireWire™ Implementation of P1394 Draft Standard**
- **Provides A Single Fully-Compliant Cable Port at 100 Megabits per Second (Mbits/s)**
- **Cable Port Monitors Line Conditions for Active Connection to a Remote Node**
- **Inactive Port Disabled to Save Power**
- **Cable-Inactivity Monitor Output and Power-Down Input Provided for Additional Power Savings (Sleep Mode)**
- **Internal Bandgap Reference Provided for Setting Stable Operating-Bias Conditions**
- **Logic Performs System Initialization and Arbitration Functions**
- **Encode and Decode Functions Included for Data-Strobe Bit-Level Encoding**
- **Incoming Data Resynchronized to Local Clock**
- **Data Interface to Link Layer Controller Provided Through Two Parallel Signal Lines at 50 Mbits/s**
- **25-MHz Crystal Oscillator and PLL Provide Transmit, Receive-Data, and Link Layer Controller Clocks at 50 MHz**
- **Digital I/Os are 5-V Tolerant**
- **Node Power Class Information Signaling for System Power Management**
- **Cable Power Presence Monitoring**
- **Cable Bias and Driver Termination Voltage Supply**
- **Single 3-V Supply Operation**
- **Separate Multiple Package Terminals Provided for Analog and Digital Supplies and Grounds**
- **High-Performance 48-Pin TQFP (PT) Package**

PRODUCT PREVIEW

description

The TSB11LV01 provides the analog transceiver functions needed to implement a single port node in a cable-based P1394 network. The cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, initialization and arbitration, and packet reception and transmission. The TSB11LV01 is designed to interface with a link layer controller such as the TSB12C01A.

The TSB11LV01 requires an external 24.576-MHz crystal, which drives an internal phase-locked loop (PLL) generating the required 98.304-MHz reference signal. The 98.304-MHz reference signal is internally divided to provide the 49.152-MHz ±100-ppm system clock signals that control transmission of the outbound-encoded strobe and data information. The 49.152-MHz clock signal is also supplied to the associated link layer controller for synchronization of the two chips and is used for resynchronization of the received data. The power down function, enabled by taking the PWRDN terminal high, stops operation of the PLL.

Data bits to be transmitted are received from the link layer controller on two parallel paths and are latched internally in the TSB11LV01 in synchronization with the 49.152-MHz system clock. These bits are combined serially, encoded, and then transmitted at 98.304-Mbits/s as the outbound data-strobe information stream. During transmit, the encoded data information is transmitted differentially on the TPBx cable pair, and the encoded strobe information is transmitted differentially on the TPAx cable pair.

† P1394 Draft 8.0v.1 dated June 16, 1995
‡ This serial bus implements technology covered by one or more patents of Apple Computer, Incorporated and INMOS, Limited.

FireWire is a trademark of Apple Computer, Incorporated.

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During packet reception the TPAx and TPBx cable port transmitters are disabled and the cable port receivers are enabled. The encoded data information is received on the TPAx cable pair, and the encoded strobe information is received on the TPBx cable pair. The received data-strobe information is decoded to recover the receive clock signal and the serial data bits. The serial data bits are split into two parallel streams, resynchronized to the local system clock, and sent to the associated link layer controller.

Both the TPA and TPB cable interfaces incorporate differential comparators to monitor the line states during initialization and arbitration. The outputs of these comparators are used by the internal logic to determine the arbitration status. In addition, the TPB channel monitors the incoming cable common-mode voltage for the presence of the remotely supplied twisted-pair bias voltage. The presence or absence of this bias voltage is an indication of cable connection status. The cable connection status signal is internally debounced in the TSB11LV01. The debounced cable connection status signal initiates a bus reset. On a cable disconnect-to-connect the debounce delay is 335 ms. On a connect-to-disconnect there is minimal debounce.

The TSB11LV01 provides a 1.86-V nominal bias voltage for driver load termination. This bias voltage, when seen through a cable by a remote receiver, senses the presence of an active connection. The value of this bias voltage has been chosen to allow interoperation between transceiver chips operating from either 5-V nominal supplies or 3-V nominal supplies. This bias-voltage source should be stabilized by using an external filter capacitor of at least 1.0 μF.

The transmitter circuitry is disabled under the following conditions: power down, cable not active, reset, or transmitter disabled. The receiver circuitry is disabled under the following conditions: power-down, cable not active, or receiver disabled. The twisted-pair bias-voltage circuitry is disabled during either a power down or reset condition. The power-down condition occurs when the PWRDN terminal is high. The cable-not-active condition occurs when the cable connection status indicates no cable is connected and is not debounced. The reset condition occurs when the $\overline{\text{RESET}}$ terminal is low. The transmitter disabled and receiver disabled conditions are determined from the internal logic.

The line drivers in the TSB11LV01 operate in the high-impedance current mode and are designed to work with external 112-Ω line-matching resistor networks. One network is provided at each end of each twisted-pair cable. Each network is composed of a pair of series-connected 56-Ω resistors. The pair of resistors that are connected to the twisted-pair TPAx terminals are also connected to the TPBIAS terminal. The pair of resistors that are connected to the twisted-pair TPBx terminals are also coupled to ground through a parallel resistance-capacitance (RC) network with recommended value of 5 kΩ and 250 pF. The values of the external resistors are designed to meet the IEEE P1394 draft standard specifications when connected in parallel with the internal receiver circuits.

An internal reference circuit (bandgap) provides stable bias voltages for the TSB11LV01 transceiver circuits. The driver output current, along with other internal operating currents, is set by an external resistor. This resistor is connected between R1 and R0 and has a value of 6.0 kΩ ±0.5%.

Four package terminals are used as inputs to set four configuration status bits in the self-identification packet. These terminals are hardwired high or low as a function of the equipment design. PC0 – PC2 are three terminals that indicate either the need for power from the cable or the ability to supply power to the cable. The fourth terminal (C/LKON) indicates that a node is a contender for configuration manager. C/LKON may also output a 6.114-MHz ±100-ppm signal, indicating reception of a link-on packet. See Table 4–29 of the IEEE P1394 draft standard for additional details.

In order to operate with power supplies as low as 2.7 V, this device is restricted to applications that do not provide cable power. See Note A in clause 4.2.2.2 of the P1394 draft standard.

When the TSB11LV01 is used in applications with a 5-V link layer controller, such as the TSB12C01A, the BIAS-5V terminal should be connected to the link layer controller 5-V supply. Otherwise connect this terminal to DV_{CC}.

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A power-down terminal (PWRDN) is provided to allow most of the TSB11LV01 circuits to be powered down to conserve energy in battery-driven applications. A cable status terminal (CNA) provides a high output when all twisted-pair cable ports are disconnected. This output is not debounced. The CNA output can determine when to power the device down. In the power-down mode all circuitry is disabled except the CNA detection circuitry.

If the power supply of the TSB11LV01 is removed while the twisted-pair cables are connected, the TSB11LV01 transmitter and receiver circuitry presents a high-impedance signal to the cable and does not load the reference voltage on the other end of the cable.

- **Link**
  - **Complies With High-Speed IEEE 1394–1995 Serial Bus Standard**
  - **Transmits and Receives Correctly Formatted 1394 Packets**
  - **Supports Isochronous Data Transfer**
  - **Performs Function of Cycle Master**
  - **Generates and Checks 32-Bit CRC**
  - **Detects Lost-Cycle Start Messages**
  - **Contains Asynchronous, Isochronous, and General-Receive FIFOs**
- **Physical-Link Interface**
  - **Interfaces Directly to the TSB21LV03M or TSB14C01M Phy Chip**
  - **Supports Speeds of 100, 200, or 400 Mb/s**
  - **Implements the Phy-Link Interface Described in Annex I of the IEEE 1394–1995 Serial Bus Standard**
- **Host Bus Interface**
  - **Provides Chip Control Via Directly Addressable Register**
  - **Is Interrupt Driven to Minimize Host Polling**
  - **Has a Generic 32-Bit Host Bus Interface**
- **General**
  - **Requires a Single 5-V ±5% Power Supply**
  - **Low-Power CMOS Technology**
  - **Packaged in a 100-Pin Ceramic Quad Flat Pack (WN) Military Package for Operation From –55°C to 125°C**

description

The TSB12C01AM is an IEEE 1394-1995 standard (from now on refered to as 1394) high-speed serial-bus link-layer controller that allows for easy integration into an I/O subsystem. The TSB12C01AM transmits and receives correctly formatted 1394 packets and generates and checks the 32-bit CRC. It is capable of being a cycle master and supports reception of isochronous data on two channels. It interfaces directly to the TSB21LV03M or the TSB14C01M physical layer chips. It also supports bus speeds of 100, 200, and 400 Mbps. The TSB12C01AM has a generic 32-bit host bus interface, which makes connection to most 32-bit host buses very simple. The TSB12C01AM has software-adjustable FIFOs for optimal FIFO size and performance characterization and allows for variable-size asynchronous-transmit FIFO (ATF), isochronous-transmit FIFO (ITF), and general-receive FIFO (GRF).

This document is not intended to serve as a tutorial on IEEE 1394-1995; users should refer to the 1394 serial bus for detailed information regarding the 1394 high-speed serial bus.

AVAILABLE OPTIONS

T_A	PACKAGE
	CERAMIC QUAD FLAT PACK (WN)
–55°C to 125°C	TSB12C01AMWNB

PRODUCT PREVIEW

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architecture

functional block diagram

The functional block architecture of the TSB12C01AM is shown in Figure 1.

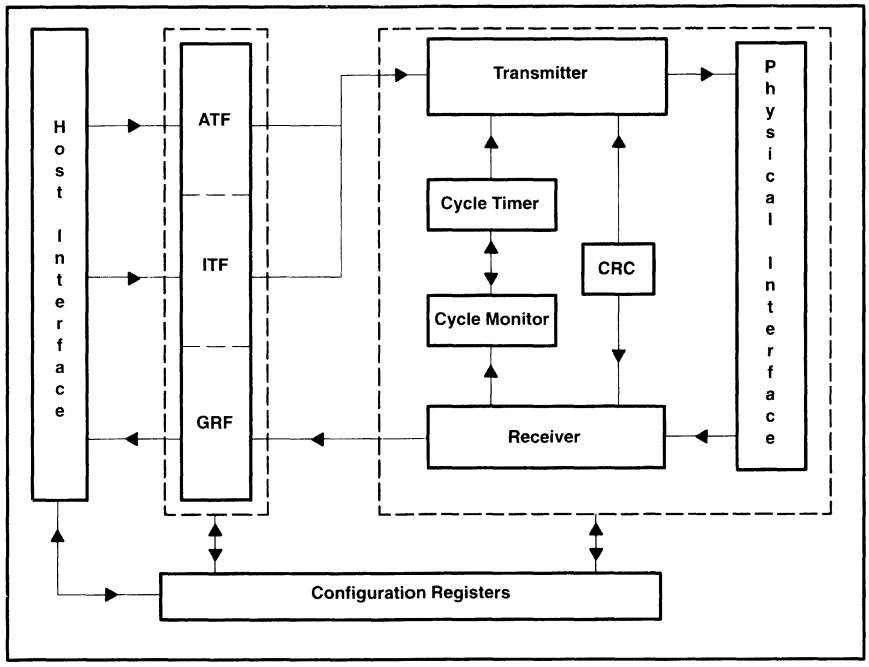

Figure 1. TSB12C01AM Functional Block Diagram

Physical Interface

The physical (phy) interface provides phy-level services to the transmitter and receiver. This includes gaining access to the serial bus, sending packets, receiving packets, and sending and receiving acknowledge packets.

The phy interface module also interfaces to the phy chip and conforms to the phy-link interface specification described in Annex J of the IEEE-1394 standard (refer to section 7 of the TSB12C01A Data Manual for more information).

Transmitter

The transmitter retrieves data from either the ATF or the ITF and creates correctly formatted serial-bus packets to be transmitted through the phy interface. When data is present at the ATF interface to the transmitter, the TSB12C01AM phy interface arbitrates for the serial bus and sends a packet. When data is present at the ITF interface to the transmitter, the TSB12C01AM arbitrates for the serial bus during the next isochronous cycle. The transmitter autonomously sends the cycle-start packets when the chip is a cycle master.

Receiver

The receiver takes incoming data from the phy interface and determines if the incoming data is addressed to this node. If the incoming packet is addressed to this node, the CRC of the packet is checked. If the header CRC is good, the header is confirmed in the GRF. For block and isochronous packets, the remainder of the packet is confirmed one quadlet at a time. The receiver places a status quadlet in the GRF after the last quadlet of the packet is confirmed in the GRF. The status quadlet contains the error code for the packet. The error code is the

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acknowledge code that is sent for that packet. For broadcast packets that do not need acknowledge packets, the error code is the acknowledge code that would have been sent. This acknowledge code tells the transaction layer whether or not the data CRC is good or bad. When the header CRC is bad, the header is flushed and the rest of the packet is ignored.

When a cycle-start message is received, it is detected and the cycle-start message data is sent to the cycle timer. The cycle-start messages are not placed in the GRF like other quadlet packets. At the end of an isochronous cycle and if the cycle mark enable (CyMrkEn) bit of the control register is set , the receiver inserts a cycle-mark packet in the GRF to indicate the end of the isochronous cycle.

Transmit and Receive FIFOs

The TSB12C01AM contains two transmit FIFOs (asynchronous and isochronous) and one receive FIFO (general receive). Each of these FIFOs are one quadlet wide and their length is software adjustable. These software-adjustable FIFOs allow customization of the size of each FIFO for individual applications. The sum of all FIFOs cannot be larger than 509 quadlets. To understand how to set the size of the FIFOs, see sections 3.2.11 through 3.2.13. The transmit FIFOs are write only from the host bus interface, and the receive FIFO is read only from the host bus interface.

An example of how to use software-adjustable FIFOs follows:

> In applications where isochronous packets are large and asynchronous packets are small, the implementer can set the ITF and GRF to a large size (200 quadlets each) and set the ATF to a smaller size (100 quadlets). Notice that the sum of all FIFOs is less than or equal to 509 quadlets.

Cycle Timer

The cycle timer is used by nodes that support isochronous data transfer. The cycle timer is a 32-bit cycle-timer register. Each node with isochronous data-transfer capability has a cycle-timer register as defined in the IEEE-1394 standard. In the TSB12C01AM, the cycle-timer register is implemented in the cycle timer and is located in IEEE-1212 initial register space at location 200h and can also be accessed through the local bus at address 14h. The low-order 12 bits of the timer are a modulo 3072 counter, which increments once every 24.576-MHz clock periods (or 40.69 ns). The next 13 higher-order bits are a count of 8, 000-Hz (or 125 µs)cycles, and the highest 7 bits count seconds.

The cycle timer contains the cycle-timer register. The cycle-timer register consists of three fields: cycle offset, cycle count, and seconds count. The cycle timer has two possible sources. First, if the cycle source (CySrc) bit in the configuration register is set, then the CYCLEIN input causes the cycle count field to increment for each positive transition of the CYCLEIN input (8 kHz) and the cycle offset resets to all zeros. CYCLEIN should only be the source when the node is cycle master. When the cycle-count field increments, CYCLEOUT is generated. The timer can also be disabled using the cycle-timer-enable bit in the control register. See section 3.2.5, Cycle-Timer Register for more information.

The second cycle-source option is when the CySrc bit is cleared. In this state, the cycle-offset field of the cycle-timer register is incremented by the internal 24.576-MHz clock. The cycle timer is updated by the reception of the cycle-start packet for the noncycle master nodes. Each time the cycle-offset field rolls over,
the cycle-count field is incremented and the CYCLEOUT signal is generated. The cycle-offset field in the cycle-start packet is used by the cycle-master node to keep all nodes in phase and running with a nominal isochronous cycle of 125 µs.

CYCLEOUT indicates to the cyclemaster node that it is time to send a cycle-start packet. And, on noncyclemaster nodes, CYCLEOUT indicates that it is time to expect a cycle-start packet. The cycle-start bit is set when the cycle-start packet is sent from the cyclemaster node or received by a noncyclemaster node.

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Cycle Monitor

The cycle monitor is only used by nodes that support isochronous data transfer. The cycle monitor observes chip activity and handles scheduling of isochronous activity. When a cycle-start message is received or sent, the cycle monitor sets the cycle-started interrupt bit. It also detects missing cycle-start packets and sets the cycle-lost interrupt bit when this occurs. When the isochronous cycle is complete, the cycle monitor sets the cycle-done-interrupt bit. The cycle monitor instructs the transmitter to send a cycle-start message when the cycle-master bit is set in the control register.

Cyclic Redundancy Check (CRC)

The CRC module generates a 32-bit CRC for error detection. This is done for both the header and data. The CRC module generates the header and data CRC for transmitting packets and checks the header and data CRC for received packets. See the IEEE-1394 standard for details on the generation of the CRC (This is the same CRC used by the IEEE802 LANs and the X3T9.5 FDDI).

Internal Registers

The internal registers control the operation of the TSB12C01AM. The register definitions are specified in section 3.

Host Bus Interface

The host bus interface allows the TSB12C01AM to be easily connected to most host processors. This host bus interface consists of a 32-bit data bus and an 8-bit address bus. The TSB12C01AM utilizes cycle-start and cycle-acknowledge handshake signals to allow the local bus clock and the 1394 clock to be asynchronous to one another. The TSB12C01AM is interrupt driven to reduce polling.

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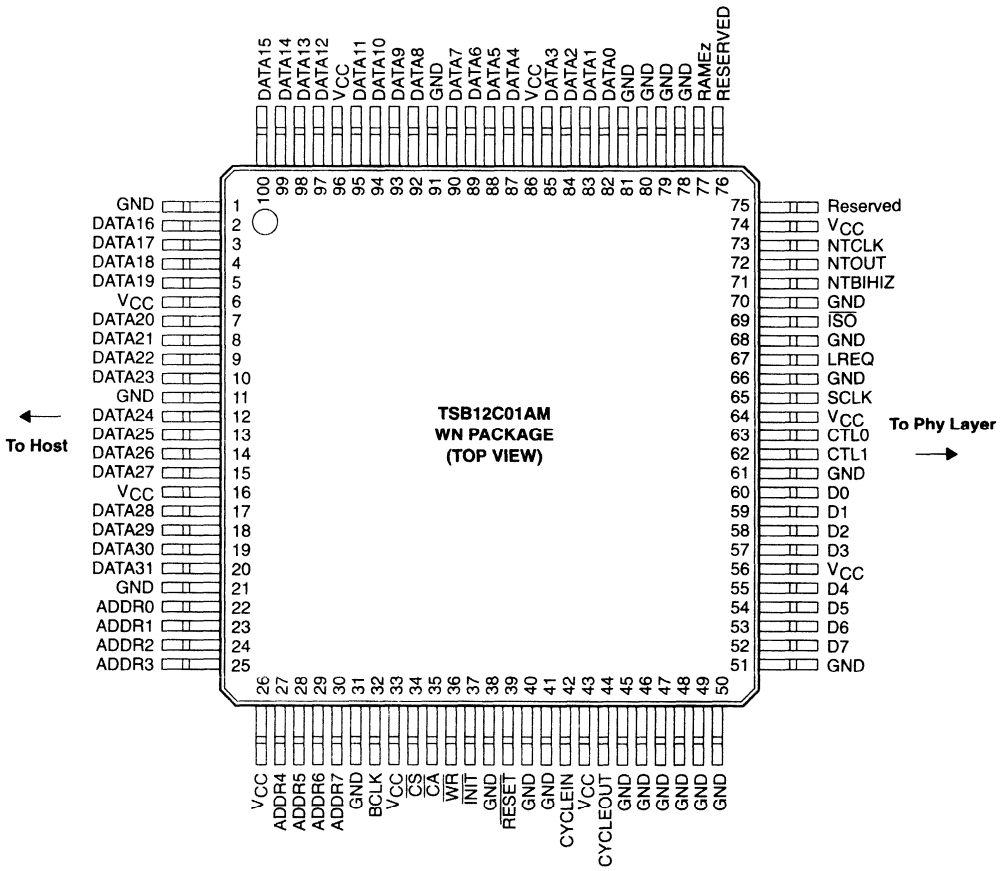
TERMINAL ASSIGNMENTS



NOTES: A. Tie reserved pins to GND.
B. Bit 0 is the most significant bit (MSB).

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terminal functions

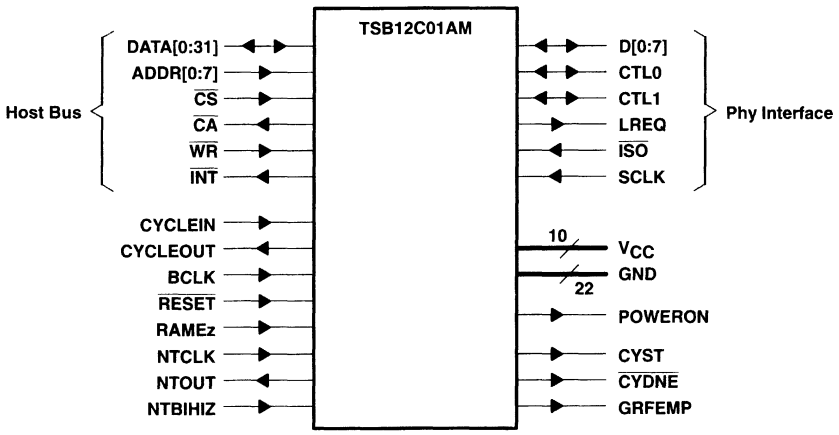

Figure 2. TSB12C01AM Terminal Functions

Table 1. Host Bus Interface Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ADDR[0:7]	22–25 27–30	I	Address 0 through address 7. Host bus address bus bits 0 through 7 that address the quadlet-aligned FIFOs and configuration registers. The two least significant address lines, 6 and 7, must be grounded.
$\overline{CA}$	35	O	Cycle acknowledge (active low). $\overline{CA}$ is a TSB12C01AM control signal to the host bus. When asserted (low), access to the configuration registers or FIFO is complete.
$\overline{CS}$	34	I	Cycle start (active low). $\overline{CS}$ is a host bus control signal to enable access to the configuration registers or FIFO.
DATA [0:31]	2–5 7–10 12–15 17–20 82–85 87–90 92–95 97–100	I/O	Data 0 through 31. DATA is a host bus data bus bits 0 through 31.
$\overline{INT}$	37	O	Interrupt (active low). When $\overline{INT}$ is asserted (low), the TSB12C01AM notifies the host bus that an interrupt has occurred.
$\overline{WR}$	36	I	Read/write enable. When $\overline{WR}$ is deasserted (high) in conjunction with $\overline{CS}$, a read from the TSB12C01AM is requested. When $\overline{WR}$ is asserted (low) in conjunction with $\overline{CS}$, a write to the TSB12C01AM is requested.

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Table 2. Phy Interface Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CTL1, CTL0	62, 63	I/O	Control 1 and control 0 of the phy-link control bus. CTL1 and CTL0 indicate the four operations that can occur in this interface (see section 7 or annex J of the IEEE-1394 standard for more information about the four operations).
D[0:7]	52–55 57–60	I/O	Data 0 through data 7 of the phy-link data bus. Data is expected on D[0:1] for 100 Mb/s packets, D[0:3] for 200 Mb/s, and D[0:7] for 400 Mb/s.
$\overline{ISO}$	69	I	Isolation barrier (active low). This $\overline{ISO}$ is asserted (low) when an isolation barrier is present.
LREQ	67	O	Link request. LREQ is a TSB12C01AM output that makes bus requests and accesses the phy layer.
POWERON	76	O	Power on indicator to phy interface. When active, POWERON has a clock output with 1/32 of the BCLK frequency and indicates to the phy interface that the TSB12C01AM is powered.

Table 3. Miscellaneous Signals Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BCLK	32	I	Bus clock. BCLK is the host bus clock used in the host-interface module of the TSB12C01AM. It is asynchronous to SCLK.
CYCLEIN	42	I	Cycle in. CYCLEIN is an optional external 8,000-Hz clock used as the cycle clock, and it should only be used when attached to the cycle-master node. It is enabled by the cycle source bit and should be tied high when not used.
CYCLEOUT	44	O	Cycle out. CYCLEOUT is the TSB12C01AM version of the cycle clock. It is based on the timer controls and received cycle-start messages.
CYDNE	49	O	Status of CyDne bit. When the RevAEn bit of the control register is set, CYDNE indicates the value of the CyDne bit of the interrupt register. When RevAEn is cleared, CYDNE is a 3-state output.
CYST	50	O	Status of CySt bit. When the RevAEn bit of the control register is set, CYST indicates the value of the CySt bit of the interrupt register. When RevAEn is cleared, CYST is a 3-state output.
GND	1, 11, 21, 31, 38, 40, 41, 45–47, 51, 61, 66, 68, 70, 78–81, 91		Ground reference
GRFEMP	48	O	Status of Empty bit. When the RevAEn bit of the control register is set, GRFEMP indicates the value of the Empty bit of the GRF status register. When RevAEn is cleared, GRFEMP is a 3-state output.
RAMEz	77	I	RAM 3-state enable. When RAMEz is deasserted (low), FIFOs are enabled. When RAMEz is asserted, the FIFOs are 3-state outputs. (This is a manufacturing test-mode condition and should be grounded under normal operating conditions.)
NTBIHIZ	71	I	NAND-tree bidirectional 3-state output. When NTBIHIZ is deasserted (low), the bidirectional I/Os operate in a normal state. When NTBIHZ is asserted (high), the bidirectional I/Os are in the 3-state output mode. (This is a manufacturing test-mode condition and should be grounded under normal operating conditions.)
NTCLK	73	I	NAND clock input. The NAND-tree clock is used for V_{IH} and V_{IL} manufacturing tests. (This input should be grounded under normal operating conditions.)
NTOUT	72	O	NAND-tree output. This output should remain open under normal operating conditions.
$\overline{RESET}$	39	I	Reset (active low). $\overline{RESET}$ is the asynchronous reset to the TSB12C01AM.
SCLK	65	I	System clock. SCLK is a 49.152-MHz clock from the phy, that generates the 24.576-MHz clock.
V_{CC}	6, 16, 26, 33, 43, 56, 64, 74, 86, 96		5-V ±5% power supplies

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absolute maximum ratings over free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 6 V
Input voltage range, at any input, V_I ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 2) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 3) ..... ±20 mA
Storage temperature range ..... −65°C to 150°C
Case temperature for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. Applies to all inputs
3. Applies to all outputs

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Input voltage, V_I		0		V_{CC}	V
High-level input voltage, V_{IH}		2		V_{CC}	V
Low-level input voltage, V_{IL}		0		0.8	V
Clock frequency	BCLK		25	33	MHz
	SCLK		49.152		
Operating free-air temperature, T_A		−55		125	°C

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -4$ mA	$V_{CC} - 0.8$			V
V_{OL}	Low-level output voltage	$I_{OL} = 4$ mA			0.5	V
V_{IT+}	Positive-going input threshold voltage	Phy interface			$0.7\ V_{CC}$	V
		All other inputs (see Note 4)			2	
V_{IT-}	Negative-going input threshold voltage	Phy interface	$0.2\ V_{CC}$			V
		All other inputs (see Note 4)	0.8			
I_{IL}	Low-level input current	$V_I = GND$			−1	µA
I_{IH}	High-level input current	$V_I = V_{CC}$			1	µA
I_{OZ}	High-impedance-state output current	$V_I = V_{CC}$ or GND (see Note 5)			±10	µA
I_{CC}	Supply current	No load on outputs, SCLK = 49.152 MHz BCLK = 25 MHz		150		mA

† All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.

NOTES: 4. This applies for all inputs except SCLK, BCLK, and $\overline{RESET}$.
5. All outputs are in the high-impedance state.

host-interface timing requirements over operating free-air temperature range

PARAMETER		MIN	MAX	UNIT
t_{c1}	Cycle time, BCLK (see Figure 3)	30		ns
$t_{w1(H)}$	Pulse duration, BCLK high (see Figure 3)	10		ns
$t_{w1(L)}$	Pulse duration, BCLK low (see Figure 3)	10		ns
t_{su1}	Setup time, DATA[0:31] before BCLK↑ (see Figure 4)	4		ns
t_{h1}	Hold time, DATA[0:31] after BCLK↑ (see Figure 4)	2		ns
t_{su2}	Setup time, ADDR[0:7] before BCLK↑ (see Figures 4 and 5)	12		ns
t_{h2}	Hold time, ADDR[0:7] after BCLK↑ (see Figures 4 and 5)	2		ns
t_{su3}	Setup time, $\overline{CS}$ before BCLK↑ (see Figures 4 and 5)	12		ns
t_{h3}	Hold time, $\overline{CS}$ after BCLK↑ (see Figures 4 and 5)	2		ns
t_{su4}	Setup time, $\overline{WR}$ before BCLK↑ (see Figures 4 and 5)	12		ns
t_{h4}	Hold time, $\overline{WR}$ after BCLK↑ (see Figures 4 and 5)	2		ns

host-interface switching characteristics over operating free-air temperature range, C_L = 45 pF (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
t_{d1}	Delay time, BCLK↑ to $\overline{CA}$ (see Figure 4)	4	16	ns
t_{d2}	Delay time, BCLK↑ to $\overline{CA}$ (see Figure 4)	4	16	ns
t_{d3}	Delay time, BCLK↑ to DATA[0:31] valid (see Figure 5)	4	24	ns
t_{d4}	Delay time, BCLK↑ to DATA[0:31] invalid (see Figure 5)	4	24	ns

phy-interface timing requirements over operating free-air temperature range

PARAMETER		MIN	MAX	UNIT
t_{c2}	Cycle time, SCLK (see Figure 6)	20.24	20.45	ns
$t_{w2(H)}$	Pulse duration, SCLK high (see Figure 6)	9		ns

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$t_{w2(L)}$	Pulse duration, SCLK low (see Figure 6)	9	ns
t_{su5}	Setup time, DATA[0:7] before SCLK↑ (see Figure 8)	6	ns
t_{h5}	Hold time, DATA[0:7] after SCLK↑ (see Figure 8)	0	ns
t_{su6}	Setup time, CTL[0:1] before SCLK↑ (see Figure 8)	6	ns
t_{h6}	Hold time, CTL[0:1] after SCLK↑ (see Figure 8)	0	ns

phy-interface switching characteristics over operating free-air temperature range, C_L = 45 pF (unless otherwise noted)

	PARAMETER	MIN	MAX	UNIT
t_{d5}	Delay time, SCLK↑ to D[0:7] valid (see Figure 7)	3	14	ns
t_{d6}	Delay time, SCLK↑ to D[0:7] (see Figure 7)	3	14	ns
t_{d7}	Delay time, SCLK↑ to D[0:7] invalid (see Figure 7)	3	14	ns
t_{d8}	Delay time, SCLK↑ to CTL[0:1] valid (see Figure 7)	3	14	ns
t_{d9}	Delay time, SCLK↑ to CTL[0:1] (see Figure 7)	3	14	ns
t_{d10}	Delay time, SCLK↑ to CTL[0:1] invalid (see Figure 7)	3	14	ns
t_{d11}	Delay time, SCLK↑ to LREQ (see Figure 9)	3	14	ns

miscellaneous timing requirements over operating free-air temperature range (see Figure 11)

	PARAMETER	MIN	MAX	UNIT
t_{c3}	Cycle time, CYCLEIN	124.99	125.01	µs
$t_{w3(H)}$	Pulse duration, CYCLEIN high	62		µs
$t_{w3(L)}$	Pulse duration, CYCLEIN low	62		µs

miscellaneous signal switching characteristics over operating free-air temperature range

	PARAMETER	MIN	MAX	UNIT
t_{d12}	Delay time, SCLK↑ to $\overline{INT}$ low (see Figure 10)	4	18	ns
t_{d13}	Delay time, SCLK↑ to $\overline{INT}$ high (see Figure 10)	4	18	ns
t_{d14}	Delay time, SCLK↑ to CYCLEOUT high (see Figure 12)	4	16	ns
t_{d15}	Delay time, SCLK↑ to CYCLEOUT low (see Figure 12)	4	16	ns

PARAMETER MEASUREMENT INFORMATION

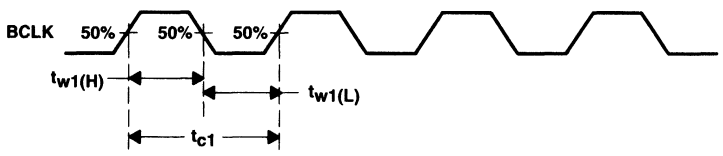
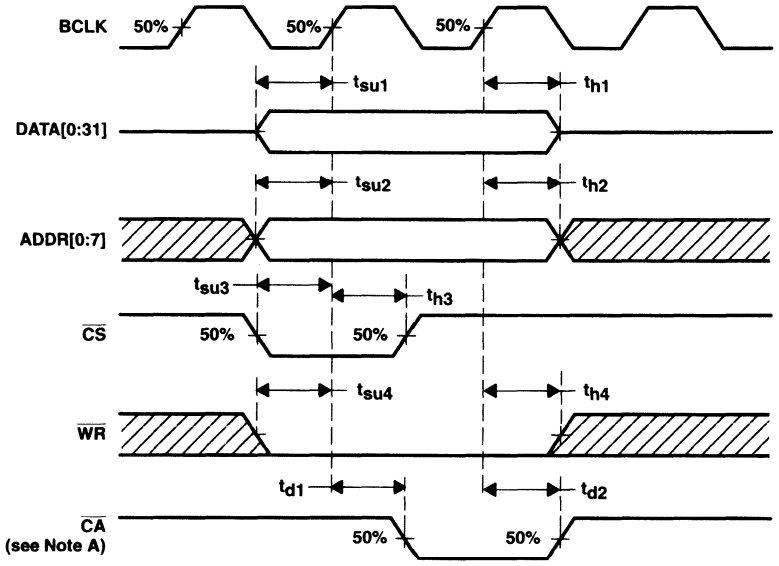


Figure 3. BCLK Waveform



NOTE A: When back-to-back write cycles are done, a maximum of 9 BCLK cycles may be required after the falling edge of $\overline{CS}$ before $\overline{CA}$ is asserted (low). DATA[0:31], ADDR[0:7], and $\overline{WR}$ need to remain valid until $\overline{CA}$ is asserted (low).

Figure 4. Host-Interface Write-Cycle Waveforms

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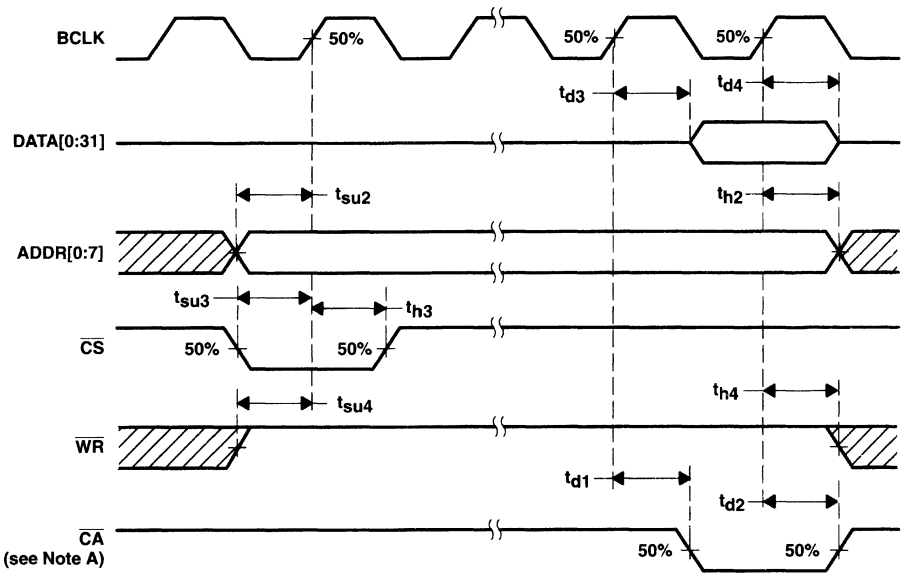

NOTE A: When back-to-back read cycles are done, a maximum of 9 BCLK cycles may be required after the falling edge of $\overline{CS}$ and before $\overline{CA}$ is asserted (low). ADDR[0:7] and $\overline{WR}$ need to remain valid until $\overline{CA}$ is asserted (low).

Figure 5. Host-Interface Read-Cycle Waveforms

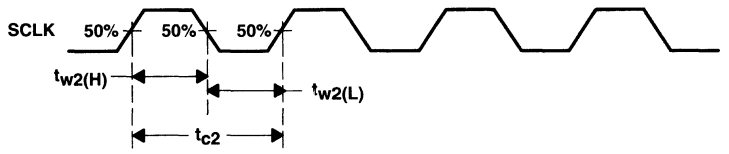

Figure 6. SCLK Waveform

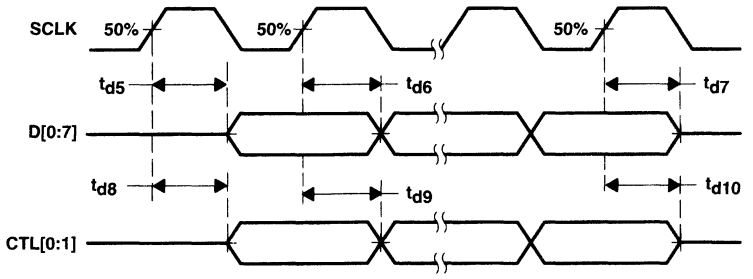

Figure 7. TSB12C01AM-to-Phy-Layer Transfer Waveforms

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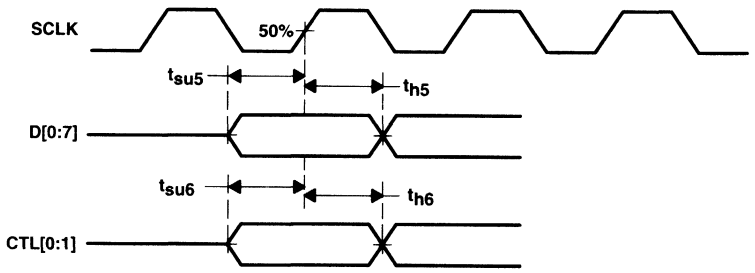

Figure 8. Phy-Layer-to-TSB12C01AM Transfer Waveforms

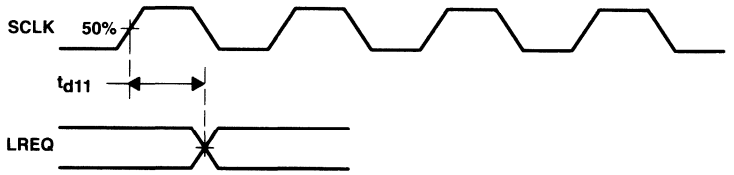

Figure 9. TSB12C01AM-Link-Request-to-Phy-Layer Waveforms

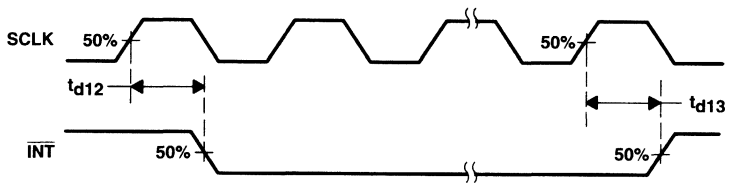

Figure 10. Interrupt Waveform

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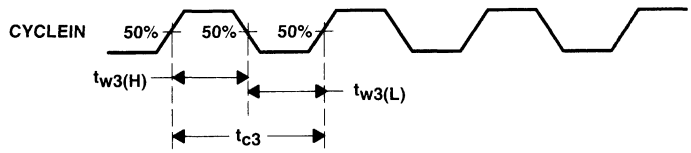

Figure 11. CYCLEIN Waveform

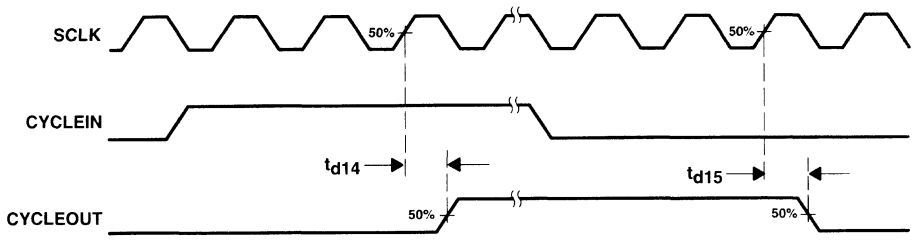

Figure 12. CYCLEIN and CYCLEOUT Waveforms

PRODUCT PREVIEW

- **Supports Provisions of IEEE P1394 Draft Standard† for High-Performance Serial Bus‡**
- **Fully Interoperable With FireWire™ Implementation of P1394**
- **Provides A Backplane Environment That Supports 100 Megabits per Second (Mbits/s)**
- **Logic Performs System Initialization and Arbitration Functions**
- **Encode and Decode Functions Included for Data-Strobe Bit-Level Encoding**
- **Incoming Data Resynchronized to Local Clock**
- **Separate Transmitter and Receiver for Greater Flexibility**
- **Data Interface to Link Layer Controller Provided Through Two Parallel Signal Lines at 50 Mbits/s**
- **100-MHz Oscillator Provides Transmit, Receive-Data, and Link Layer Controller Clocks at 50 MHz**
- **Single 5-V Supply Operation**
- **High-Performance 64-Pin TQFP (PM) Package**

description

The TSB14C01 provides the transceiver functions needed to implement a single port node in a backplane-based P1394 network. The TSB14C01 provides two terminals for transmitting, two terminals for receiving, and two terminals to externally control the drivers for data and strobe. The TSB14C01 is not designed to drive the backplane directly, this function must be provided externally. The TSB14C01 is designed to interface with a link layer controller such as the TSB12C01A.

The TSB14C01 requires an external 98.304-MHz reference oscillator input. The 98.304-MHz reference signal is internally divided to provide the 49.152-MHz ±100-ppm system clock signals used to control transmission of the outbound encoded strobe and data information. The 49.152-MHz clock signal is also supplied to the associated link layer controller for synchronization of the two chips and is used for resynchronization of the received data.

Data bits to be transmitted are received from the link layer controller on two parallel paths and are latched internally in the TSB14C01 in synchronization with the 49.152-MHz system clock. These bits are combined serially, encoded, and then transmitted at 98.304-Mbits/s as the outbound data-strobe information stream. During transmission, the encoded data information is transmitted on TDATA, and the encoded strobe information is transmitted on TSTRB.

During packet reception the encoded information is received on RDATA and strobe information on RSTRB. The received data-strobe information is decoded to recover the receive clock signal and the serial data bits. The serial data bits are split into two parallel streams, resynchronized to the local system clock, and sent to the associated link layer controller.

The TSB14C01 is a 5-V only device and provides CMOS-level outputs.

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† P1394 Draft 8.0v.1 dated June 16, 1995
‡ This serial bus implements technology covered by one or more patents of Apple Computer, Incorporated and INMOS, Limited.

FireWire is a trademark of Apple Computer, Incorporated.

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TSB14C01M
IEEE 1394-1995 BACKPLANE TRANSCEIVER/ARBITER FOR 5-VOLT SUPPLY OPERATION

SGLS090– MARCH 1996

- **Supports Provisions of IEEE 1394-1995 Standard† for High-Performance Serial Bus‡**
- **Fully Interoperable With FireWire™ Implementation of IEEE 1394-1995**
- **Provides A Backplane Environment That Supports 100 Megabits per Second (Mbits/s)**
- **Logic Performs System Initialization and Arbitration Functions**
- **Encode and Decode Functions Included for Data-Strobe Bit-Level Encoding**
- **Incoming Data Resynchronized to Local Clock**
- **Separate Transmitter and Receiver for Greater Flexibility**
- **Data Interface to Link Layer Controller Provided Through Two Parallel Signal Lines at 50 Mbits/s**
- **100-MHz Oscillator Provides Transmit, Receive-Data, and Link Layer Controller Clocks at 50 MHz**
- **Single 5-V Supply Operation**
- **High-Performance 64-Pin TQFP (PM) Package**
- **68-Pin Ceramic Quad Flat Package (HV) For Military Operation (–55°C to 125°C)**

description

The TSB14C01 provides the transceiver functions needed to implement a single port node in a backplane-based IEEE1394-1995 (from now on refered to as 1394) network. The TSB14C01 provides two terminals for transmitting, two terminals for receiving, and two terminals to externally control the drivers for data and strobe. The TSB14C01 is not designed to drive the backplane directly, this function must be provided externally. The TSB14C01 is designed to interface with a link layer controller such as the TSB12C01A.

The TSB14C01 requires an external 98.304-MHz reference oscillator input. The 98.304-MHz reference signal is internally divided to provide the 49.152-MHz ±100-ppm system clock signals used to control transmission of the outbound encoded strobe and data information. The 49.152-MHz clock signal is also supplied to the associated link layer controller for synchronization of the two chips and is used for resynchronization of the received data.

Data bits to be transmitted are received from the link layer controller on two parallel paths and are latched internally in the TSB14C01 in synchronization with the 49.152-MHz system clock. These bits are combined serially, encoded, and then transmitted at 98.304-Mbits/s as the outbound data-strobe information stream. During transmission, the encoded data information is transmitted on TDATA, and the encoded strobe information is transmitted on TSTRB.

During packet reception the encoded information is received on RDATA and strobe information on RSTRB. The received data-strobe information is decoded to recover the receive clock signal and the serial data bits. The serial data bits are split into two parallel streams, resynchronized to the local system clock, and sent to the associated link layer controller.

The TSB14C01 is a 5-V only device and provides CMOS-level outputs.

PRODUCT PREVIEW

† This serial bus implements technology covered by one or more patents of Apple Computer, Incorporated and INMOS, Limited.
FireWire is a trademark of Apple Computer, Incorporated.

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SLLS230 – MARCH 1996

- **Supports Provisions of IEEE P1394 Draft Standard† for High-Performance Serial Bus‡**
- **Fully Interoperable with FireWire™ Implementation of P1394 Draft Standard**
- **Provides Three Fully-Compliant Cable Ports at 100/200 Megabits per Second (Mbits/s)**
- **Cable Ports Monitor Line Conditions for Active Connection to Remote Node**
- **Device Power-Down Feature to Conserve Energy in Battery Powered Applications**
- **Inactive Ports Disabled to Save Power**
- **Logic Performs System Initialization and Arbitration Functions**
- **Encode and Decode Functions Included for Data-Strobe Bit-Level Encoding**
- **Incoming Data Resynchronized to Local Clock**
- **Single 3.3-V Supply Operation**
- **Interface to Link Layer Controller Supports Optional Electrical Isolation**
- **Data Interface to Link Layer Controller Provided Through Two/Four Parallel Lines at 50 Mbits/s**
- **25-MHz Crystal Oscillator and PLL Provide Transmit, Receive Data at 50/100 MHz, and Link Layer Controller Clock at 50 MHz**
- **Interoperable with Link Controllers Using 5-V Supplies**
- **Node Power Class Information Signaling for System Power Management**
- **Cable Power Presence Monitoring**
- **Cable Bias and Driver Termination Voltage Supply**
- **Separate Multiple Package Terminals Provided for Analog and Digital Supplies and Grounds**
- **Interoperable with Transceivers Using 5-V Supplies**
- **High-Performance 64-Pin TQFP (PM) Package**

PRODUCT PREVIEW

description

The TSB21LV03 provides the analog transceiver functions needed to implement a 3-port node in a cable-based P1394 network. Each cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, initialization and arbitration, and packet reception and transmission. The TSB21LV03 is designed to interface with a link layer controller such as the TSB12C01A.

The TSB21LV03 requires an external 24.576-MHz crystal. The crystal oscillator drives an internal phase-locked loop (PLL), which generates the required 196.608-MHz reference signal. The 196.608-MHz reference signal is internally divided to provide the 49.152-/98.304-MHz clock signals that control transmission of the outbound encoded strobe and data information. The 49.152-MHz clock signal is also supplied to the associated link layer controller for synchronization of the two chips, and is used for resynchronization of the received data. The power-down function, enabled by taking the PD terminal high, stops operation of the PLL.

The TSB21LV03 supports an optional isolation barrier between itself and its link layer controller. When the $\overline{\text{ISO}}$ terminal is tied high, the link interface outputs behave normally. When this terminal is tied low, internal differentiating logic is enabled and the outputs become short pulses that can be coupled through a capacitor or transformer. See the P1394/Draft 8.0v1 Annex J for further details.

† P1394 Draft 8.0v.1 dated June 16, 1995

‡ This serial bus implements technology covered by one or more patents of Apple Computer, Incorporated and INMOS, Limited.

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description (continued)

Data bits to be transmitted are received from the link layer controller on two/four parallel paths, and are latched internally in the TSB21LV03 in synchronization with the 49.152-MHz system clock. These bit pairs are combined serially, encoded, and then transmitted at 98.304/196.608 megabits per second (Mbits/s) as the outbound data-strobe information stream. During transmission, the encoded data information is transmitted differentially on the TPBx cable pair(s), and the encoded strobe information is transmitted differentially on the TPAx cable pair(s).

During packet reception the TPAx and TPBx receiving cable port transmitters are disabled, and the cable port receivers are enabled. The encoded data information is received on the TPAx cable pair, and the encoded strobe information is received on the TPBx cable pair. The received data-strobe information is decoded to recover the receive clock signal and the serial data bits. The serial data bits are split into two/four parallel streams, resynchronized to the local system clock, and sent to the associated link layer controller. The received data is also transmitted (repeated) out of the other active cable ports.

Both the TPA and TPB cable interfaces incorporate differential comparators to monitor the line states during initialization and arbitration. The outputs of these comparators are used by the internal logic to determine the arbitration status. The TPA channel monitors the incoming cable common-mode voltage value. The value of this common-mode voltage is used during arbitration to set the speed of the next packet transmission. In addition, the TPB channel monitors the incoming cable common-mode voltage for the presence of the remotely supplied twisted-pair bias voltage. The presence or absence of this common-mode voltage is an indication of cable connection status. The cable connection status signal is internally debounced in the TSB21LV03 on a cable disconnect-to-connect. The debounced cable connection status signal initiates a bus reset. On a cable disconnect-to-connect the debounce delay is 335 ms. There is no delay on a cable connect-to-disconnect.

The TSB21LV03 provides a 1.86-V nominal bias voltage for driver load termination. This bias voltage, when seen through a cable by a remote receiver, senses the presence of an active connection. The value of this bias voltage has been chosen to allow interoperability between transceiver chips operating from either 5-V nominal supplies or 3-V nominal supplies. This bias-voltage source should be stabilized by using an external filter capacitor of approximately 1.0 μF.

The transmitter circuitry is disabled under the following conditions: power-down, cable not active, reset, or transmitter disabled. The receiver circuitry is disabled under the following conditions: power-down, cable not active, receiver disabled. The twisted-pair bias-voltage circuitry is disabled either with a power-down or a reset condition. The power-down condition occurs when the PD terminal is high. The cable-not-active condition occurs when the cable connection status indicates no cable is connected and is not debounced. The reset condition occurs when the $\overline{\text{RESET}}$ terminal is low. The transmitter disabled and receiver disabled conditions are determined from the internal logic.

The line drivers in the TSB21LV03 operate in a high-impedance current mode and are designed to work with external 112-Ω line-matching resistor networks. One network is provided at each end of each twisted-pair cable. Each network is composed of a pair of series-connected 56-Ω resistors. The pair of resistors that are connected to the twisted-pair TPAx terminals are also connected to the TPBIAS terminal. The pair of resistors that are connected to the twisted-pair TPBx terminals are also coupled to ground through a parallel resistance-capacitance (RC) network with recommended values of 5 kΩ and 250 pF. The values of the external resistors are designed to meet the draft standard specifications when connected in parallel with the internal receiver circuits.

The driver output current, along with other internal operating currents, is set by an external resistor. This resistor is connected between the R0 and R1 terminals and has a value of 6.3 kΩ, ±0.5%.

PRODUCT PREVIEW

description (continued)

Four package terminals are used as inputs to set four configuration status bits in the self-identification packet. These terminals are hardwired high or low as a function of the equipment design. PC0 – PC2 are the three terminals that indicate either the need for power from the cable or the ability to supply power to the cable. The fourth terminal (CMC/LKON) indicates whether a node is a contender for configuration manager. See Table 4–29 of the IEEE P1394 draft standard for additional details.

A power-down terminal (PD) is provided to allow most of the TSB21LV03 circuits to be powered down to conserve energy in battery-driven applications. A cable status terminal (CNA) provides a high output when all twisted-pair cable ports are disconnected. This output is not debounced. The CNA output can determine when to power the TSB21LV03 down. In the power-down mode all circuitry is disabled except the CNA detection circuitry. It should be noted that while the device is powered down it does not act in a repeater mode.

If the TSB21LV03 is being used in a single port application and the power supply of the TSB21LV03 is removed while the twisted-pair cables are connected, the TSB21LV03 transmitter and receiver circuitry presents a high-impedance signal to the cable and does not load the reference voltage on the other end of the cable.

TSB21LV03M
IEEE 1394-1995 TRIPLE-CABLE TRANSCEIVER/ARBITER

SGLS089 – MARCH 1996

- Supports Provisions of IEEE 1394-1995 Standard for High-Performance Serial Bus†
- Fully Interoperable With FireWire™ Implementation of IEEE 1394-1995
- Provides Three Fully Compliant Cable Ports at 100/200 Mbits Per Second (Mbits/s)
- Cable Ports Monitor Line Conditions for Active Connection to Remote Node
- Device Power Down Feature to Conserve Power in Battery-Driven Applications
- Inactive Ports Disabled to Save Power
- Logic Performs System Initialization and Arbitration Functions
- Encode and Decode Functions Included for Data-Strobe Bit-Level Encoding
- Incoming Data Resynchronized to Local Clock
- Single 3.3-V Supply Operation
- Interface to Link Layer Controller Supports Optional Electrical Isolation
- Data Interface to Link-Layer Controller Provided Through 2/4 Parallel Lines at 50 Mbits/s
- 25-MHz Crystal Oscillator and PLL Provide Transmit, Receive Data at 50/100 MHz, and Link-Layer Controller Clocks at 50 MHz
- Interoperable With Link Controllers and Transceivers Using 5-V Supplies
- Node Power Class Information Signaling for System Power Management
- Cable Power Presence Monitoring
- Cable Bias and Driver Termination Voltage Supply
- Separate Multiple Package Terminals Provided for Analog and Digital Supplies and Grounds
- Interoperable with Transceivers Using 5-V Supplies
- 68-Pin Ceramic Quad Flatpack (HV) and Characterized For Operation Over the Full Military Temperature Range of −55°C to 125°C

PRODUCT PREVIEW

description

The TSB21LV03M provides the analog transceiver functions needed to implement a three-port node in a cable-based IEEE 1394-1995 (from now on referred to as 1394) network. Each cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions needed for determining connection status, for initialization and arbitration, and for packet reception and transmission. The TSB21LV03M is designed to interface with a link-layer controller, such as the TSB12C01AM.

The TSB21LV03M requires an external 24.576-MHz crystal. The crystal oscillator drives an internal phase-locked loop (PLL), which generates the required 196.608-MHz reference signal. The 196.608-MHz reference signal is internally divided to provide the 49.152/98.304-MHz signals used to control transmission of the outbound encoded strobe and data information. The 49.152-MHz clock signal is also supplied to the associated link-layer controller for synchronization of the two chips and is used for resynchronization of the received data.

The TSB21LV03M supports an optional isolation barrier between itself and its link-layer controller. When $\overline{ISO}$ is tied high, the link interface outputs behave normally. When ISO is tied low, internal differentiating logic is enabled and the outputs become short pulses that can be coupled through a capacitor or transformer. See the IEEE 1394-1995 Standard Annex J for more information.

† Implements technology covered by one or more patents of Apple Computer, Incorporated and INMOS, Limited.
FireWire is a trademark of Apple Computer, Incorporated.

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description (continued)

Data bits to be transmitted are received from the link-layer controller on two/four parallel paths and are latched internally in the TSB21LV03M in synchronization with the 49.152-MHz system clock. These bit pairs are combined serially, encoded, and transmitted at 98.304/196.608 Mb/s as the outbound data-strobe information stream. During transmit, the encoded data information is transmitted differentially on the TPB cable pair(s) and the encoded strobe information is transmitted differentially on the TPA cable pair(s).

During packet reception, the TPA and TPB transmitters of the receiving cable port are disabled and the receivers for that port are enabled. The encoded data information is received on the TPA cable pair, and the encoded strobe information is received on the TPB cable pair. The received data-strobe information is decoded to recover the receive clock signal and the serial data bits. The serial data bits are split into two/four parallel streams, resynchronized to the local system clock and sent to the associated link-layer controller. The received data is also transmitted (repeated) out of the other active cable ports.

Both the TPA and TPB cable interfaces incorporate differential comparators to monitor the line states during initialization and arbitration. The outputs of these comparators are used by the internal logic to determine the arbitration status. The TPA channel monitors the incoming cable common-mode voltage value, which is used during arbitration to set the speed of the next packet transmission. The TPB channel monitors the incoming cable common-mode voltage. The presence or absence of this bias voltage is used as an indication of cable-connection status.

PRODUCT PREVIEW

The TSB21LV03M provides a 1.86-V nominal bias voltage for driver load termination. This bias voltage, when seen through a cable by a remote receiver, is used to sense the presence of an active connection. The value of this bias voltage has been chosen to allow interoperability between transceiver chips operating from either 5-V nominal supplies or 3-V nominal supplies. This bias voltage source should be stabilized by using an external filter capacitor of approximately 1 μF.

The line drivers in the TSB21LV03M operate in the high-impedance current mode and are designed to work with external 112-Ω line matching resistor networks. One network is provided at each end of each twisted-pair cable. Each network is composed of a pair of series-connected 56-Ω resistors. The midpoint of the pair of resistors that is directly connected to the twisted-pair A-package terminals is connected to the TPBIAS voltage terminal. The midpoint of the pair of resistors that is directly connected to the twisted-pair B-package terminals is coupled to ground through a parallel RC network with recommended values of 5 kΩ and 250 pF. The values of the external resistors are designed to meet the IEEE 1394-1995 standard specifications when connected in parallel with the internal receiver circuits.

The driver output current, along with other internal operating currents, is set by an external resistor. This resistor is connected between R0 and R1 and has a value of 6.3 kΩ ±0.5%.

Two terminals are used to set up various test conditions used in manufacturing. Terminals TESTM1 and TESTM2 should be connected to V_{CC} for normal operation.

Four terminals are used as inputs to set four configuration status bits in the self-identification packet. These terminals are hardwired high or low as a function of the equipment design. PC[0:2] are three terminals used to indicate either the need for power from the cable or the ability to supply power to the cable. The fourth pin, CMC/LKON, is used to indicate if a node is a contender for configuration manager. See Table 4–29 of the IEEE 1394-1995 standard for additional details.

A power down terminal (PD) is provided to allow most of the TSB21LV03M circuits to be powered down to conserve energy in battery-driven applications. A cable-status terminal (CNA) provides a high output when all twisted-pair cable ports are disconnected. This output can be used to determine when to power the device down. In the power-down mode, all circuitry is disabled except the CNA-detection circuitry. Note that when the device is powered down, it will not act in a repeater mode.

If the TSB21LV03 is being used in a single port application and the power supply of the TSB21LV03 is removed while the twisted-pair cables are connected, the TSB21LV03 transmitter and receiver circuitry presents a high-impedance signal to the cable and does not load the reference voltage on the other end of the cable.

The TSB21LV03M is characterized for operation from –55°C to 125°C.

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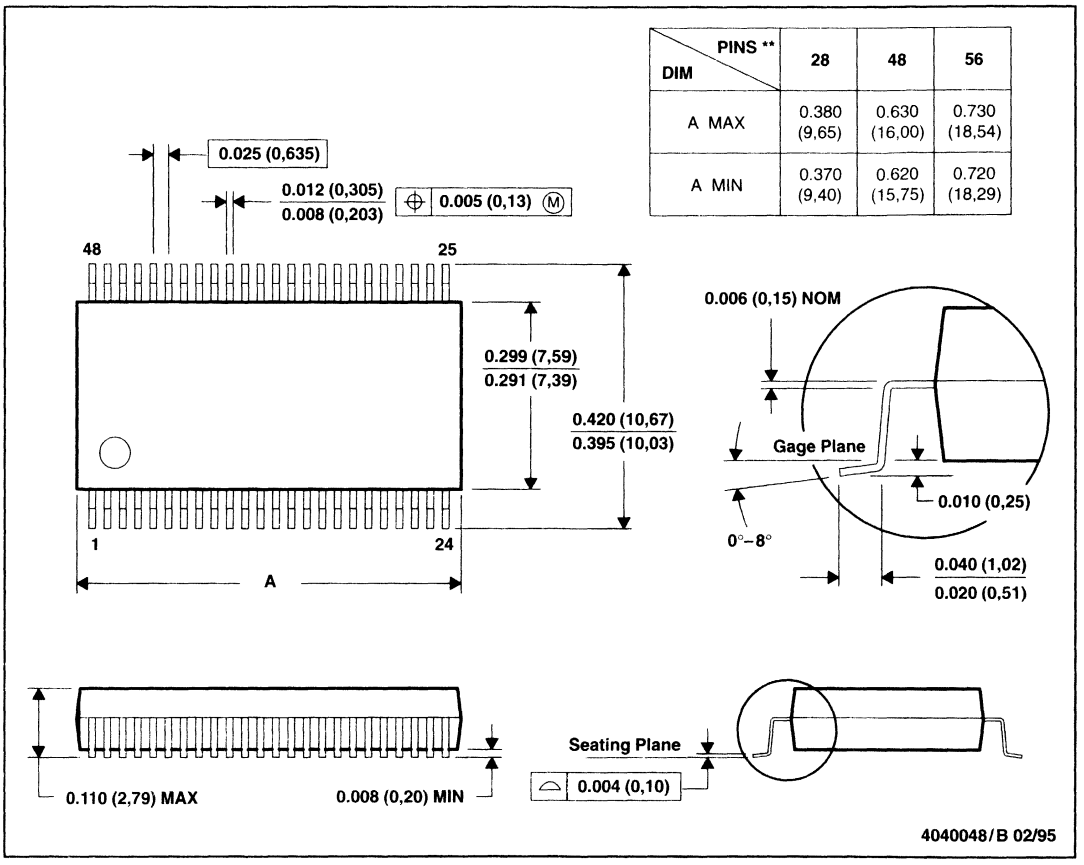
6 Mechanical Data

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PIN SHOWN



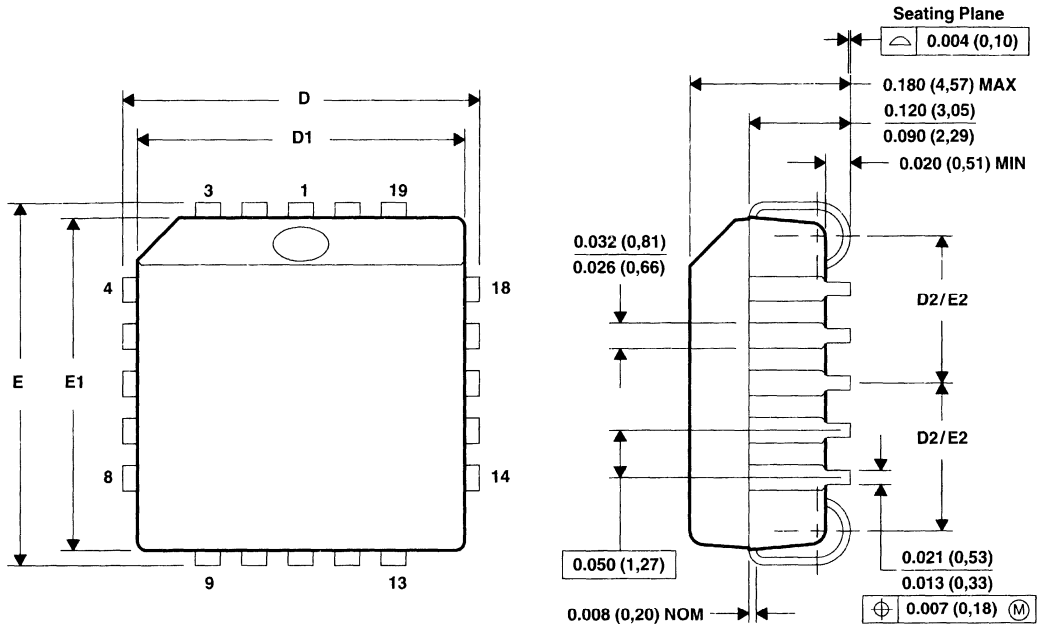
DIM \ PINS **	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

FN (S-PQCC-J**)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

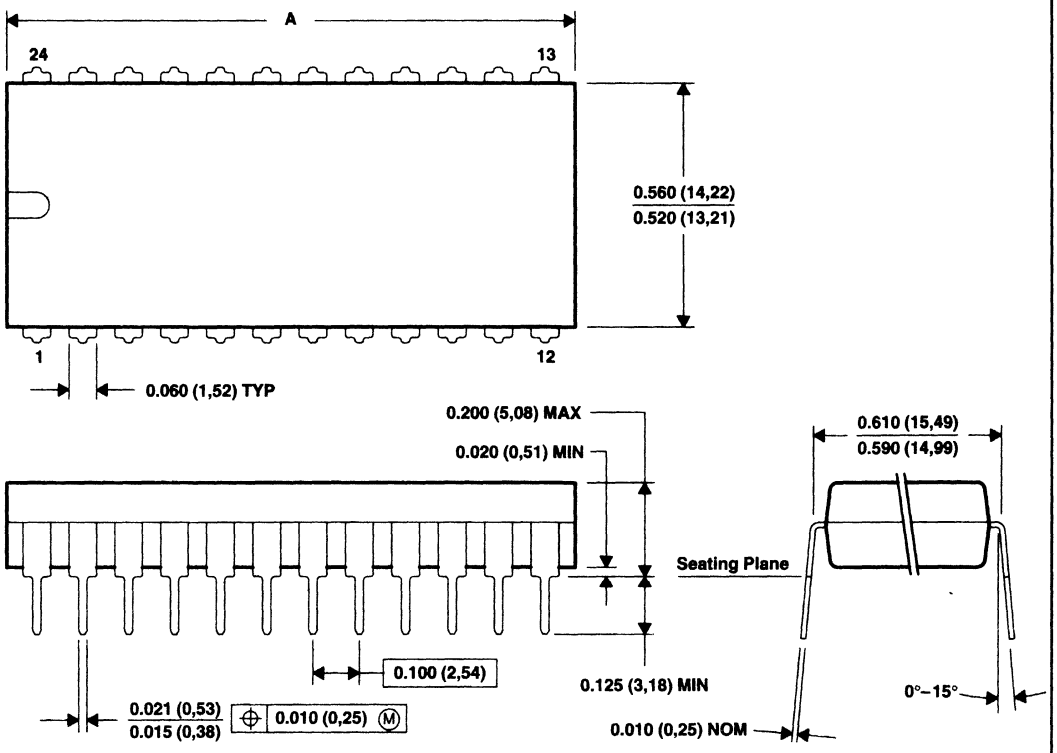
4040005/B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

24 PIN SHOWN

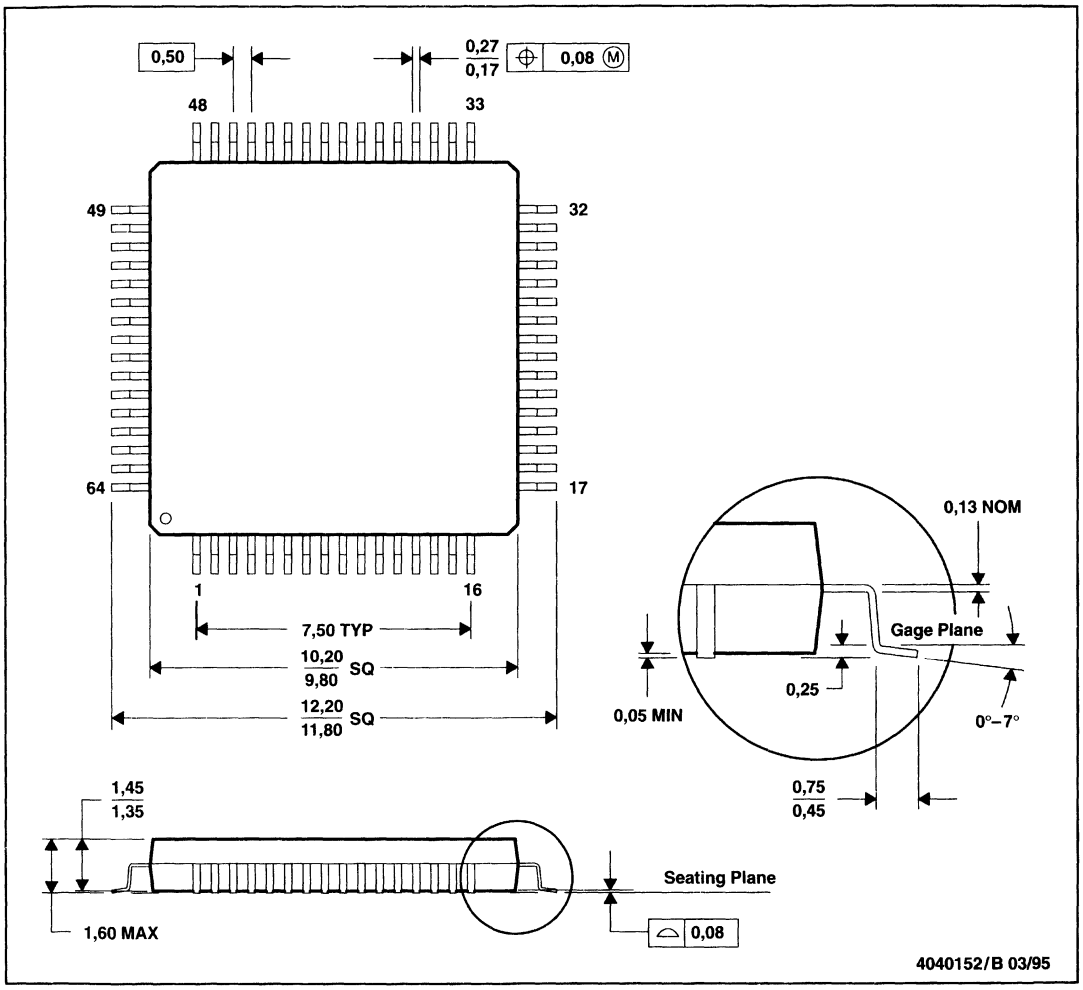


DIM \ PINS **	24	28	32	40	48	52
A MAX	1.270 (32,26)	1.450 (36,83)	1.650 (41,91)	2.090 (53,09)	2.450 (62,23)	2.650 (67,31)
A MIN	1.230 (31,24)	1.410 (35,81)	1.610 (40,89)	2.040 (51,82)	2.390 (60,71)	2.590 (65,79)

4040053/B 04/95

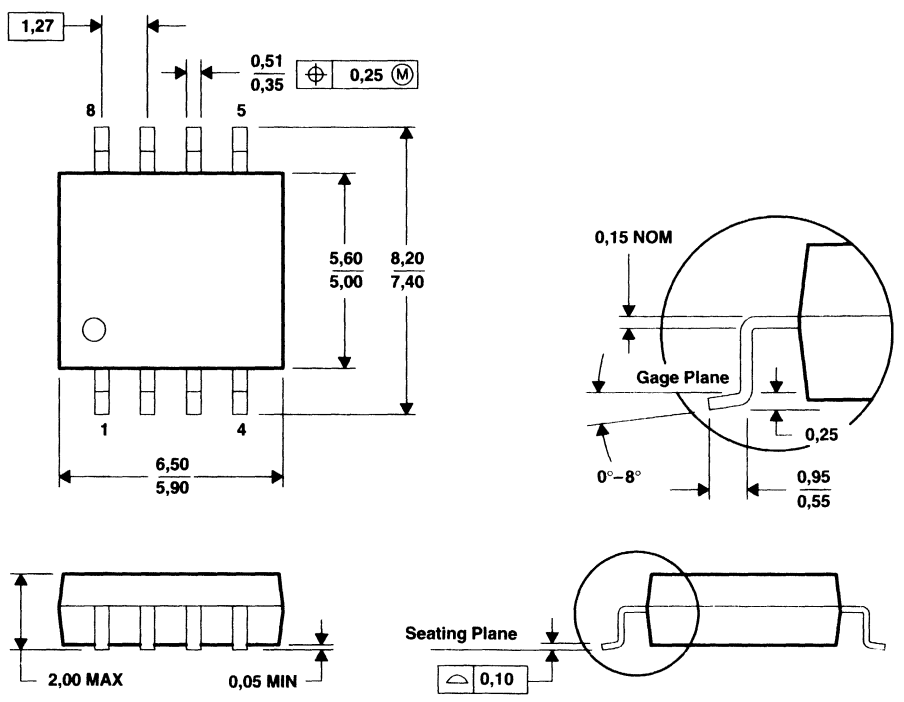
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-011
D. Falls within JEDEC MS-015 (32 pin only)

PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



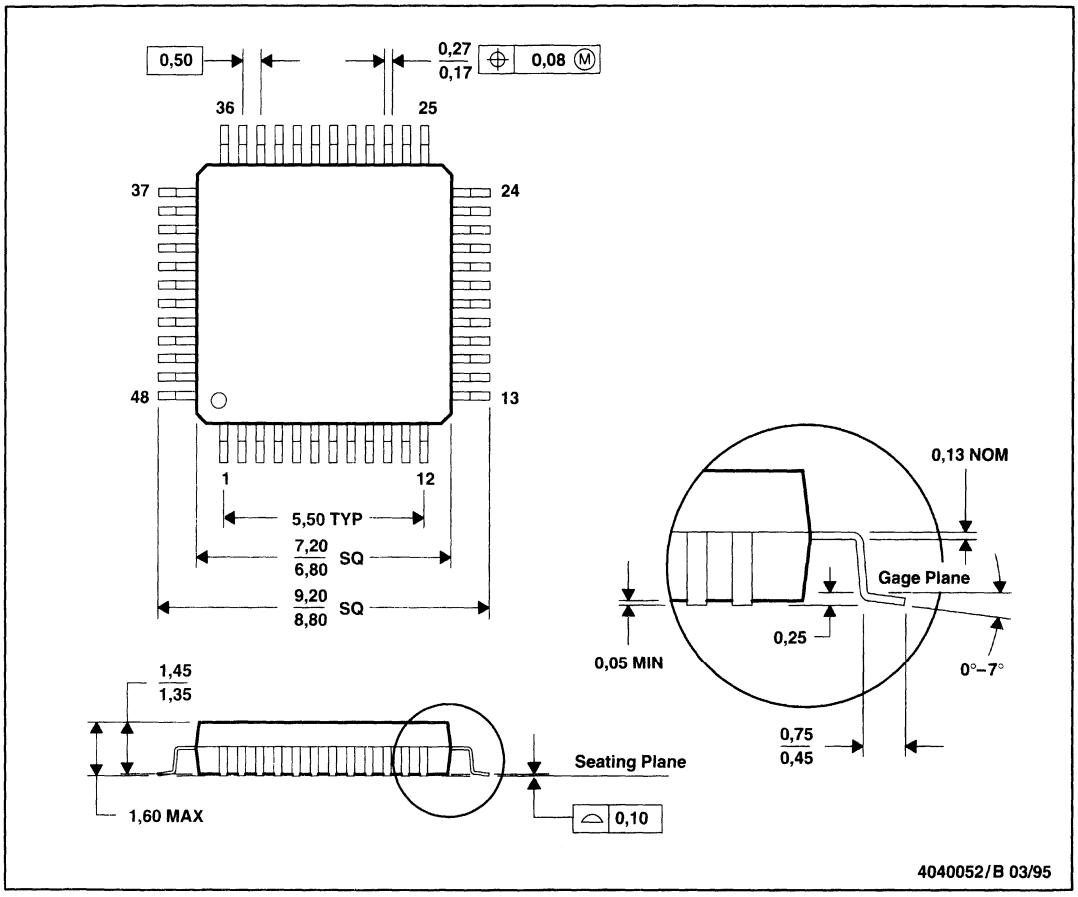
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



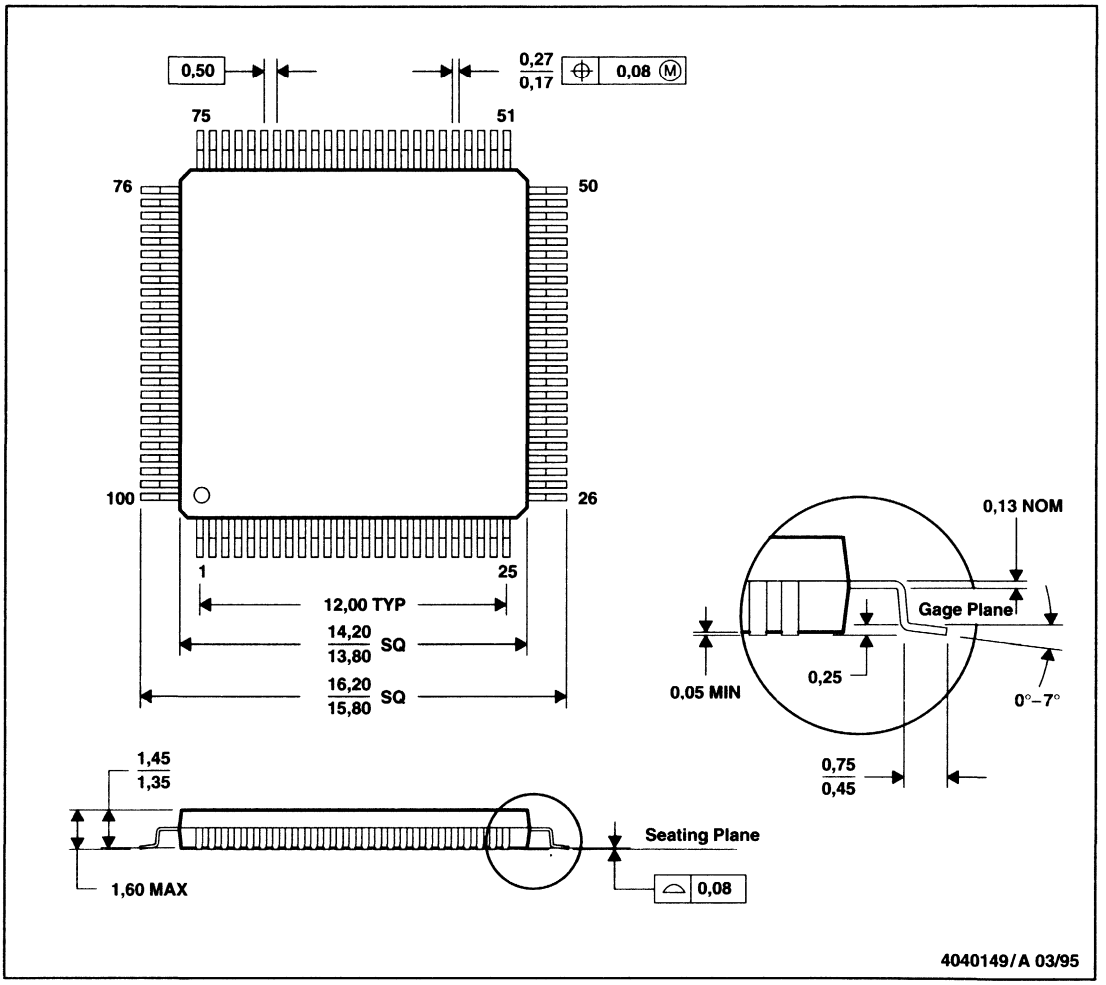
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PT (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136
D. This may also be a thermally enhanced plastic package with leads conected to the die pads.

PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

NOTES

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A022396

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3–96

SLLD003